Fundamentals of Micro and Nanofabrication
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Lecture – 02
Substrate

Hello! This is a lecture on substrates, which is part of a course on the Fundamentals of Micro and Nanofabrication. Any micro or nanofabrication starts with a substrate because that is where you make your integrated circuit or structure on. It's very important to understand the properties of that substrate and specifically, how to choose one, how it is made, and how the choice of a substrate affects the properties and the eventual application.

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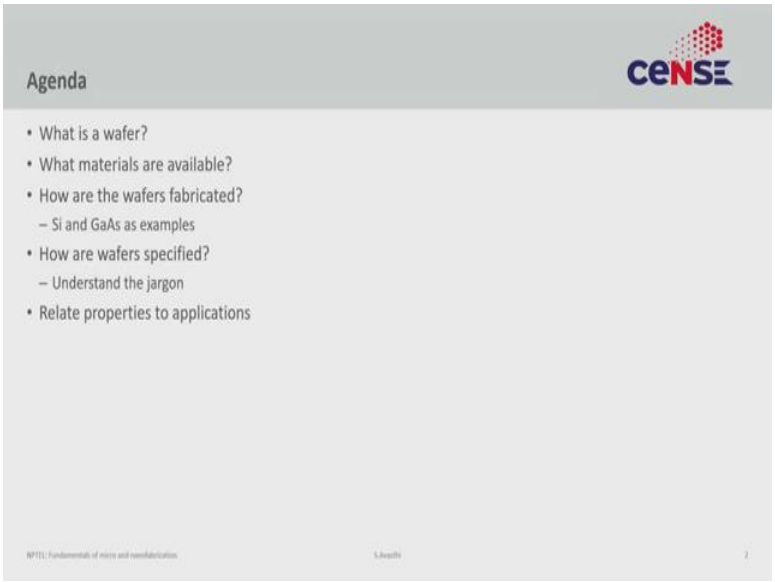

Our agenda: we will go over what is a wafer, why is substrate called a wafer in the first place. We will briefly discuss the various materials that are available. As you will see, while a lot of materials are possible, for most applications, a very small subset of materials or substrates is enough. Then we will go into details of how those wafers are fabricated because only when we understand how the substrate is made can we truly appreciate its properties. We will also go through some jargon to understand how the wafers are specified. If you were to purchase a wafer tomorrow, you may need to specify certain properties and what those properties are and what the jargon means is something

we will go over in this lecture. We will finish off with an understanding of how to relate the properties of the wafer to the eventual application (given an application, what type of substrate you need).

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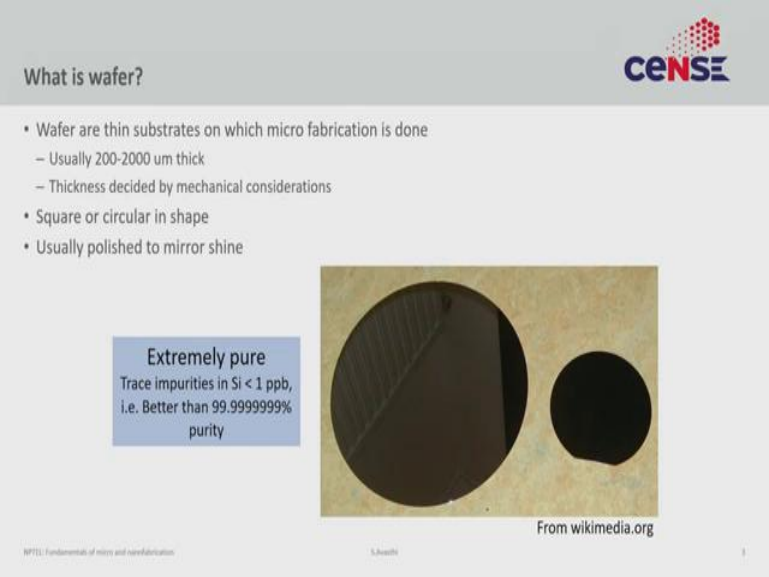

So, what is a wafer? As the name suggests wafer is a thin substrate on which the micro and nanofabrication is done. The name comes from historical reasons Here is an example of a silicon substrate and you can see that it looks like a thin slice or wafer and that is why the word wafer.

Typically, it is 200 to 2000 μm thick. This thickness is decided either by a standard, mechanical considerations or electrical properties, depending on the application. A little note on mechanical considerations: as the size of the wafer increases, for example, from a 2-inch wafer to a 4-inch wafer, there is a possibility that the large wafer will break if it's very thin. So, larger wafers tend to be thicker and smaller wafers tend to be thinner.

In general, wafers come circular in shape (a consequence of the way we make the wafer), but you can also purchase wafers in square shapes. Certain specialty wafers also come in a square shape for very specific reasons.

Typically, these wafers are given mirror shine. If you look at this image below, it has a shiny surface that reflects. This level of smoothness is important because when you are doing micro and nanofabrication on top of the substrate, any topology on the wafer will

also be reflected in your eventual structure. Flats surface gives you the best chance to accurately reproduce a micro/nanostructure.

Most importantly, these substrates are remarkably pure; much purer than what a typical material scientist or a chemist would call pure. If you want to purchase a chemical, 99.99 % or 99.999 % chemical is considered extremely pure. Wafers for micro and nanofabrication, especially those that need to be used in electronics have to be much purer than that. Routine silicon wafer that we use in our lab can often be parts per billion (i.e. 99.9999999 %) pure.

Silicon is one of the purest materials we know how to make irrespective of any industry. After the next few slides it will become more clear, how do we actually achieve this remarkable amount of purity. Here is the list of various materials that are available.

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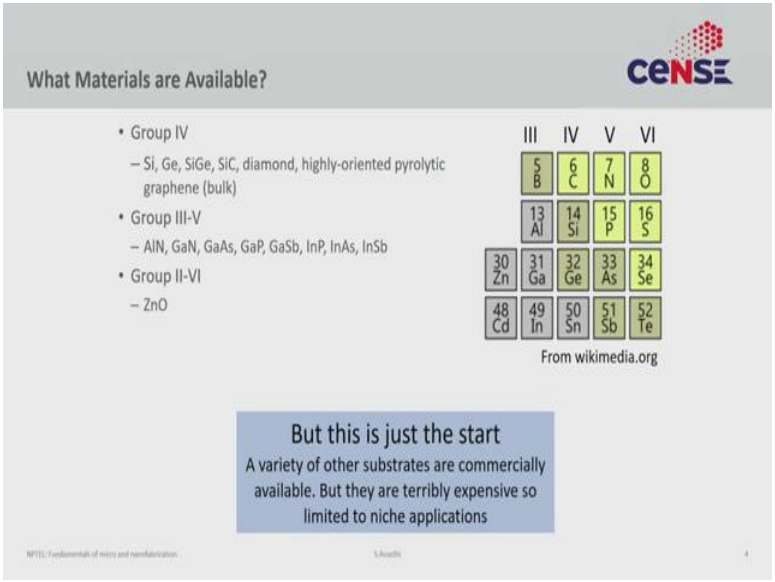

The workhorse for most micro and nanofabrication is silicon. On the right, you see a small part of the periodic table. You looking at group 4 which is carbon, then below that silicon, germanium, and tin. Out of those four elements, three elements: carbon, silicon, and germanium can all be considered semiconducting. In fact, the first semiconducting device was demonstrated on germanium and not on silicon.

As you go from carbon to germanium the bandgap reduces. This is not a course on electronics; we will not go into detail about what a bandgap means, but it sufficient to

say that the reduction of band gap has certain implications on the optical and electronic properties of the material.

Chemically, you can achieve the same number of “average” bonds if instead of taking a group IV element like silicon, you take one group III element, for example, gallium and one group V element which is arsenide. Gallium arsenide is also a semiconductor. You can extend this further to a whole family of what is called III-V materials. For example, aluminum nitride, aluminum phosphide, aluminum arsenide, aluminum antimonite etcetera and similarly with gallium and indium. These III-V materials are often used in optoelectronic applications.

Taking the same concept further, we can make a semiconductor by going to group II and group VI. A good example of that would be zinc oxide. Zinc is not group II material, but it does have an oxidation state of II. Similarly, cadmium sulfide, cadmium oxide cadmium arsenide are also semiconductors.

This is just the beginning. Semiconductor does not just have to be a binary like gallium arsenide, it can be a tertiary or ternary and all of that leads to a bewildering variety of substrates that we can actually purchase commercially. With the arrival of 2D materials and perovskites, the sheer number of semiconductors that we can purchase a substrate has increased significantly. In most of the cases, those substrates are only useful for niche applications. They tend to be extremely expensive, hard to make and available in very small sizes. By and large, if you are getting started in micro and nanofabrication you tend to look at silicon, III-Vs, oxides etcetera

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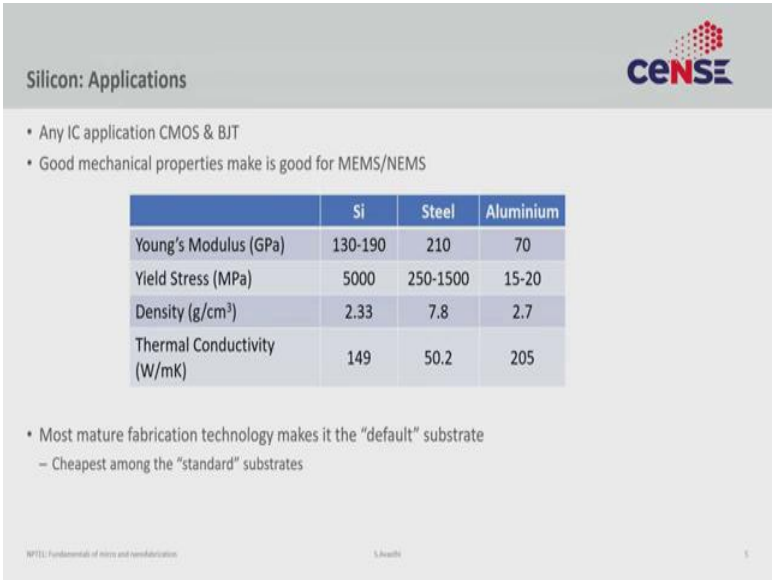

Let us go into details of silicon. It is used primarily in the IC industry. All the chips that you are using if you are using a laptop to look at this presentation, a mobile phone, the Internet etcetera that is backed up by circuits based on silicon chips. Silicon is used to make both CMOS and BJT types of circuits on which most of the microchips are based. (this course does not go into details of CMOS or BJT).

Beyond electronics, another very interesting aspect of silicon is its extremely good mechanical properties. Comparing some typical mechanical properties of silicon to steel and aluminum, you would notice that it has the same Young's modulus of elasticity as steel, its yield stress is extremely high, is very strong and the density is low which makes the structures light and its thermal conductivity compared to steel is much better and is almost as good as aluminum, which is a metal.

These are remarkably good mechanical properties that have allowed us to make microstructures that are also mechanical structures. This has allowed the preparation of MEMS and NEMS types of devices where the goal is not an electronic but a mechanical device. Silicon is the most mature platform that we have and is a good starting substrate for micro and nanofabrication.

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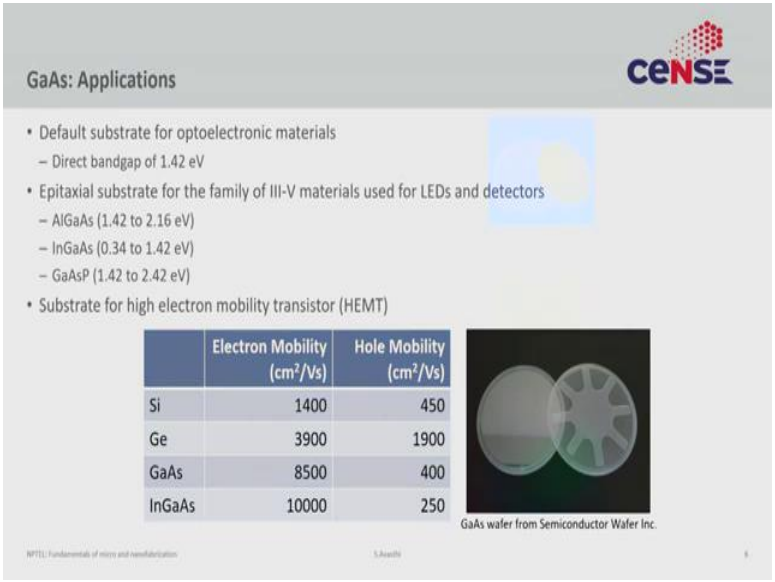

Next let us look at gallium arsenide, the most popular III-V semiconductor. A great advantage of gallium arsenide and in general, III-V semiconductors is that they tend to be a direct bandgap semiconductor. That means they are much more efficient in emitting light than silicon. So, gallium arsenide is often used in the LED type of applications. Any LED that you would have seen which is green or red in color or somewhere in between is probably based on III-V semiconductors.

Gallium arsenide bandgap can be tuned by alloying with other III-V elements like aluminum gallium arsenide, indium gallium arsenide or indium gallium arsenic phosphide over a range of values. This is very useful in optoelectronic applications because the color of the LED is directly related to the bandgap of the material.

Gallium arsenide, and in general, III-V semiconductors have very high mobility. Look at the table to compare the mobilities with silicon or germanium which are elemental group IV semiconductors. Gallium arsenide and indium gallium arsenide have much higher electron mobility. So, these materials are often used when very high mobilities are required and you form these High Electron Mobility Transistors (HEMTs).

Gallium arsenide is also used for (strategic) RF applications such as solid-state radars. It is a very interesting material with very interesting optoelectronic properties but the only problem is that it is significantly more expensive than silicon. It has played second fiddle

to silicon simply because it is much more expensive and harder to make. We will discuss in some detail on why is it so hard to make gallium arsenide compared to silicon.

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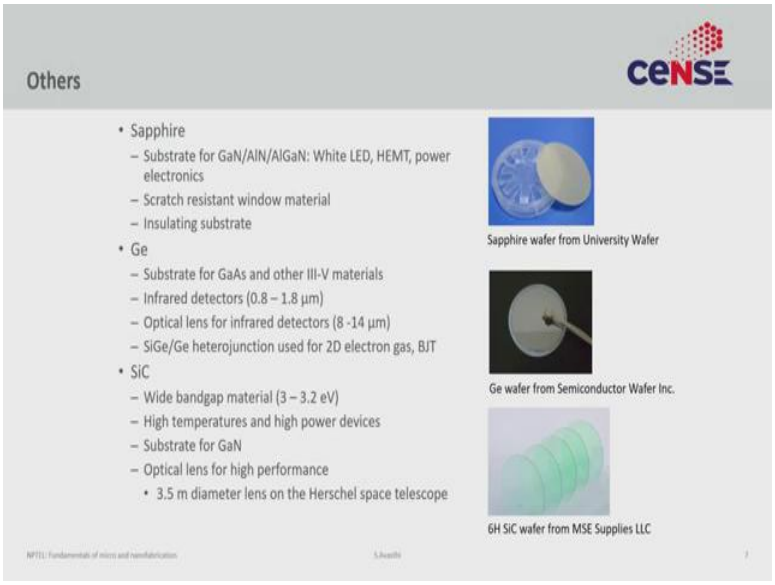

Here is a list of other substrates that we can look at, for example, sapphire. Sapphire is crystalline aluminum oxide. It is an insulating substrate. It is also used to grow nitrides. Gallium nitride has become an extremely important semiconductor and a lot of the gallium nitride HEMTs are made on sapphire. It also is a very hard material. If you remember your hardness scale, sapphire is right below diamond and that allows the use of sapphire as a scratch-resistant window material, for example, in the high-end watches.

Another interesting elemental semiconductor is germanium. As I mentioned earlier, germanium was actually the material on which the first transistor was demonstrated. Unfortunately, it has certain problems regarding its oxide which is why silicon became more popular than germanium in the long run; however, germanium as a substrate is still available and popular. A very niche application of germanium is that you can use it as a substrate to grow III-Vs on top.

III-Vs are not very compatible with silicon but are more compatible with germanium. When gallium arsenide substrates were very hard to make a lot of the gallium arsenide work was actually done on gallium arsenide that was deposited on top of the germanium. Germanium also is optically transparent in the infrared, mid-infrared and it's used in that

application. Germanium and silicon are miscible. So, you can form alloys, Si-Ge which have found a lot of use in HBT which is a faster version of the silicon BJT.

Next is silicon carbide, an alloy between silicon and carbon which is a group IV material. It is a very wide bandgap material; if you look at the image, you can see that the silicon carbide wafers tend to be transparent, indicating their high bandgap. The advantage with silicon carbide is it is a very stable material that can survive very high temperatures. The large bandgap allows it to function at high temperatures. So, high power devices where you want to flow a large current, silicon carbide has become very popular. It is also a substrate for gallium nitride just like sapphire was.

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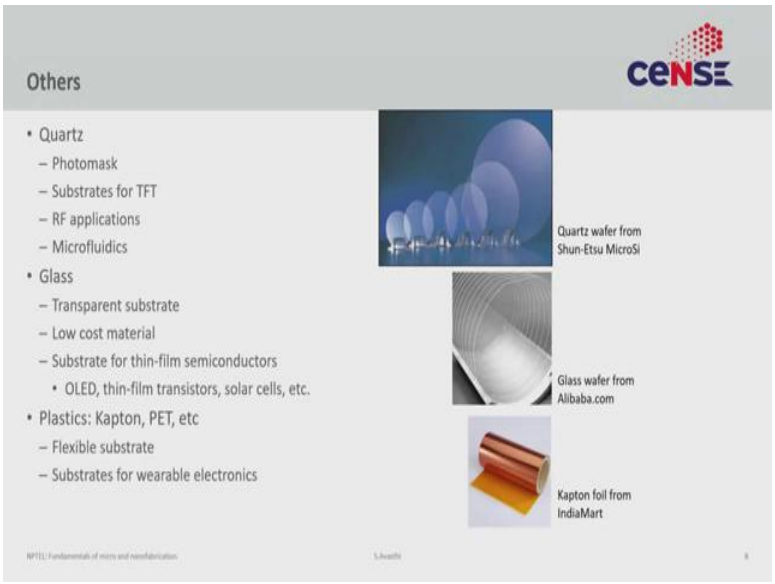

Next is quartz; quartz is silicon dioxide, but a crystalline version of silicon dioxide. It is transparent just like glass. The only difference between glass and quartz is that glass is an amorphous solid and the quartz is a crystalline solid. Quartz is often used in photomasks. We shall go into detail about photomask when we discuss lithography. Quartz is used as a substrate for thin-film transistors. It is also used in RF applications because it has very low losses and often used in microfluidics as a transparent substrate.

A cheaper version of quartz is glass, which also can be shaped into wafers. OLED, thin-film transistors, solar cells, displays for your mobile phones, for example, are made on glass substrates.

Plastics have become more popular as flexible substrates lately. In general, plastics do not survive very high temperatures which limit what sort of micro and nanofabrication processes we can do on them. In fact, it's a research area to try to reduce the temperature of micro and nanofabrication techniques so, that they are compatible with plastics. As that research area has matured, so has the use of plastics. The common ones are Kapton and PET; Kapton is yellow colored material that survives a little high temperature around 300^{o}C, which is high enough to do a lot of fabrication and actually make electronic devices on it. If you are looking at flexible, low cost and semi-transparent type of applications, plastic is a good place to start.

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After a general discussion on various types of common substrates that are available, let us discuss how do you actually buy them. If you go to buy a silicon wafer today, you would have to specify certain properties of that material. Here is an example of what typical silicon wafer specifications would look like. We have to specify the size (diameter) of the wafer. Back in the 1960s, 1 to 2-inch wafers were the state of the art because it was harder to make identical and standardized devices on large area wafers. Since then, as technology evolved, we were able to make them on larger and larger area substrates. These days, the industry standard is 300 mm (12") or 450 mm (17.7"). For most research applications, 4" is a good place to start.

You then have to specify the crystallographic orientation, since this is single crystalline silicon. The orientation refers to the orientation of the flat face of the wafer. It can be (110), (100) or (111). (100) orientation is the most popular for silicon wafers because it is the one that is used in CMOS and it is made in the highest volume.

The next is the grade. You can either select a prime grade, a solar grade, a test grade or a mechanical grade. The grade is determined by the amount of the impurity in the material and how well it was made. For electronic applications, you typically want prime grade silicon. For solar cells, where cost is important, a slightly lower solar-grade is used.

Test and mechanical grades are only used when you don't care about the electronic property so much. So, if you are doing some tests or trying to optimize a recipe for micro and nanofabrication, or you have a MEMS application where the mechanical properties of silicon are important, but electronic properties are not, you may consider buying test or mechanical grade wafers. They will be significantly cheaper.

How the silicon wafer was made or how the crystalline silicon was made also has a huge implication on the properties. Depending upon whether that method was float zone or czochralski or microcrystalline, the properties differ. We will look at each of these separately in the next few slides. So, for now, I will skip this.

Next, you specify the thickness depending on the application. Solar grade wafers tend to be thinner, standard CMOS grade wafers tend to be thicker. The thickness scales up as these wafers become larger and larger.

Next is resistivity, which refers to how much doping has been added to the wafer. Doping changes the conductivity (and hence, resistivity) of the wafer. Typically, it's specified in a range. You cannot have arbitrarily precise resistivity. Why? We will see that a couple of slides later. Resistivity values can be very low (<0.005 Ω-cm) for a highly doping wafer with $10^{19}/cm^3$ doping concentration to very high ~ 10^5 Ω-cm for an insulating wafer.

Next: surface finish. You would want a smooth finish on at least one of the face so, that is called a single side polish wafer, but for certain applications, you may want to make electronic structures on both sides in which case you want a double side polished wafer.

On top of that, you can also get some amount of preprocessing done on the wafer. If you do not have access to all the tools of micro and nanofabrication, you can request the vendor to do simple blanket depositions or processes. Those are typically optional and increase the cost, but are available.

Now let's talk about how we make a single crystalline silicon ingot.

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We start with polysilicon, which is silicon that has been purified to 99.999 %. For most material or chemical applications, it is essentially pure. So, that is the purest silicon you can buy and comes in chunks. What you then need to do is convert this polycrystalline, extremely pure, but not pure enough silicon into a silicon wafer. The first step is creating a single crystalline ingot.

The ingot has only 1 grain and can be much purer (1000 to 10000 times more) than the grade of the feedstock that you started with. Then you shape this ingot into a perfect cylinder by cutting off the beaks that you see in the ingot and smoothening out the wavy patterns that are on the surface. Then you cut this smoothened cylinder into wafers.

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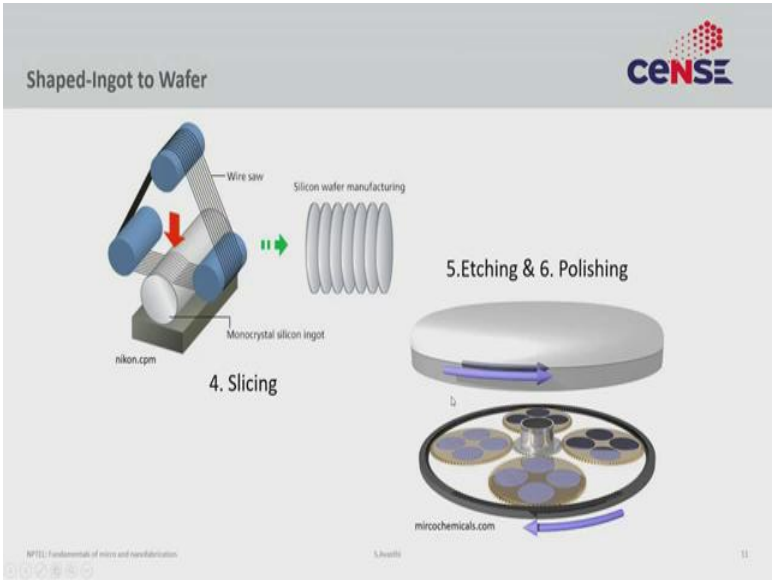

This process is similar to how a log is converted into round shapes. The diamond wire saw is used to cut the ingot down into thin slices. The distance between the wire saw decides the thickness of the wafer. This sort of sawing leaves certain striations on these wafers which are called saw marks. In order to get a smooth or mirror shine, you need to polish these substrates. That is done in this etching and polishing set up.

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Let us go into the detail of each of these steps. First is making the ingot from the polysilicon feedstock. The polysilicon feedstock is generally 99.999 % pure, and it comes from Siemens process that you can read up on the internet if you are interested.

Czochralski method is the most common method of converting polysilicon feedstock into an ingot. It was developed by a Polish scientist Yan Czochralski in 1918. It's a generic method of making any crystal ingot but is especially popular for making silicon. The technology has become extremely matured. We can now make ingots that are taller than humans and of very large diameter (as shown in the slide). Making such large ingots was not always feasible You will see why, in a few slides.

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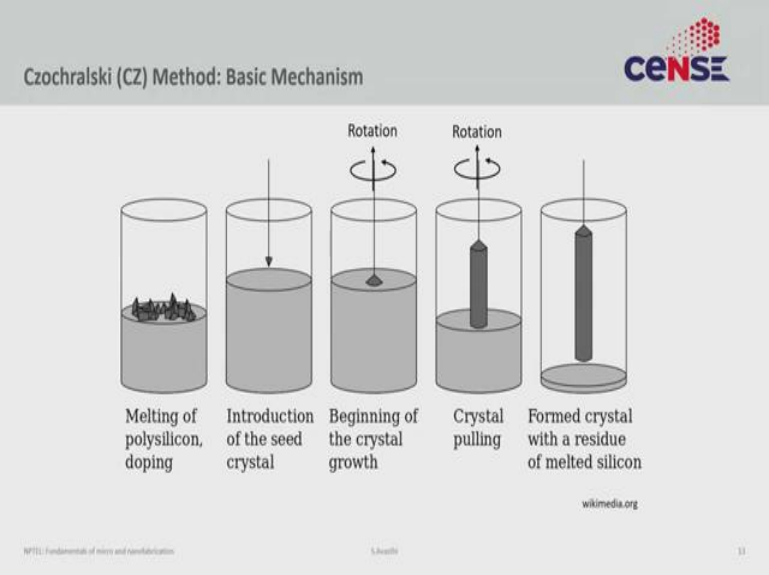

The basic mechanism of the Czochralski method is given in this slide. You start by melting the polysilicon feedstock. Heat it above the melting temperature of silicon, and once it has completely melted you can add a certain amount of dopants. The number of dopants you add will define the resistivity of the eventual wafer. Because you are dissolving it in a homogeneous solution the doping that you would get in this melt would be hopefully uniform.

Then you start with a seed crystal that has a certain orientation, which will decide the orientation of the ingot and ultimately, the orientation of the wafer. (111) oriented wafer would require a suitable seed. Starting seed is typically very small and hopefully single-crystalline; the size does not really matter as long as it is small. You would dip it in the

silicon melt and start rotating it. The rotation causes the ingot that eventually forms to be cylindrical in shape and homogeneous. So, this is why wafers are circular.

You rotate it and slowly pull it out. As you pull it out, the temperature of the silicon reduces and it starts freezing while it is in contact with the seed. Because it is in contact with the single-crystal seed, the silicon ingot that forms gets oriented along that orientation. As you keep pulling it, you continuously increase the size of that one grain.

Because of the rotation, you get a cylindrical shape. As you keep pulling the ingot, the amount of the melt reduces and you continue this process until your melt is exhausted. So, what you have done is, you have started with polycrystalline pieces of silicon and converted into one single ingot of single crystalline silicon.

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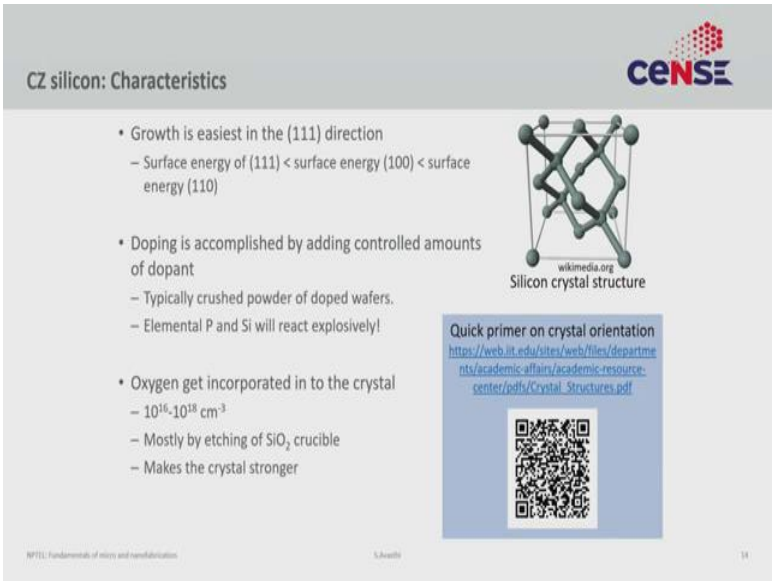

Whatever seed you select will decide the orientation, the easiest growth is done along the [111] direction (this is just the property of silicon) because of the surface energy of (111) < (100) < (110). So, (100) is a little harder to make than (111) and (110) is even harder, which is why it is more expensive.

If the nomenclature on the orientation is not obvious to you, I would urge you to read up a quick primer on crystal orientation (QR code in the slide) So, you understand, for example, that the silicon has an interpenetrated FCC lattice and silicon atoms are tetrahedrally bonded to other silicon atoms.

Doping is accomplished by adding control amounts of dopants. Elemental phosphorus and silicon will react explosively, so it has to be done carefully (that detail we shall not cover here). An important aspect of this process is that oxygen does get incorporated in the crystal; the concentration of oxygen is typically 10^{16} to 10^{18} cm^{-3}. This essentially means 0.01 to 0.001 % oxygen, which mostly comes because the crucible that we are keeping the melt in is often made of an oxide - silicon dioxide or aluminum oxide and oxygen from that leech into the melt.

Electronically speaking this does not prove to be too much of a problem so we do not care about it and a happy side effect of this oxygen is that it actually increases the crystal strength making the wafer a little more resilient. So, the CMOS industry actually wants some of this oxygen in there.

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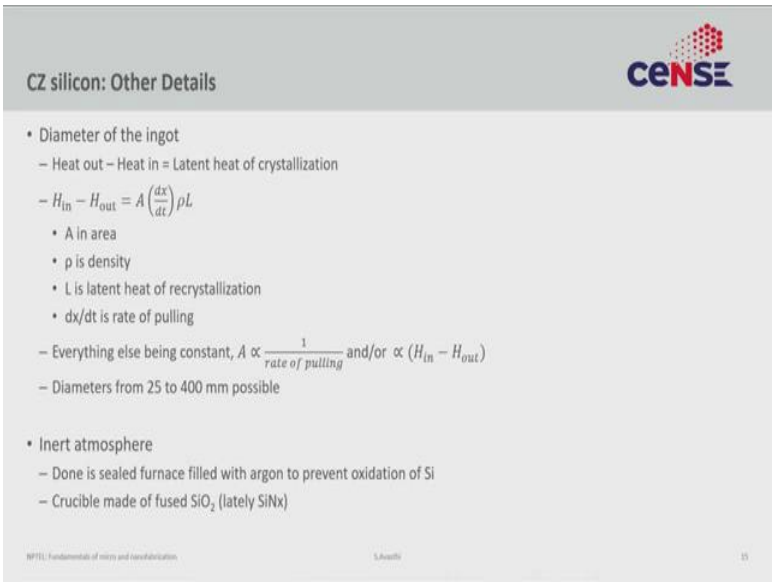

Another very important detail is the diameter of the ingot. As silicon technology has matured we have started growing larger and larger ingots. So, how do we control that process? we simply look at the thermodynamics. Assuming this is a closed system where we are putting in some amount of heat by heating the crucible, some amount of heat is being lost and the rest must be taken by the latent heat of crystallization, which is described by this expression.

Everything in this expression is either a geometrical factor such as the area, or a material constant for example, density and L. The thing that we control is the rate at which we are

pulling the system and the amount of heat we are providing the system which is H_{in}. So, controlling these two factors we can actually achieve a certain area assuming everything else remains the same.

Looking at this expression, you can probably appreciate why it is harder to make larger diameters (A). The rate of pulling for larger diameters must be extremely slow. So, this has to be a very slow and controlled process. Also, for the larger diameters, the difference between the heat that you are putting in and the heat that you are losing must be fairly large, making the thermal management difficult. The thermal management is easy when the amount of heat being supplied is small but it is much harder when the amount of heat that you are supplying is much larger. It has taken some amount of maturity and time before we were able to develop control systems that can manage this process very precisely.

As of today, the industry can routinely make ingots of various standard sizes, ranging from 25 mm to 400 mm. Most of this is done under an inert atmosphere or partly so that the silicon does not oxidize. The crucible must be made from some reflective material because at the end of the day you are holding this very hot silicon melt. It is often made of silicon dioxide, but also lately silicon nitride.

In the next lecture, we will go into detail on how the CZ growth happens and the concept like supersaturation to explain the crystal growth process.

So thank you.