Fundamentals of Micro and Nanofabrication Prof. Sushobhan Avasthi Centre for Nano Science and Engineering Indian Institute of Science, Bengaluru

# Lecture – 58 CMOS integration

In this lecture, we continue the general module on process integration. We were looking at making silicon solar cells at an enormous throughput and low cost. We started with the wafer, done texturing, cleaning, diffusion, and  $Si_3N_4$  deposition using PCVD. In this lecture, we will deposit electrodes, create modules, and put the whole thing together into something you can sell.

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In the wafer cross-section, you have doped phosphorus (orange layer) on both sides, as we dope without any patterning. The back phosphorous doped layer will later go away. We have a layer of PECVD  $Si_3N_4$  (dark blue) to reduce reflection. Now we deposit metal. If you notice, we have completely gotten rid of all patterning processes. We have not done one lithography, and we shall not do any! For 100 µm features, lithography is overkill and extremely expensive. It is using a Ferrari where a tractor works. The industry has moved away from lithography to more scalable and cheaper patterning methods, specifically, screen printing. Screen printing can't do anything thinner than 10-20 µm, but it is enough for solar cells where the features are around 30-40 µm.

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A screen printer has a screen attached to a frame. The screen has the mask pattern; It has holes from which ink can go through. You attach a screen and add some metallic paste (silver, aluminum). It is not a fully formed metal but a sticky, viscous, semi-liquid paste with organic materials that allow it to flow. You dry it and cure it at a high temperature. During curing, the organics desorb and leave behind the silver or aluminum to make the metal contact. The metal paste is a specialty product sold by specialty people; that gray liquid in the cartoon.

A squeegee is like a blade, post against this screen as you drag it from left to right. The edge pushes the paste out through the screen holes screen and prints it on the substrate. The screen pattern transfers to the substrate. If you zoom into the screen, you see a steel mesh. Your ink goes through these holes in the mesh. To make a pattern, you add some ceramic plates that block the holes so the metal paste won't go through, where you don't want it to go through. How small you can print is some function of what the smallest hole you have in this mesh. If you try to print something smaller than the mesh opening, it will not look continuous; it would look jagged and break.

So the mesh decides the critical printing dimension. What is stopping you from making a finer mesh? A finer mesh provides more resistance to the ink flow. Your ink must be more fluid, but then it will spread out and not hold shape. There is this delicate balance where you want the ink to be viscous enough to hold shape, but not so much that it can't

go through the holes when we push. At the current state of the art, you can't print reliably below 20-30  $\mu$ m. Most commercial Indian manufacturers that I know print somewhere between 30-60  $\mu$ m. So, that is the thinnest they can make. You call these thin lines fingers and the thick trunk busbars. Pattern transfer happens without using photolithography through a squeegee and a screen printing machine.

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First, we coat aluminum paste at the back and make the back-electrode. We leave some holes to deposit silver. This silver is where we make a solderable contact, and the aluminum is our p-type dopant that will form this  $p^+$  layer. During printing, it is just a liquid. It happens during firing when this paste dries, and aluminum diffuses. Currently, the aluminum paste is wet; BSF will form down the line. Then you deposit Ag.

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The front and back Ag pastes are slightly different because the front Ag paste must penetrate the  $Si_3N_4$  to contact silicon. If you remember the diffusion lectures,  $Si_3N_4$  is a pretty good diffusion barrier or a masking layer. So, you add some grit to the Ag paste to make it able to break through the  $Si_3N_4$ . Once again, we have avoided a lithography step!

You pattern the metal using screen printing + firing; You don't have to pattern  $Si_3N_4$  separately. In this slide, you see an inline screen-printer. You can see the wafers coming in and going out. Within seconds, you can print these front electrode patterns and do it continuously. Remember, these are still semisolid viscous liquids; they are not dry yet. First, dry them and then fire to form metal.

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For firing, you send the wafers through a belt furnace. It is a continuous, low-cost, inline process. They don't like batch processes. The wafers go in from the back and come out from the front. Inside the long furnace, there is a whole range of temperatures, and you precisely maintain this profile. All the metal layers (back Ag, front Ag, Al BSF) cure simultaneously. It would take too long if you do it one after another, so they have optimized one firing step to curate all the three pastes. As you form Al BSF (back surface field), you eliminate that phosphorous doped layer (orange) by overriding the P-doping with Al-doping, making it  $p^+$ . So, you have the  $p^+$ , p-layer, n-layer, Si<sub>3</sub>N<sub>4</sub> on the top, Al at the bottom, and silver contacts. That is how you make commercial silicon solar cells.

I want to highlight how important these small optimizations are. Here are four different recipes tried in this furnace, where the temperatures in each of these six zones were slightly different. With minimal temperature changes, you can get small efficiency changes. For researchers, the difference between 16.25 and 16.6 may be minuscule; For a commercial fabrication system producing thousands of wafers/hour, each small efficiency improvement may be worth a few million dollars!

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This image shows an SEM of the final structure: p-type silicon, front Ag electrode, back Al paste, Al BSF, and  $p^+$ -p junction.

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This slide shows the top and bottom view of a commercial silicon cell.  $Si_3N_4$  gives this blue tinge at the top; You see the front electrode, the Al BSF, and the back Ag electrode. You have to connect these different cells in series to form a module by soldering the busbars. You solder one busbar to the next by tabs. You see this tab, metal wire connected to the wafer. In the end, you combine these tabs to form a module.

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Before that, however, you have to test and sort. Thousands of wafers come out an hour, and not all of them have precisely the same efficiency. In a module, all the cells are in series; they must have the same current, or you lose considerable efficiency. People sort it in the bins of different efficiencies, and the number can be 16-20. For doing a module, you take wafers from one bin; you don't mix and match. As this lady is doing, you can sort manually or have automatic systems measure the efficiency and sort the wafers in appropriate holders. So, you have to do testing and sorting before.

Typical modules have either 60 or 72 cell modules. These days, people have started making much larger modules, but the vanilla modules are 72 cells of 6".

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The module is a structure that provides these cells with some physical support, so they work in the field without damage. 180  $\mu$ m thick silicon can quickly wear or crack. In the cross-section, you have these p-n junctions connected in series. These tabs make contact from the top n-type to the bottom p-type. You join 72 cells one after the other; that is just the electrical part. To protect them from the environment, you have the top tempered glass, often with some anti-reflection coating. You can have a glass on the back if the module accepts light from both sides; that is a bifacial module. It is not very common; the more common thing at the end is mechanical support. So, it has some Tedlar (some polyvinyl fluoride) film. Between this glass and the back surface, you have a lot of space, which is undesirable as the wafers can move around. You fill it with some pottant like EVA; EVA is a petroleum-based product.

A lot of the shoe soles are probably EVA. The ones you use are transparent and stable. All this yellow is EVA that fills all the nooks and crannies and immobilizes the wafers. You see the aluminum frame, front glass, wafers, encapsulant (EVA) film, the back sheet, and the wafers. Finally, electrical connections have to come out. You attach a junction box and connect it to the wires. The aluminum frame provides some rigidity. So, it can withstand some abuse during installation.

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You have 72 cells ( $6 \times 12$ ), and each module is ~  $1 \times 1.5$  m in size. The multi-crystalline wafers are square-shaped, so you don't have any dead space in the middle. The monocrystalline cells have rounded corners, so in a module, you see these squarish open shapes. That area is lost, but there is nothing you can do about it. As the technologies have progressed, silicon solar manufactures have tried to reduce this dead space. But it still exists. From the presence or absence of the holes, you can tell if it is monocrystalline or multi-crystalline. The monocrystalline cells also look a little darker or blacker; they have better texturing because it's easy to form pyramids on those. Multi-crystalline wafers don't have that good texturing. So, they reflect a little and have this bluish tinge. You can see the grains in the multi-crystalline cells but not in the monocrystalline cells.

Depending on the technology, a typically 72 cell module gives between 300 - 400 W. Mostly 320-340 W, rarely > 400 W, unless you have a heterojunction or some other advanced technology. Although they are also doing (slightly different) microfabrication, the silicon solar cell industry has reduced the cost by avoiding photolithography. They still make very efficient and marketable electronic product.

This lecture is my last lecture for this course; thank you for your time.