Switching Circuits and Logic Design
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Lecture – 32
Latches and Flip-Flops (Part II)

So, in the last lecture we talked about 2 different kind of latches; the S R latch and the D latch; we also considered the variation of the latch with an enable input. So, we continue with our discussion today in the second part of this lecture on Latches and Flip-Flops.

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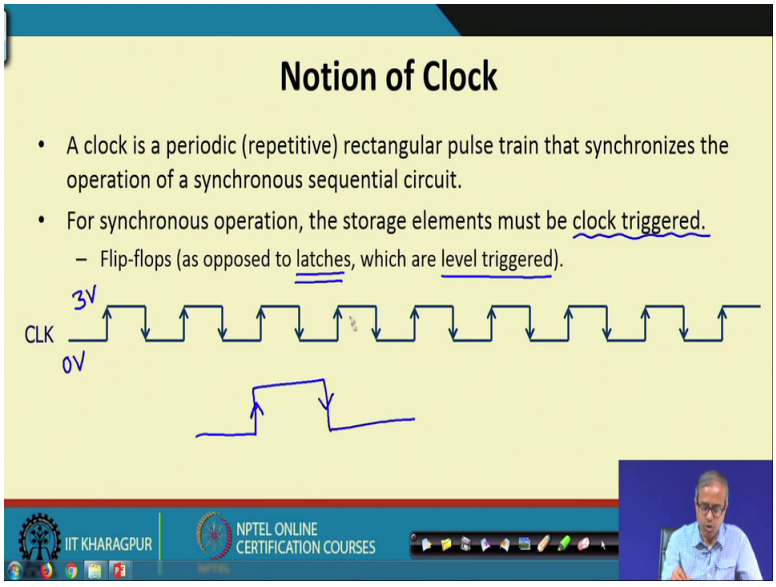

So, we shall be talking about clocks, the notion of a clock and how we can modify our design of the latch to make it a flip flop, which can be operated by a clock. Now let us try to understand why we need this kind of a clock and what is a clock?

See a latch I mentioned if you recall in our last lecture it is level triggered; for example, in an S R latch whenever you apply S R 0 1 or 1 0 and apply enable equal to 1; the output will be set to 0 or 1 accordingly, similarly for a D latch.

So, whenever the inputs are changing the output is changing immediately after the gate delay of course. But for a flip flop we talk about something called an event; output do not change immediately when the inputs are changing; we have the notion of time there is something called a clock. Whenever there is a clock signal only then the outputs are

supposed to change in response to whatever we are applied in the inputs. So, clock gives some kind of synchronous kind of operation for a sequential circuit. It tells you well inputs I can change any time I want, but when the outputs are going to change that will be determined by the clock.

So, let us see formally what a clock is; a clock is a periodic rectangular pulse strain just like what is shown here in this diagram below. It is a repetitive pulse strain this signal goes up and down, up and down well it depends of course, on what kind of logic system you are having. This low level can be your 0 volts, the high level can be 3 volts, 1 volts, 5 volts; it can be anything.

So, it can be just 2 levels of voltage and you see whenever there is a clock signal coming like this; there are 2 events 1 event is when the clock is going from low to high and the other event is one it is going from high to low. So, I can say that my circuit will be triggered by some edge of the clock I call it clock triggered

So, I can say it is triggered by the leading edge or the positive edge or the falling edge or the nomine negative edge of the clock positive edge triggered, negative edge triggered. Well in contrast in latches I mentioned earlier these are triggered by voltage levels and such clock concept is not there in a latch fine.

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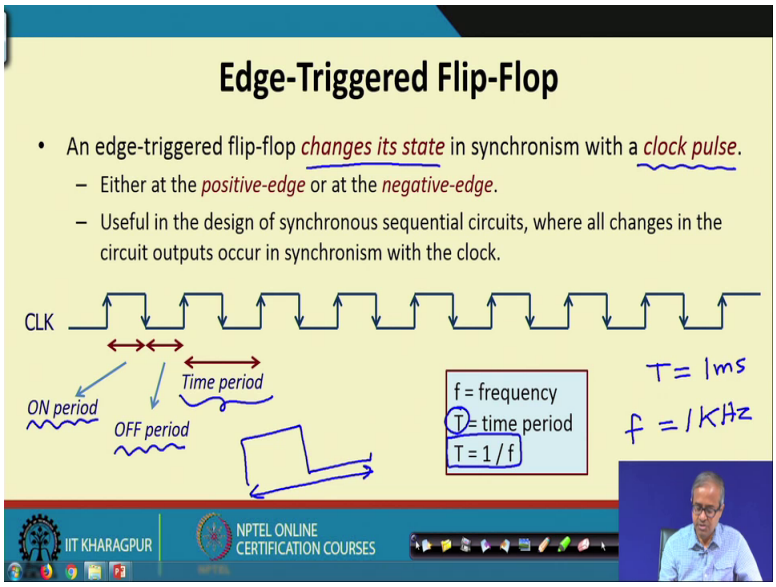

So, with this background we shall be trying to explain what so called edge triggered flip flops are. You see flip flop is nothing, but an extension of the latches same kind of logic applies; say for an S R latch depending on the S R values the output will be set to 0 or 1. For a S R flip flop for example, same concept is there you apply some S R values, but the output will change only when there is an active clock signal that is coming, only when there is a clock the output will be set to 0 or 1 right.

So, at edge triggered flip flop basically it changes its state in synchronism with a clock signal or a clock pulse. So, we have already said how a clock signal looks like; now a clock signal is characterized by the time during which it is high this is called the on period. The period it is low it is called the of period and the total sum of the on period and of period this is called the time period.

So, the clock going up, down here and again going up this total time duration is called the time period. And if T denotes the time period then the reciprocal of it 1 by f is the frequency or the other way round; if f is the frequency then 1 by f will be the time period.

Ah. So, I can say if my T is for example, if my this time is 1 milliseconds then my frequency will be 1 by T which is 1 kilo hertz. So, in 1 second there will be 1000 times up, down, up, down this kind of things that will happen. And we use clocks to synchronize operations in a sequential circuit. And this synchronization can happen either at the positive edges of the clock which are these when the clock is going from 0 to 1 or at the negative edges of the clock which means here when the clock is going from 1 to 0 right. So, when we design a circuit all output changes will occurred in synchronism with this clock edge; positive edge or negative edge fine.

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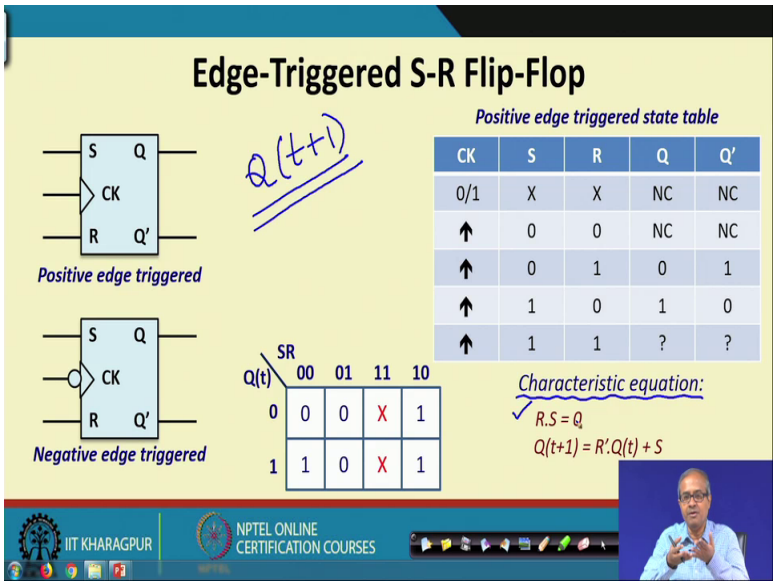

Let us now look at a edge triggered S-R flip flop; now you already know what an S R latch is let me try to explain what is shown in the slide. First is this symbolic notation in a diagram how you show and S R edge triggered flip flop. You see in an S R latch you have S and R Q Q bar outputs; here in addition you have another input called clock and this is how you show a clock just by a this angular symbol here.

Now if we show it like this, this indicates positive edge triggered that whenever the clock is going from 0 to 1; the output will change during that time. But if we use a small circle or a bubble here like it shown here, a small bubble before this triangle this indicates negative edge triggered, where the output will change whenever the clock is going from high to low.

So, just in a circuit diagram whenever you show a flip flop you either show this bubble or do not show this bubble this will indicate whether it is positive edge triggered or negative edge triggered right. Let us assume that we have a positive edge triggered S R flip flop; so, what will be the state table like? You see here instead of enable, we have used a signal called clock.

What does this table says? It says the clock can be either 0 or 1, but no leading edge or positive edge. So, it can be either continuously 0 or continuously 1; no problem there will be no change in the output. The outputs will change only when there is a positive

going transition in the clock; that means, clock is going from 0 to 1 only during that time this circuit operation will take place and output will be changed.

So, for a latch we had the enabled signal whenever enable is high the latch was open; here whenever the clock edge is coming only exactly at that point the output will be evaluated this is the idea. So, whenever there is an edge well the rest is exactly like an S R latch that is same behavior; 0 0 means no connection, 0 1 means no change, 0 1 means output is 0, 1 0 means output is 1, 1 1 is invalid.

Now, from this behavior we can write down the characteristic equation of an S R flip flop means what is the output expression. Now see for a flip flop there is a notion of a clock clocks are coming 1, 2, 3, 4, 5, 6; I can count how many clocks are coming. So, we use this notation the value of the output Q at time t plus 1; Q t plus 1 indicate what will be the value of the output when t plus 1 th clock pulses come; just after t th clock pulse.

The characteristic equation says two things first it says R and S must be 0 which is an indirect way of saying both R and S never be 1. Because if R and S are 1 then end will be also be 1; it says its end must be 0 and second 1 is it also tells what the next Q will be in terms of the present states.

So, you see you can draw a Karnaugh map and you can derive this expression how have comment come to it. You see in a Karnaugh map on this side I am showing the S R this S and R inputs and on this side I am showing the output at time t; that means, in the previous state what the output was. Well why I need this? You see if my S R input is 0 0; it is supposed to be no change; if it is 0 0.

So, if the previous output was 0; it will remain as 0, if the previous output is 1 it will remain as 1, but if my input S R is 0 1; then the output is definitely 0 it is definitely 0. And if it is 1 0; it is definitely 1 definitely 1, but because 1 1 is not a valid input, we can mark it as a do not care right; so we have the Karnaugh map.

So, in this Karnaugh map; you see I can make 1 Q like this will be 1 latch Q and 1 Q like this will cover all the ones this latch Q is nothing, but S and this Q will be Q t here and in this case it will be R bar R bar Q t. So, R bar Q t or S this will be the expression for the output when the clock comes it will be evaluated according to this expression right.

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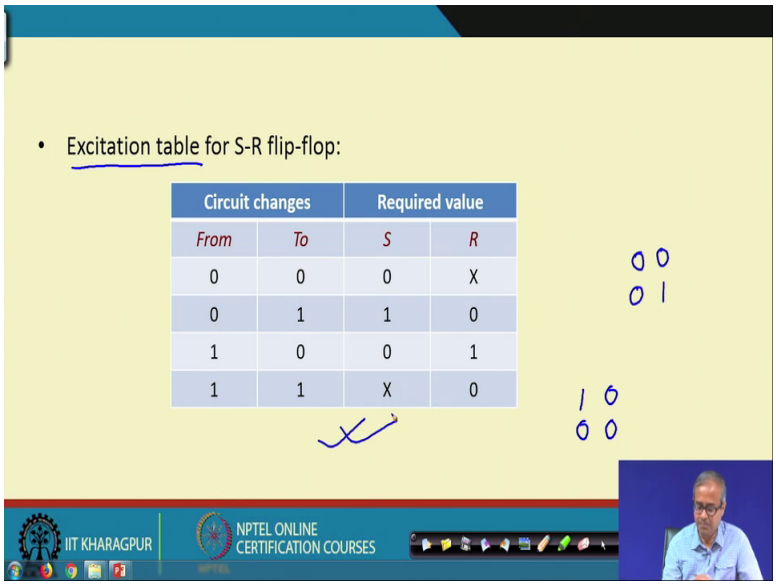

Now, another thing we define for a flip flop; it is something called excitation table now excitation table means we can setup flip flop to 0, we can setup flip flop to 1.

Now, only that you also want to see that how we can change the output of a flip flop from 0 to 0, 0 to 1, 1 to 0 or 1 to 1 all possible 4 combinations this is shown by something called an excitation table this excitation table says that when the circuit output changes from all possible 4 combination 0 to 0, 0 to 1, 1 to 0 1 to 1 what is the required S R values I have to apply say the output was 0 I want to change it to 0; that means, no change means.

So, I can either apply 0 0 or I can apply 0 1; so, I am writing 0 do not care. See if I want to change from 0 to 1, there is only one way I have to set S equal to 1 R equal to 0. Similarly from 1 to 0 I have to set S equal to 0 R equal to 1 and it is 1 it remains at 1; then I can either apply 1 0 or 0; 0 0 means no change; that means, do not care 0, do not care 0 this is the excitation table of the S R flip flop right.

For any flip flop we can design and write down such an excitation table. Now let us look at a simple timing diagram for an S R flip flop; I am just showing suppose I have a sorry let us go back.

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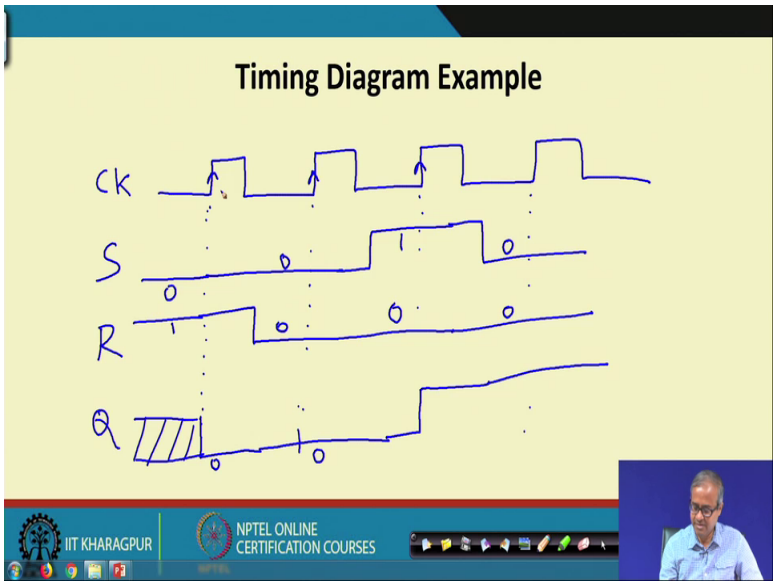

Suppose I have a clock signal let us say I have a clock let us consider there are 4 such pulses coming clock signal. And the flip flop is positive edge triggered I am assuming it is positive edge triggered, it is triggered on this edge this triggered on this edge.

Now let us assume some values on S and R suppose my S value is like this and I am also showing the value of Q. Suppose initially my S value was 0, S value was 0 and R value was 1 R value was 1. So, when the first clock edge comes here it says that S is 0, R equal to 1. So, the value of Q will be 0 over; earlier Q can be anything I do not know what Q was earlier; so I am showing it like this; I do not know what is Q was.

But after the clock edge comes because S is 0 R equal to 1, Q will be 0 definitely. Now suppose this S remains as 0 and R also becomes 0; so, both of them are 0 0 here when the next clock comes. Now 0 0 means no change; so output Q was 0, this will remain as 0. So, so even after this it will remain as 0; now let us say this S is becoming 1 here and R is remaining 0.

So, now, S is 1 R is 0; so, at the third clock this output will be becoming 1 because S 1 R 0 and let us say this S is again becoming 0 here and R remains 0. So, 0 0 is no change; so, this will again remain at 1.

So, a simple example I am showing this is just a timing diagram that with respect to S R flip flop. As the input changes and as the clock edges comes well how the things go on changing right.

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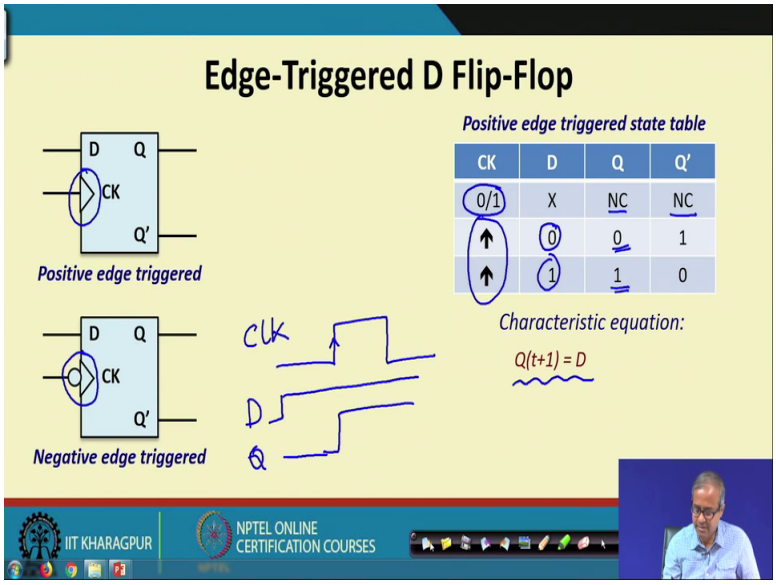

Now, let us talk about the edge triggered version of a D flip flop; it is exactly similar to an S R flip flop. First this symbolic notation exactly same; so I can show it either positive edge triggered like this negative edge triggered like this. This is single input D, this state table also will look like this if the clock there is no leading edge positive edge triggered; no change if there is a clock edge.

So, whatever is there in D that same value gets copied to the output. So, here you do not have to do any calculation; characters equation is very simple. Q t plus 1 is nothing, but whatever has been applied to D at that point in time ok. So, whenever the clock edge comes at that point in time whatever the value of D was; that will go to the output.

So, you see just I am telling you one thing; suppose this is your clock and your D input was 1 and your Q was 0. So, whenever the clock comes then only Q will become 1. Q will not become 1 means immediately as soon as you make D 1 not like that; it will wait for the clock to come only then this change will occur alright.

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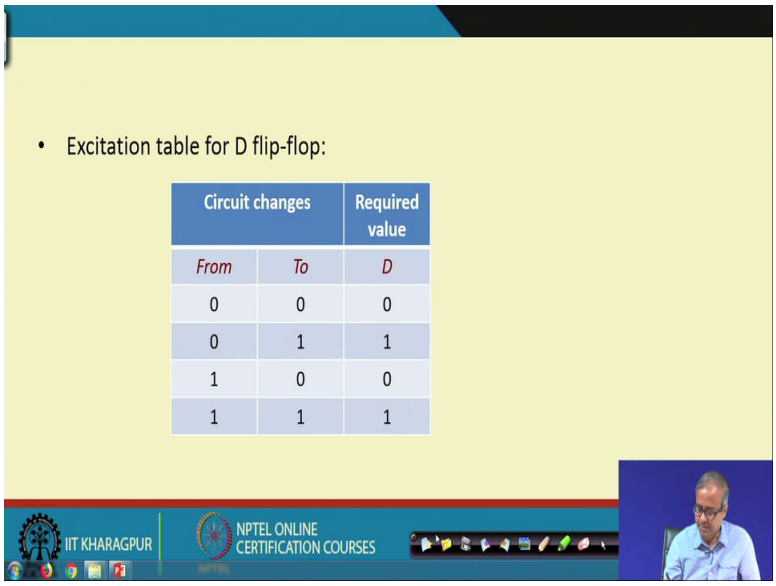

So, in a similar way we can construct the excitation table for the D flip flop; say for D flip flop if you want to change from 0 to 0, I have to apply 0 in the D input that 0 will go in; 0 to 1 I have to apply 1, 1 to 0 have to apply 0 1 to 1 I have to apply 1.

So; that means, whatever I want to change to; I have to apply that same value in D irrespect to what it was earlier right this same thing I have to apply.

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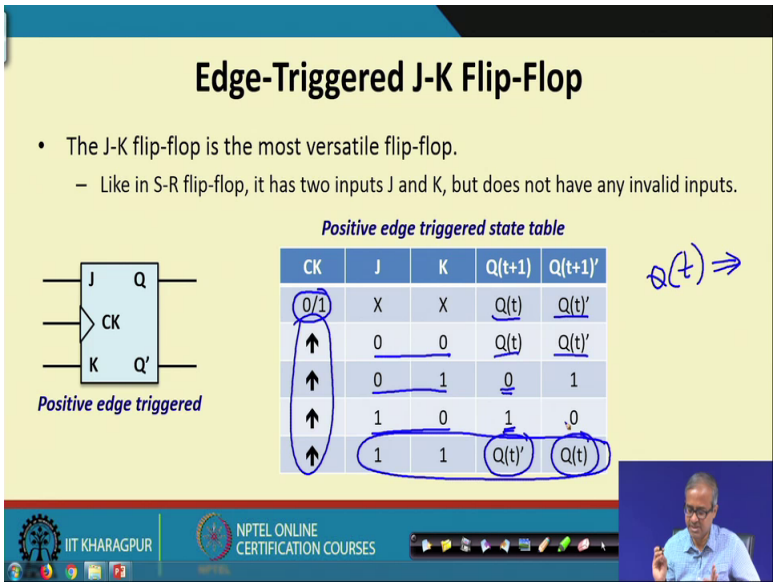

Now, let us talk about another kind of a flip flop called J-K flip flop. J-K is the most versatile of the flip flop versatile means it is more powerful than the other kind of flip

flop, you can implement some functions with the other flip flops may not be able to do it directly.

Let us see what it looks like and how it works first thing is that there are 2 inputs J and K just like S R flip flop. There is a clock here I am showing only the positive edge version negative edge will be similar there will be a bubble here that will be negative edge triggered. Now, let us see how a J-K flip flop looks like.

Now in the state table you see we have shown it in a slightly different way instead of just writing Q and Q bar; we have written Q t plus 1 and Q t plus 1 bar because we need to keep track of the time. Here as per our notation Q t will indicate, the value of the output at t th time unit; that means, after the t th clock pulse has come.

And Q t plus 1 will be the output after t plus 1 th clock pulse has come; that means, it keeps track of the time. So, I am saying what will be the value of Q t plus 1 and Q t plus 1 prime depending on at the previous state what Q t was? Q t was the previous history. So, if there is no edge it will remain at Q t and Q t bar; no change. And when there is an edge 0 0 means no change again Q t and Q t bar; 0 1 exactly like an S-R flip flop 1 0.

So, far it is exactly like an S-R flip flop the only change is the last row. For a S-R flip flop the 1 1 combination was supposed to be invalid, but for a J-K flip flop we are not saying it is invalid. If J-K is 1 1 the output value will be complemented; that means, 1 will become 0 0 will become 1 that is the difference. So, when the inputs are 1 1; Q t plus 1 will be same as Q t bar, Q t plus 1 bar will be same as Q t; that means, it will be the K naught of the previous state; this is the only change.

This is why we say that J-K is the most versatile and most general kind of flip flop because it is S-R flip flop plus this additional functionality which S R flip flop does not has. Talking about the characteristic equation you see again.

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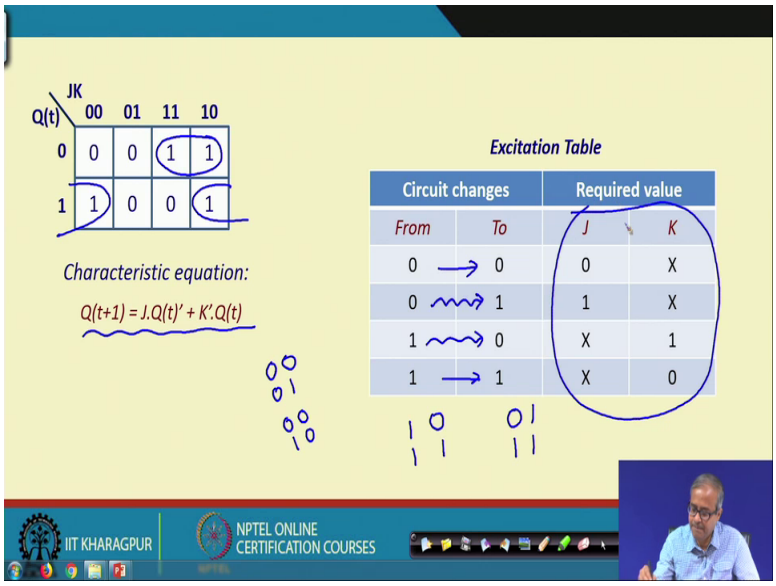

So, here we are again showing JK and Q t; if JK is 0 0 no change; that means, if your 0 will remains 0, if it is 1 it will be remain 1. 0 1 means it will be 0; set to 0 1 0 means it will be set to 1 and 1 1 means naught, if the output was 0 it will become 1 if the output has 1 it will become 0. So, if you want to minimize this Karnaugh map; the Q S will be 1 will be this other Q will be this. So, if you just write down the minimize expression this will be the characteristic equation J Q t bar, K bar Q t.

This will correspond to this second term this one J Q t bar is this Q and the other Q S K bar Q t. And regarding excitation table; suppose we want to go from 0 to 0 for a J K flip flop you can apply either 0 0 or 0 1 just like an S R flip flop. So, it will be 0 do not care, 0 do not care if you want to go from 1 to 1 this is also S R flip flop you apply either 0 0 or 1 0.

That means do not care, 0 do not care 0 but the differences are here if we want to go from 0 to 1, then you either apply 1 0 which will make it definitely or you apply 1 1 which will complement the output was 0 it will change it. So, it is 1 do not care 1 do not care and 1 to 0 will also be different; 1 to 0 you either apply 0 1 or you complement 1 1 do not care 1. So, these are the excitation values for J K flip flop.

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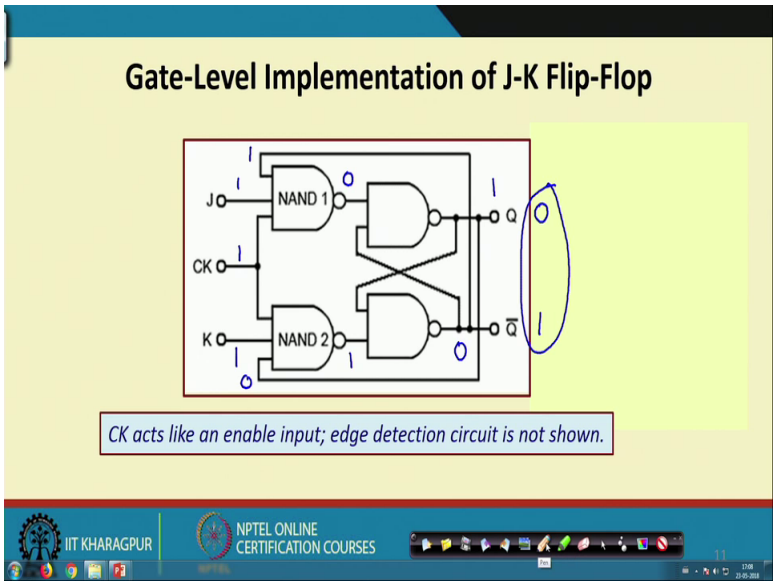

Now, let us look at the gate level implementations of a J K flip flop. Here I am just showing this diagram where we have referred to has here clock, but we have not shown any edge detection circuit we shall discuss it later, but assume that somehow some edge detection mechanism is there. So, when ever clock edge comes then only here some 1 comes.

Now just let us see how it works let us say, but I have applied J 1 and K 1 and here also it is clock works like an enable; this also is 1. And let us say the output this Q was 0 and Q bar was 1; you see there is a feedback from Q bar there is a feedback to here. So, Q bar was 1; so this input is 1 Q is 0 there is a feedback this is 0. So, 1 and 1 and 1; this NAND output will be 0 and 1 1 0 this will be 1.

So, this cross coupled NAND gate this 0 will make this 1 and this 1 1 will make this 0. So, you see whatever it was; it gets complemented J 1, K 1 should complement it. So, I will leave it as excess fall to verify that for the other combinations this J K flip flop state table also gets satisfied ok; this is the gate level implementation.

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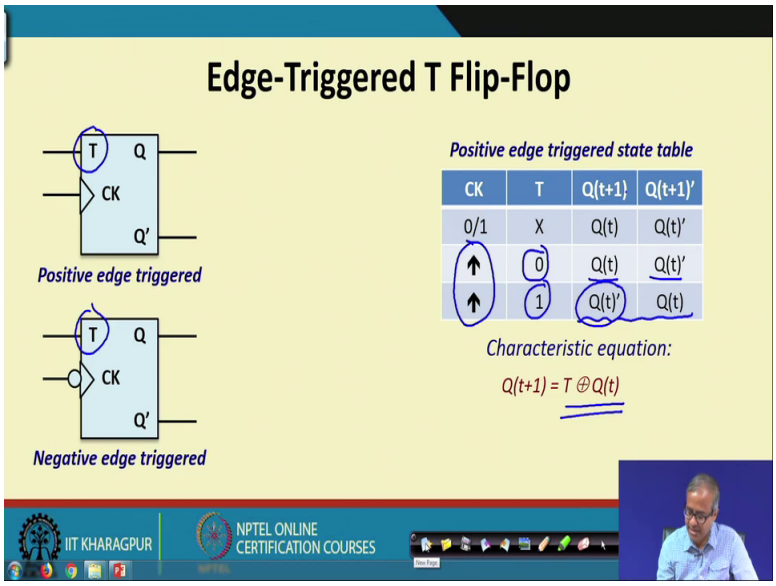

Now, there is another kind of a flip flop which you can say is a special case of a J K flip flop; this is called a toggle or a T flip flop. So, a T flip flop has a single input T as this diagram shows there is a single input T this S this is the positive edge portion negative edge portion and what this T flip flop says; if T is 0 there will be no change.

If T is 1 the output will toggle; toggle means it will be it will get complemented naught, no set reset kind of thing only toggle. So, this is equivalent to that J equal to 1 K equal to 1 combination of a J K flip flop the output will toggle just that. So, you see the state table; so, whenever there is a clock active edge, you see if T is 0; no change. If T is 1 there is a toggle Q t plus 1 becomes Q t bar; Q t plus 1 bar becomes Q t.

And characteristic equation you can read like this, you can write straight way like this because you see anything X or with see if T is 0; 0 x or Q t is this Q t itself same. And if T is 1; 1 X or something is naught; so you are getting naught this is the characteristic equation of a T flip flop T type flip flop.

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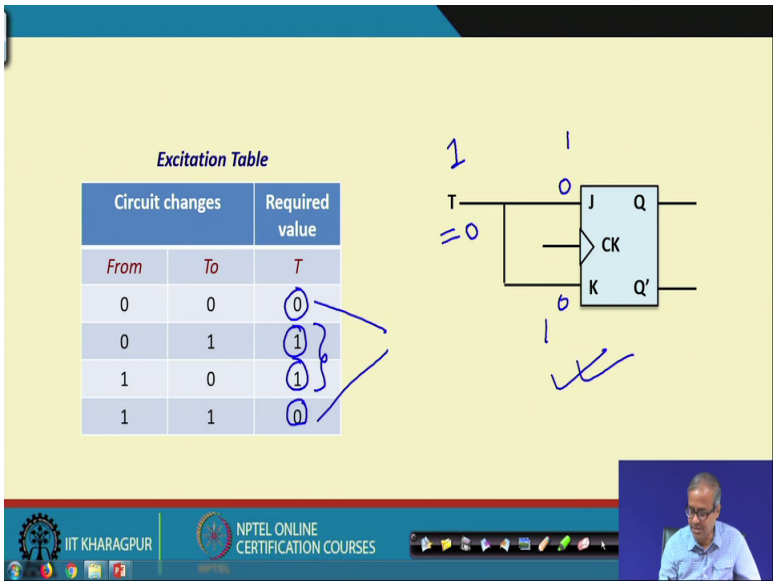

And talking about the excitation table whenever you want to go from 0 to 0, there is no change no toggle.

So, T is 0 0 to 1 there is the toggle there is a change you just set T equal to 1. 1 to 0 toggle set T equal to 1, 1 to 1 no change set T equal to 0. So, whenever there is a change you set T equal to 1, when there is no change; you set T equal to 0. And just as I said T is the special case of a J K flip flop if we simply tie J and K together and you call it T you can implement a T flip flop. Because if we apply T equal to 0 this is equivalent to J 0 K 0 which means no change; if we apply T equal to 1 which means J 1, K 1 which means toggle output that is what T flip flop is right.

So, with this we come to the end of this lecture. Now in the next lecture we will looking at some other aspects of flip flop design. And in particular we did not mention one thing that how this edge triggering is implemented. We I have said that the flip flop will work whenever the edge of the clock comes, but there must be some circuit which is detecting the edge and activating the flip flop during that time right. So, we shall be seeing that in the next lecture.

Thank you.