Architectural Design of Digital Integrated Circuits

Prof. Indranil Hatai
School of VLSI Technology
Indian Institute of Engineering Science and Technology, Shibpur, Howrah

Lecture – 13
Algorithm to Efficient Architecture Mapping (Contd.)

So, welcome back to the course on Architectural Design of ICS. So, in the last few classes we are seeing Algorithm to Efficient Architecture Mapping techniques, there are several tricks and tips for; that means, techniques for designing the efficient architecture of from different one particular algorithm that can be implemented in different way, in considering speed or area as a measure constraint.

So, we have seen few of the examples, how we can design them considering different aspects ok. So, in a last class we have seen that one architecture of y equal. So, suppose I have to implement one function that is y equals to 2 to the power x plus 1. So, at the time what will be its architecture, if the that initially we have started from designing this y equals to 2 to the power x function, then we have just started designing another function, which we will be implemented from that particular point that is y equals to 2 to the power x plus 1.

And in the last class I have just ended with that ok. So, we have seen that I can design 2 to the power x plus 1. So, from that particular point can I design 2 to the power x plus 2, 2 to the power x plus 4, 2 to the power x plus 8. So, if I can design then how can I design, what will be the techniques or tips for designing them ok.

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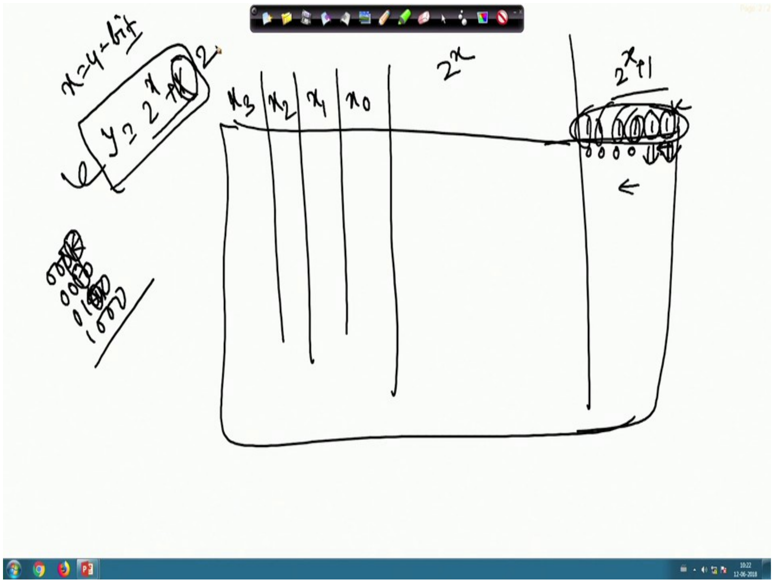

So, we will see that so, in the last class what we have seen. So, we have seen y equals to 2 to the power x plus 1, in the last class right. So, whenever we have designed this 2 to the power x plus 1 at the time, how we have design. So, initially what we do so, considering x equals to of 4 bit ok.

So, how we have design so, initially we have plotted like this x 3, x 2, x 1 and x 0 and for that what will be this 2 to the power x value and, then we have to find out this 2 to the power x plus 1. And after getting this operation table of this particular circuit, then we have find out the corresponding each of these expression that means, each of this bit positions what will be the logical expression for that.

So, after finding this logical expression for each of these bits, then we have just map that logical expression into architecture. So, whenever we have design this 2 to the power x plus 1 so, at the time what we have seen, we have seen that there is only change in this two particular position, rest of the positions are remain same. That means, as I am adding only one at the LSB position so, that is why it is effecting this LSB bits of this 2 to the power x and the corresponding bit, which is just at the same to this LSB that means, next to the LSB, why because these carry is basically effecting the corresponding bit.

And then why it is not traversing to the other MSB side, because in 2 to the power x how we are getting it is we are getting the that means, output like 1, 0 then 4, then 8 something like this.

So, as this only one of this bit is 1 rest of the bit is 0 so, that is why it is not effecting the corresponding other bit; that means, the carry is basically diminishes at these particular second; that means, at the same to this LSB position, it is not traversing or it is not effecting the other bits that, we have seen in the last class.

Now, consider instead of this 2 to the power x plus 1 ok, now here I need 2 to the power x plus 2 so, at that time what it will be the or how I can implement the circuit that is 2 to the power x plus 2, or where will be the change or, what I need to change so, that this circuit implement 2 to the power x plus 2 function.

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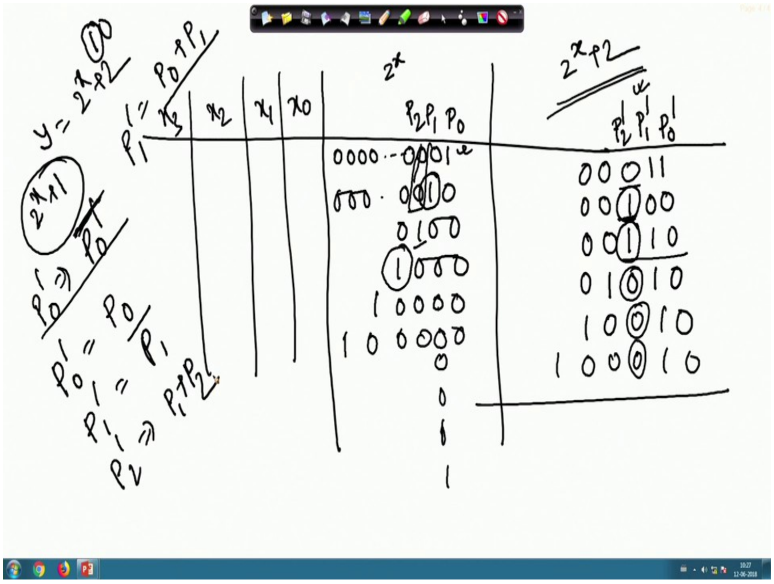

So, let us consider these things, I have to implement 2 to the power x plus 2 ok. So, for that again what I have to do so, we know that we know that this is x 3, x 2, x 1 and x 0 ok. So, for 2 to the power x it will be something like this, 1 then this consider this, 0 1, then 0 0 1 0 2 then, 4 then, 8 then, 16 something like this I will get for 2 to the power x, now what I need to do that is 2 to the power x plus 2.

So, 2 to the power x plus two if I want to design so, at the time if I just added with 2 so, at the time what it will be, it will be like 1 1, it will be it will became 3, then it will became 2 to the power x 1, then 2 which 2, if I just add then it will became 4, after that it will became this 4 will became what 6, 4 plus 2 that is 6. So, 10 will became 12 sorry this is 8, 8 will became 10, then 16, 16 will became 18 so; that means, this.

So, if you see; that means, whenever I am getting there; that means, it is effecting whenever I am adding these 2 so, at the time up to this it is basically changing its value. So, after that for whenever I am ah; that means, adding with 8, then 16, then if I just added with 32 ok.

So, so; that means, at the time these bits are not effected by the corresponding addition of this 2 so, if I just now if I just want to conclude, or if I just want to ah; that means, observing the trends of changing of this position. So, at the time we find that here, this corresponding suppose if this is P 0, P 0 remain same for 2 to the power x plus 2 so, here if this is P 0 dashed that is same as P 0 then if you just follow P 1 dashed if this is P 1.

So, if you see that this position is was 0, now this became 0, this is 0, now it becomes 1, each of these bit position now we will became 1. So, in the earlier case whenever we are doing 2 to the power x plus 1 at the time what we have seen that P 0 dash position, that was changing sorry yes sorry this is not this that was P 0 bar. So, now, here also you see this P 1 dashed that is nothing, but just inversion of this particular position, there which is P 1 so; that means, now for this particular 2 to the power x plus 2, the P 0 dashed for will be same as P 0 and P 1 dashed that will be P 1 bar here.

Now, if I consider this P 2 dashed so, how it is changing from 2 to the power x so, here also you see the same trend what we have followed, or what we have observed in the 2 to the power x plus 1 case. So, in the 2 to the power x plus 1 case what we have seen, that for this particular bit position if I consider; initially there was 2 0, then the there was one then rest of the bits was 0. So, here you see this is 0 and only this is there is 1 and otherwise it remains same ok. So; that means, this is the carry which is generated for addition of 1 over here ok.

So; that means, now in case of; that means, addition of 1, what we have write; that means, on that particular case P 1 was the bit, where P 1 was the XOR sorry OR with P 0 and P 1; that means, where the carry is being; that means, to at the sent LSB the bit position which is the last two LSB position that were affected by addition of 1 there. So, here whenever I have I am adding 2; that means, 2 means 1 0. So, now, this 1 is basically effecting at the very next it is starting from this P 1 position ok. So, otherwise the its remain same so; that means, at that this case P 2 dash can be written as P 1 plus P 2 ok.

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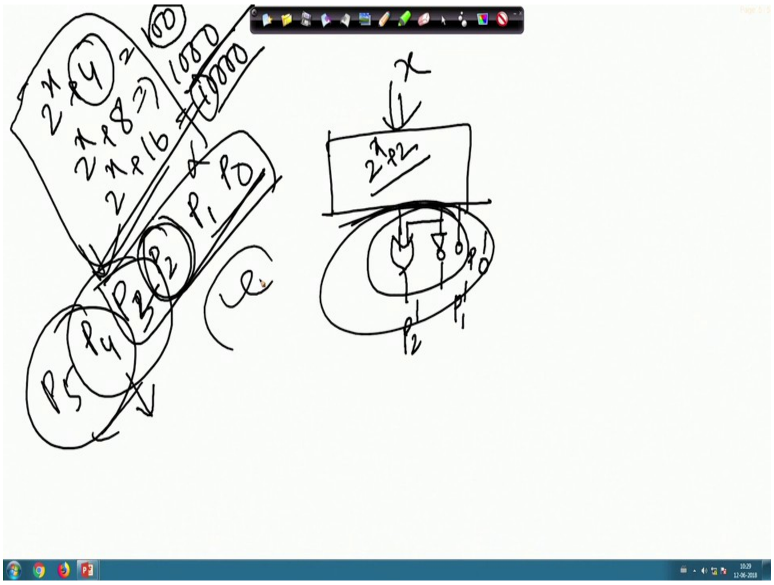

So, now if I just draw the circuit so, at the time it will be something like, if I put x over here so, P 0 is nothing, but P 0 here and here this is P 1 dashed and, if I just put 1 OR gate over here. So, this is new P 2 dashed and these circuit is basically nothing, but 2 to the power x plus 2 ok. So, now, next if I just ask you to design 2 to the power x plus 4, or 2 to the power x plus 8, or 2 to the power x plus 16 something like that, if I want to ask for; that means, if I just ask you to design these, then what you can do that means, 4 means it will start effecting from the third bit P 1 and P 0 so, 4 means this is 1 0 0.

So, as I am adding 0 0 to this particular bit position; that means, this two will not be effected it will start effecting P 2 and P 3. So, for 8 so; that means, this 2 this 3 bit position will not be effected, it will sorry this is P 3 then P 3 and P 4 will be effected, if I added with 60 sorry if I added with 16 so, at the time up to P 3, it will not touch it will start effecting P 4 and P 5 something like this it will start effecting.

At which position I will just try to add this so, this particular circuit will continue from that particular point, or for form that particular corresponding bit positions ok. So, now, I can design any circuit something like, this which is 2 to the power x plus 2, 1, 2, 4, 8, 16, 32 any values I can do, or I can implement by following the same trend ok. So, this is the design procedure of 2 to the power x plus 1, or 2 to the power x plus power of 2 value. It is not that if I want to add any other value so, at that time the design technique will be different

It is only applicable for if the value, which I am I want to add that is in the power of 2 ok. So, if we want to add some different value so, at the time using this method, or whatever technique, I have followed to find out the logical expression using that you have to find out and, then you have to draw the corresponding architecture for that ok.

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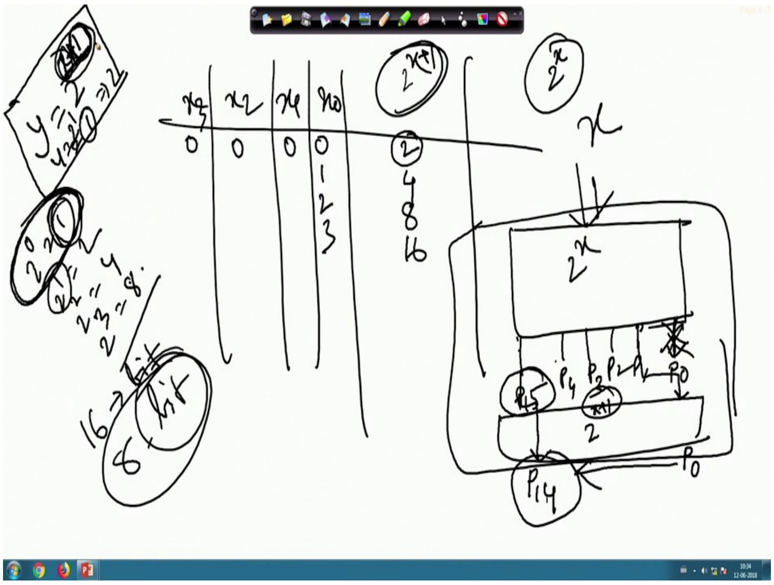

Now, next if I want to implement another function which is let us consider another circuit, which is y equals to 2 to the power x plus 1 ok. So, y equals to 2 to the power x plus 1 if I want to design so, at the time how it will look like. So, here you see 2 to the power x plus 1 means so, this x value is basically this is x 3, x 2, x 1 and x 0 and if this is 2 to the power x plus 1 let us consider ok.

So, this value is basically started from 0, but here instead of that as I am adding at along with this x plus 1; that means, it will start from 1. So, initially what was what we are getting 2 to the power x going we are finding this 2 to the power x, at the time 0 means this was starting from 1, because 2 to the power 0 means there is 1, but here what we are doing in the next what was their y equals to 2 to the power 1 that is equals to 2 so, 2 to the power 1, then 2 then 2 to the power 2, then 4, then 2 to the power 3 that is 8 something like this, it was following.

But so, as I am adding plus 1 1 over here so; that means, it will not this 2 to the power 0 that we will not get ok, it will start from 2 to the power 1 so; that means, here we will get 2, then we will get 4 for 1, we will get 4 for 2, we will get 8 for 3 we will get 16 so; that means, now from this 2 to the power x block how can we design this 2 to the power x plus 1.

If I just draw this particular circuit so, if this is x so, at the time what it will be that means, for this initially there was this 1 so, that position if this is P 0, then the P 1, then P 2, then P 3, sorry P 3, P 4 something like this, if this was up to 15 ok. So, in this case this P 0 will not be connected so, P 1 will be connected which will be P 0 of this particular block and, P 15 that will be P 14 ok.

So that means, now I can as I am considering because here whenever for the final bit, it will be as I have just increase the power of 2. So, if I am considering fixed of 16 bit or 8 bit so, at the time I cannot hold the values of the maximum of x. So, that is why you though for 2 to the power x, I can hold the value of 2 to the P 15, but 2 to the power x plus 1 I cannot hold the value within that bit position, or within that word length.

So, that is why up to P P 14, I can consider and this will be the total block diagram of 2 to the power x plus 1 ok.

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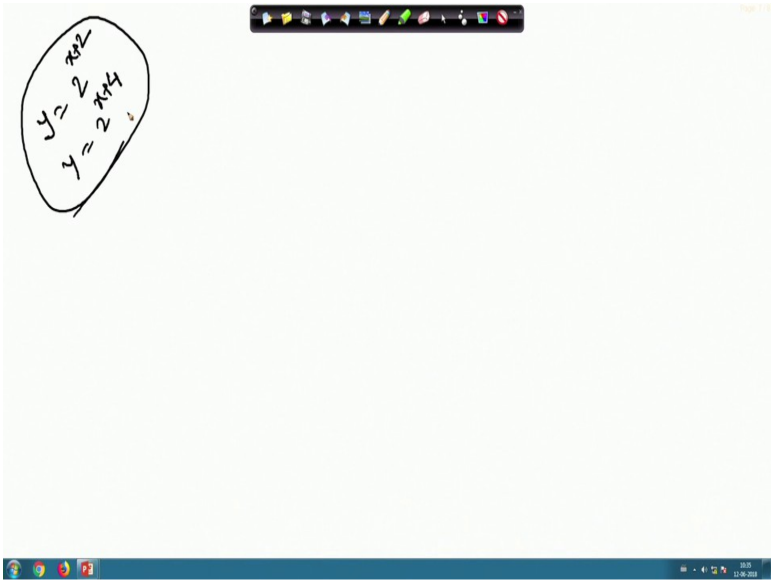

So, now, the same thing if I just using the same that means, now if I consider this y, suppose I have to add 2 to the power x plus 2, y equals to 2 to the power x plus 4, then how it will be how can I design those circuit that you can also try from this particular point ok. So, that I am not discussing over here ok. So, if you have doubt or how we can design, that we will that we will discuss it in the forum or we will discuss it in the offline ok.

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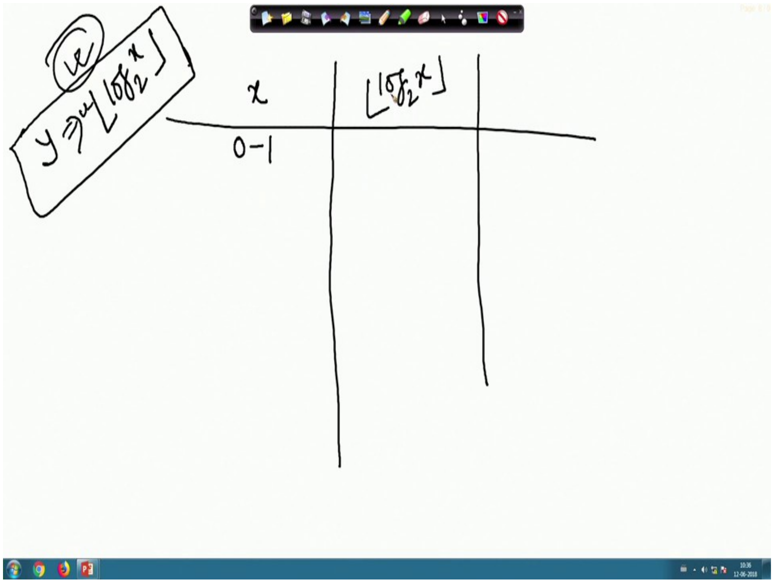

So, then next suppose I want to design a circuit, y equals to ceiling of log 2 base x ok, suppose this function I need to implement. So, at the time if you just see; that means, I need to do this ceiling, then I need to find out this log of this. So, how efficiently I can implement this particular function, or what will be the architecture for this log 2 base ceiling of this.

So, now, we will see the corresponding circuit for that ok. Now, consider this x value, now for 0 to 1 what will be the corresponding log 2 x values, for 0 to 1 as we are considering this particular point so, at the time ok.

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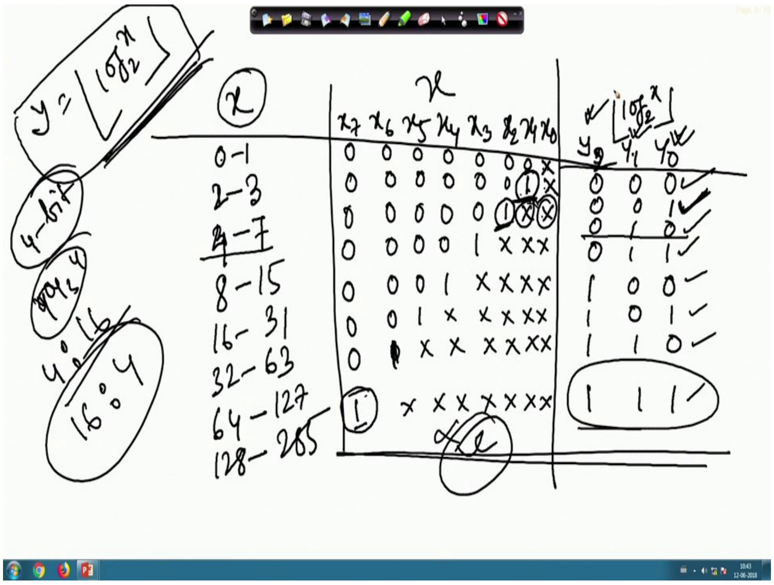

x	x_7	x_6	x_5	x_4	x_3	x_2	x_1	x_0	y_2	y_1	y_0
0-1	0	0	0	0	0	0	0	x	0	0	0 ✓
2-3	0	0	0	0	0	0	1	x	0	0	1 ✓
4-7	0	0	0	0	0	1	x	x	0	1	0 ✓
8-15	0	0	0	0	1	x	x	x	0	1	1 ✓
16-31	0	0	0	1	x	x	x	x	1	0	0 ✓
32-63	0	0	1	x	x	x	x	x	1	0	1 ✓
64-127	0	1	x	x	x	x	x	x	1	1	0 ✓
128-285	1	x	x	x	x	x	x	x	1	1	1 ✓

So, not this first let me consider y equals to ceiling of log 2 x, I need to implement right. So, if I just draw something like this x the range of x will be 0 to 1, then 1 2 for 1 2 3, then sorry then this is 2 to 3, then 4 to 7, then 8 to 15, then 16 to 31, then 32 to 63, then 64 to 127, then 128 to 255 ok, if I am considering only the x bit x of 8 bit

So, now if I just consider this x so; that means x 7, x 6, x 5, x 4, x 3, x 2, x 1 and x 0. So, if I just write it something like this for any value of that is 0 or 1 that may be 0 to 1 range means that will be 0 or 1 ok. So, for that what will be the. So, in this case sorry y 2 y 1 y 0 it will be 0 0 0.

So, at this is that means, this is the function 8 b time considering. So, log of 2 base x means that can be covered, within this 3 bit position ok. Then what I need for 1 this; that means, 2 and 3 means this is 1 and, then this position will be 0 for 2 1 for 3 ok. So, whatever is the value of this that does not effect.

If this is 1 so, at the time it will be 1 so, 4 to 7 means the range is basically from 4 0 0 4, then 5, then 6, then 7 I can implement, or I can write this particular range in this manner, then for 8 to 15 range, how can I write this will be 3, in the same manner, if I just write it for, it will be 4 for this say 32 to 63 the range will be something like this, and for that I can write this as the 5 for this sorry. So, it will be 6 and for this particular point, it will be 7 so; that means, for any values within the range of 0 to 1 this ceiling of this log 2 base x, that will be 0, then this will be 1, then this will be 2, then 3, 4, 5, 6, 7.=

As I am considering 8 bit of x so, now, from this particular operation table, can I conclude that what will be the circuit for these particular table. So, if you see this is nothing, but a priority encoder circuit so; that means, priority encoder means in digital encoder how it will be; that means, for 0 0 so, for suppose 4 bit if I just consider ok. So, at the time how it will it will look like; that means, for y 0, y 3, y 2 that means, at the time each of this bit for the each of these bit position how this the corresponding output bit varies. So, that we encode ok.

But here; that means, for a decoder circuit what was that that 4 to 16, in encoder how it will be it will encode from 16 to 4 ok. Now, but here the thing is that whenever this bit position is 1 no matters it depends on the other values ok. So, if I find this bit position as 1 so, obvious at that point this will became 1 So, no matters what is the value of this two particular bit position, if these bit position is x to be position is 1 at the time the corresponding encoded value will be 2.

So, from this particular table you can see so, as this at this particular point x 7 value is 1 no matters what is the value of others these bits, it will corresponds to this triple 1 or 7 ok. So, for this is if I just consider this particular operation table, it is same as the priority encoder circuit ok. So, priority encoder circuit means, now this log 2 base x function, that can be implemented using these particular function that can be implemented using 1 particular priority encoder circuit.

Now, the thing is that now I have to derive, or I have to draw the architecture of priority encoder circuit. So, from this particular table if I just observe and, after observing what is I have to do I have to find out the logical expression for each of this particular bit position, that we have to find out. And after finding out those logical expression those logical expression will be converted, or that will be you in; that means, implemented via logic gates that we will see ok so, that will be see in the next class.

Thank you for today’s class.