Architectural Design of Digital Integrated Circuits
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Lecture - 45
Issues in Timing Closure

So, welcome back to the course on Architecture Design of ICs. So, in the last class we have seen the CORDIC architecture. So, today we will discuss about actually few other topic are left, which is again we will see that how one FFT or that means, the bigger circuit which is any transform circuit like FFTi ft TEST and then DCT some kind of transforms or some kind of system approach if you could take as an example, at the time how we can design that that we will see.

Apart from that whenever we are talking about this architectural design, mostly we are in the digital design site right. So, at the time we have seen several architecture, we have seen; that means, optimization all these things we have seen, but what we have not considered till now that is the timing issues or the issues which are related in this mostly in the digital design part; so, that we have not seen till now ok.

So, today we will see this Issues in Timing Closure, what are the issues are available or what are the factors which basically degrades the performance of the though; that means, why I am telling that or why you need to that means, know about this factor because whatever optimization you have done right, but still if you are whenever you are making chip at that time, it should be perfectly in the working condition. That means whenever you are; that means, after the chip you have got fabricated your chip should be work properly ok. So, whenever during the test testing face, it should be tested ok.

So, that is why it is not that for any other issue, you have made this optimization for area, power, speed all the things we have made, but if your chip is not working because of other some factors, then whatever optimization you have done for your designing your system that is not at all meaning anything. So, that is why whenever your designing, at that time some of the issues also you have to be keep your mind. So, today we will discuss actually not in details actually I can describe because itself this timing closure itself takes so, much of time or so, much of that means, effort to learn this particular procedure, but I can give you some of the overview or some of the basics what you have to know. But if you want to learn or if you want to more then you have to search in the

that means, internet for the latest up gradation in this particular direction or if you are interested then also please you also kind let me know that I am interested then please I will that means, try to help you whatever is my limit. So, today we will start or we will see the issues which are related to digital design.

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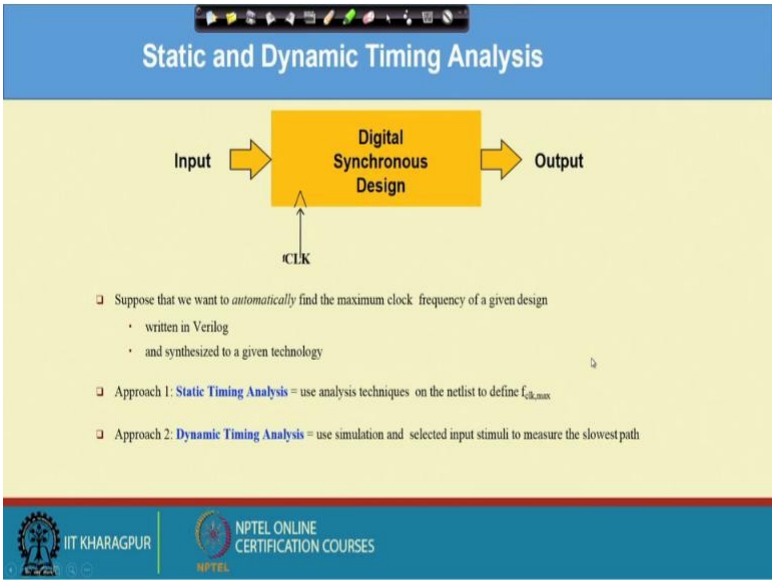

So, in digital synchronous circuit, actually in digital design there you might find two type of circuit. One is this synchronous circuit another one is asynchronous circuit. Why I am telling? Actually apart from that actually that is not the case. In digital design, it is the starting that there are two type of circuit; one is this combinatorial circuit another one is sequential circuit. In sequential circuit you might find two type of circuit that is one is synchronous circuit another one is asynchronous circuit.

So, what is synchronous circuit? Synchronous circuit means if the system there will be a one single clock ok; that means, all the; that means, the corresponding sequential elements which are present on that particular design, both will be clock by the same clock ok. So, that means, depending on the same clock all the; that means, sequential element they will change their state it is not that, but in case of asynchronous there you might find more than one clock.

That means, one clock that may be run at f 1 megahertz or f 1 hertz or f 1 gigahertz and another clock in different frequency, which may be f 2 or it may be more than that.

So that means, there is the operation of the sequential element that is not synchronize as in case of asynchronies circuit design. So, when actually both has some of the advantage ok. So, where to use synchronous design, where to you use asynchronous design again

itself it is a that means, that means, technical knowledge you know. So, but I will give brief idea where you can use this synchronous design and where you can use asynchronous design.

So, whenever we are doing this timing analysis, timing analysis means why I required to do this timing analysis? Because to meet that means, whatever to find out this f clock. So, in this particular system you see this f clock is the clock basically which is connected to each of the synchronous element which is present with in this digital synchronous design right.

So, what will be the maximum achievable clock frequency? For this particular design, so that you only able to know by doing this timing analysis. So that means, suppose if you see that this if you just have noticed that, suppose one that whenever we are talking about the processor let us say Intel Pentium 4 that may be a run at let us 2.8 gigahertz. So, 2.8 gigahertz has the clock frequency where that processor can run. So, why it is needed? Because depending on that clock frequency, now higher the clock frequency; that means, the corresponding computation time which is related to this your instruction fetching or your instruction to be executed on the CPU or in the processor, that becomes lesser.

So that means, you can do the processing or you can do the computation in the processor, in a faster way if the clock frequency is on the higher site. So, that is why our mostly or our; that means, primary intension always is to maximize this clock frequency ok. And whenever we have to calculate these clock frequency, we have to do this timing analysis; how you can do? Timing analysis can be done in two ways; one is static timing analysis another one is dynamic timing analysis. So, what is static timing analysis? Static timing analysis is it uses this analysis techniques on the net list to defined this f clock max.

But in the dynamic that means, here whatever is the corresponding critical path; critical path means, from the input to the output which path it is taking the maximum time that is the critical path for your system. So, that particular path how much time it is taking, so, 1 by that time is basically your frequency or the maximum achievable frequency. Then you can ask that if that is that means, if I make it lesser; that means, if the time period suppose that critical path requires the time of let us say 10 nano second, but if I make that clock frequency of 9 nano second period, so, at that time what will happen?

So, at that time what will happen, before the execution of that path your data will be changed that the input side. Though your operation is still not; that means that is yet to be

completed because it is required 10 nano second, but at the input what you are doing? You are changing the input at 9 nano second or before that 10 nano second. So, at the time what will happen? Though the operation is still yet; that means, that is not completed, but your changing the data means it will take the next data for the computation again so; that means, at the output you will not get the proper result.

So, that is why this actually that is not all for all the things, it is not the case that the critical path; critical path basically corresponds to this considering the gate delays only gate delays and net delays. So, if you considered this get delays net delays for that particular path. So, it is not that only because of those factors, the critical path is 10 nano second it may be more than 10 nano second. So, why there is this more than their 10 nano second that we will see ok. But in dynamic timing approach this dynamic analysis approach what we do? We use this simulation base timing analysis.

Simulation timing analysis means we gives some of the; that means, selected input stimuli. Means, some of that means, what I said that for static timing analysis the input is not defined; that means, the combination of what will be the corresponding combination of input that we have not consider.

This is here we do the rough estimation based on this the available information from the gate delays from the net delays, which is depending on the totally on the library it; that means, the from the library I will get those information and based on that I can calculate this what will be the timing requirement for that. But in dynamic timing analysis what we do? We basically gives a selected set of stimuli; selected set of inputs of the combination of inputs to check what will be for that particular for those particular combination, what will be the timing requirement for this particular circuit ok.

So; that means, what and why I need this, this dynamic timing analysis because in during the testing how you can do the testing during the testing face what we will do? We will give some of the test vector to the circuit for properly whether that is properly working or not. So, during that time whenever we are that means, giving the; that means, in the real time whenever we are giving the input. So, at the time your circuit may fail. So, that is why from the beginning if we check by; that means, providing some of the input combination to the design, and then if you do the timing analysis. So, at the time the probability of that failure that becomes reduced or my intention is to reduce those; that means, the probability of that failure.

So, that is why we do timing this dynamic timing analysis. So, this is the two condition, where we use study timing analysis and where you used dynamic timing analysis, but for the particular; that means, for any system design, which is has to be like in the; that means, chip format or if it is has to be run on the real time. So, at that time both the timing analysis we have to do whether that is static timing analysis and that is the timing analysis.

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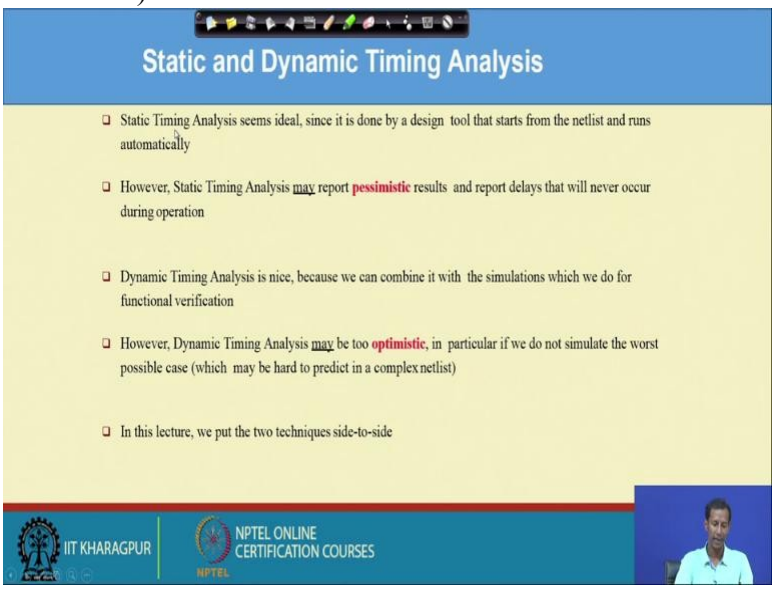

So, here you see this static timing analysis since ideal since it is done by a design tool that starts from the net list and run automatically means what? What I said that based on the library information about the get delay and the net delays, the tool itself it calculates the corresponding timing requirement for that the critical path or for that the system design. However, this static timing analysis may report pessimistic results, and report delays that we will never occur during pre operation.

So; that means, here whatever results we will get that is one rough estimation of the; that means, this circuit; that means, the delay the information. So, that is why this report may be that is why it is says that the report may be pessimistic results. But in case of dynamic timing analysis, this is; that means dynamic timing analysis when we do or why we do? Basically to check what will be the timing requirement whenever we will tested in the real time environment. So, that is why this dynamic timing analysis is very much important, because we can combine it with the simulation which we do for the functional verification. Not only for the functional verification during the testing whatever test vector we will give so, those stimuli we can put now; that means, at the stimulation itself

now we can put, and then we can check the timing analysis of the timing requirement for that particular design.

However, this dynamic timing analysis maybe two optimistic, and in particular if we do not simulate the worst possible case so; that means, here when this will be; that means, too much optimistic, because it is not the case that all the time we can provide all the test vectors and we do dynamic timing analysis why? Because if the size of the test vectors; suppose for a 64 bit added design. So, for a 64 bit added design. So, what will be the number of test vectors? That is 2 to the power 64.

So, 2 to the 2 to the per 64 number of test vectors application of that generation and then application then do the simulation, it will take too much of time as well as too much of wafer. So, on that particular case actually those who are working on the testing area. So, they at the time see that what will be the optimize test vector to produce or to; that means, testify the circuit whether that is working properly or not. That means, based on the reduce set of or optimization is done on the test vector itself so, that the number of the vectors became lesser, but still I can check all; that means, the possible functionality working or the proper functionality of the design.

So, what will be that number what will be that optimum number? Those who are working on the testing area. So, they basically work on that; what will be the minimum number of test vectors and what will be the combination of the test vectors ok. So, and then for that your might system will not failure. So, those type of things do who; that means, who the people working on the testing and the verification area ok. But this two particular case we use for any VLSI chip design ok.

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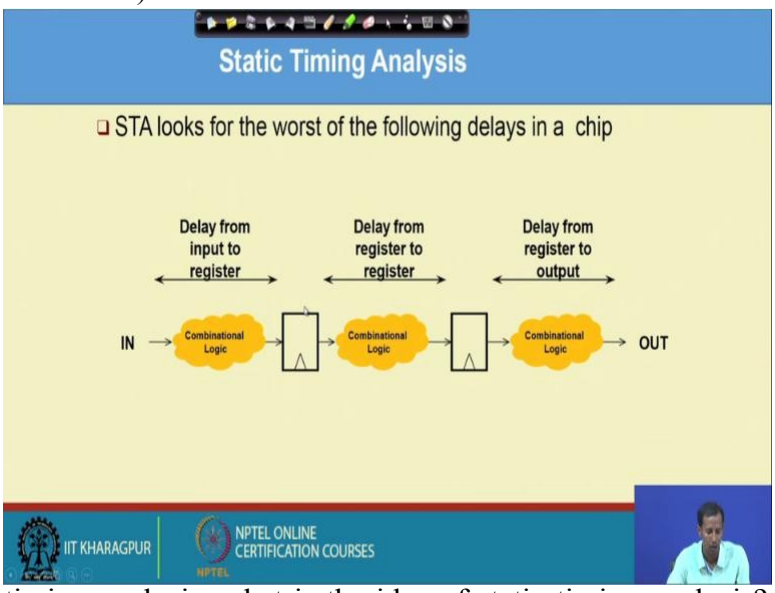

So, this static timing analysis, what is the idea of static timing analysis? Suppose I am having the input to the output whatever systems that is the block diagram representation of that system, we have seen in the earlier slide.

Now, consider one particular that inside of that system design ok. So, inside of the system if there are this two or the register or the sequential elements, and there being connected inside between these combinational logic three combinational logic; this is c 1 this is c 2 this is c 3. So, then this is the application of the input. So, this is delay from input to the register, which is happening because of this combinational logic. Then this delay from register to register and considering the corresponding factors or the corresponding logic which is available in combinatorial logic and delays from register to the output, which is again passing through another combinatorial logic.

Actually why this three are different and when this three will be much? If this registers are not there at the time, this total delay will be this c 1 the delay of this c 1 delay of c 2 plus delay of c 3. But as I have put this register sign between; that means, what I am this data dependency has became now clock dependent. Clock dependent means though there is a change actually in combinatorial circuit what happen? If I change any of the input the output automatically tries to change or the corresponding logic element they starts their operation. But in sequential element unless and until your finding the age; that means, whatever logic whether if it is age trigger, unless and until it is finding the age it will not start it operation.

So; that means, now what is depended on the clock, it is not depended on the data, but in sequence in combinatorial circuit if you change any signal. So, automatically that will reflect at the output. But in sequential element, if you find the age then it will go for checking the whatever what is the value present at the data. So, based on their data, now the output will changed. So, that is why now this is which is getting the higher priority? The clock 1.

So, that is why this is clock dependent not data dependent sequential element got it and that is basically for that particular property, if we put the registers in between. So, that became this at the time this c 1 c 2 c 3 that became individual to each other. So, now, we have to calculate the timing analysis for this.

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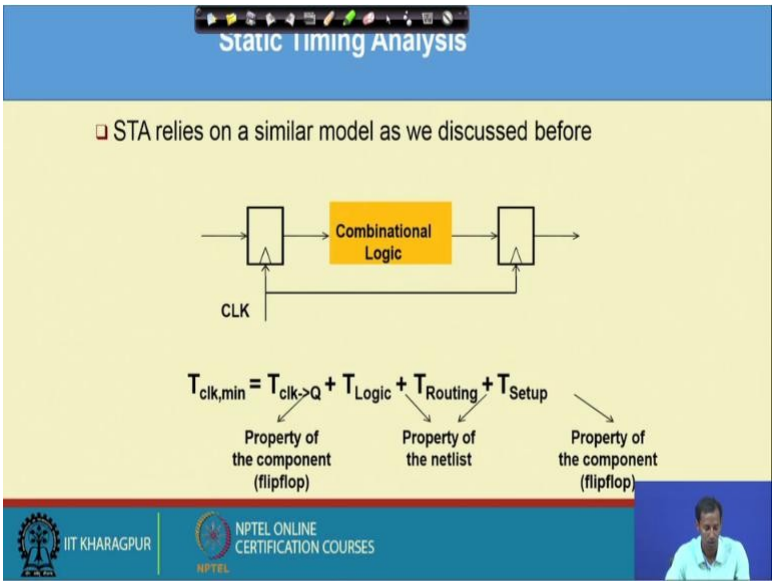

So, this STA, how we can calculate? So that means, whenever there is. So, there are input to the registers, then register to the register, then register to the output.

So, here you see inside of this register to register whatever is the logic. So, that will be consider as the timing requirement, minimum timing requirement for the corresponding clock. So, then what will be the corresponding value for this? The value for this will be T clock to Q; T clock to Q means, what is the meaning of this? This is the delay of the flip flop itself. The delay of the flip flop itself means from clocking to the delay; that means, the output which is the Q it has actually if you just remember the that corresponding that internal structure of flip flop. So, 4 NAND gate are there right.

So; that means, it has to the clock has to pass through two levels of this AND gate sorry NAND get so; that means, it also has some of the flip flop itself has some of the delay for propagating this clock to the output. So, that delay is basically mentioned over here, this is T clock to Q. Then whatever is the this logic delay or the corresponding gate delay for this combinational circuit, that that will be again consider or that again it will come to this part. Then this routing; routing means this is nothing, but the delay which is associated for the; that means, net delay. Net delay means as they are been connected from gate 1 to gate 2 or get 2 to get 3 as the wire is connected. So, because of the wire it also as for the wire there is this rc component.

So, because of that it also takes some time to signal; that means, for the signal to traverse from the one point to the another point or a one node to the another node, through that particular wire. So, those delay will also be consider in this case. So, that is this t routing and then again there is another; that means, delay which also associated for this computation of this minimum clock period, which is this T setup. So, what is setup? What is setup time and what is whole time? I think that is basically mention or that can be recalled in that is mentioned whenever in the basic digital design. But still we will again we will discuss what is the setup time and whole time we will revisit that ok.

But this T setup that is one of the requirement for this particular flip flop why that is required ok? So, that we will see later of this presentation, ok.

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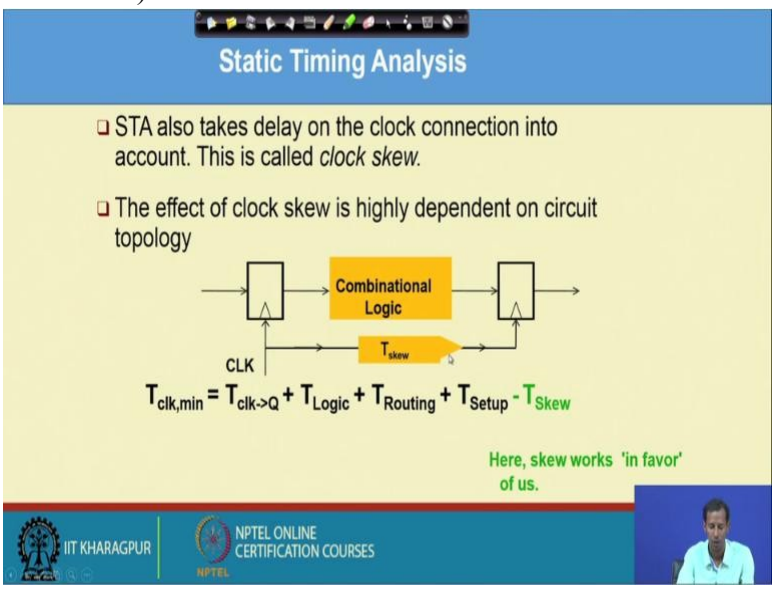

So, after that; that means, all these particulars things will come whenever we are computing this T clock minimum but then again if the clock has some of the skew. So, if

the clock has some of the skew means what is the meaning of clocks skew? In synchronous design it you might have to be very much causes because as it is clock is synchronies to each of the; that means, sequential element. So, at the time so, many factors are basically associated with that, one of them is this clocks skew then not only clocks skew clock jitter is also there.

So, what is clock skew and what is clock jitter that will again we will discuss that during; that means, in the other slides. But here actually for the time being if you consider this clock T; that means, this if this clock has a skew, then and that is in favor; in favor means if from this path to this path this clock skew basically positive. So, at the time this T skew will be minus from the corresponding delay why because here skew works in the favor of us that means favor of the us means favor of the circuit now it works. So, if in favor of circuit it works, as this direction the clock direction is basically traverse in from this side to this side.

So, that is why this clock Q; that means, the data is also flowing in this direction and the clock is also flowing in this direction. So, at the time it is in favor of us, but if the clock is basically supplied on the opposite side of the data suppose in this direction data is supplied, but in the opposite direction if the clock is supplied. So, at the time this skew will not be in favor of that will be against of us or against of us means against of the design. So, at the time this T skew also be will added for finding out. So, this T clock minimum. So, why actually what I said in the beginning that these things or this static timing analysis that has been done through the EDA tool automatically right.

So; that means, whenever this depending on this kind of fact is the EDA tool itself automatically composed what will be corresponding values of T clock minimum consideration each of these factors. Now each of this factors how we will get? This T clock to Q the delay for this flip flop that we will get from the library. How many levels or what are that means, gates are connected for this logic delay? So, that again you can compute from the library or you can get the information from the library itself then what will be the net delay? Again that will be again come from the library itself what is the set of requirement of the for flip flop? Again that comes from the library and then what is this clock skew? Then again that is also you can get from information provided to you only so; that means, all this information is already stored in the library.

So, the tool itself it fetch those data and it computes based on this equation, at its owes to you that this is the minimum clock your requirement for your design ok. So, here you see that STA takes delay on the clock connection into account which is called as this clock skew, the effect of clock skew is highly depended on the circuit apology. That means, how you have what topology you have used for the circuit representation that is a important factor over here for this Q.

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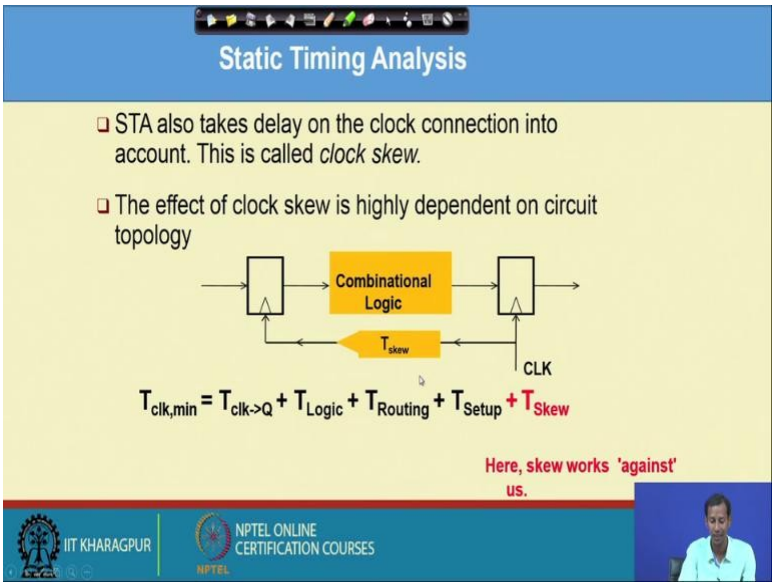

So, if you just see that if I make this; that means, if I supply this clock in the opposite direction of the data. So, at the time clock skew will be added to the; that means, this corresponding equation. So, here you see skew works against us ok.

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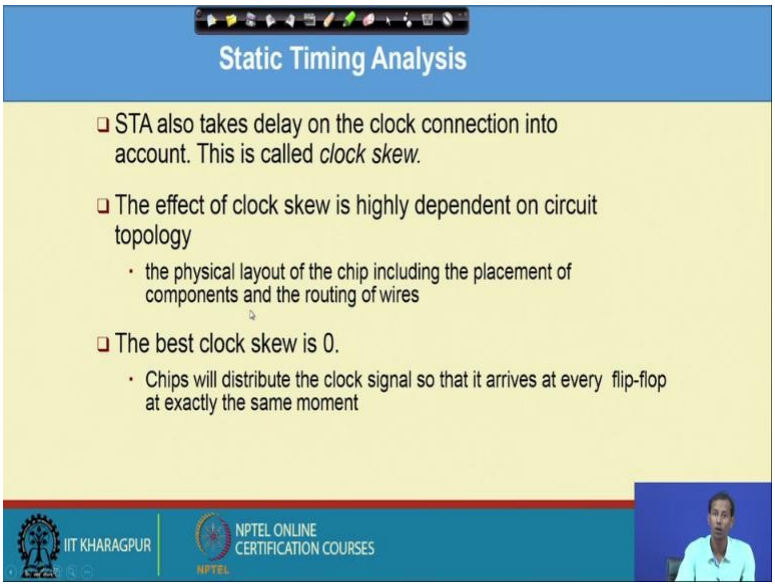

So, the effect actually the effect of clock skew is highly depended on circuit topology, that we have already seen, but the physically out of the chip including the placement of components and the routing of the wires; that means, routing of the wires means how this clock is; that means, in which direction I am supplying the clock, that is dependent for computing this skew. So, if it is against the data; that means, opposite to the data, then it will be added, if it is same direction with the data, so, at the time it will be subtracted. And the best clock skew is 0, chips will distribute the clock signal so, that it arrives at every flip flop at exactly the same movement.

Suppose, in a chip 1000 sequential elements are placed and you have only 1 clock source that; that means, the clock will be connected to 1 pin. So, from that pin now you are supplying to 100 let us say sequential element. From that particular point to reach the maximum or that means, the farthest sequential element present from that particular pin, so, it will take the maximum net delay or the maximum delay for traversing the clock to that particular element.

So; that means, at the time skew will be high enough for that or those that means, that particular path, but what I said? Skew is some time it is better some time it is; that means, not it is worst case condition for our circuit design ok. So, but in case in ideal case if you consider this clock skew is 0 that means, the clock skew is 0 means each of the clock each of the sequential element has been connected to the clock in a uniformly

distributed network; that means, from suppose from the from clock connected to the 1 and clock connected to the furthest element they takes the same amount of time.

If they take the same amount of time, at that time this clocks skew we can consider that as a 0. So, clock skew means is the time gap between the closest one to the furthest one. So, this is the; that means, this concept of this timing analysis, static timing analysis and this clock skew is an important factors not only clock skew then setup time and then this clock to Q then this T logic. So, during optimization what we actually till now what we have done this combinatorial design or the combinatorial logic part. We have done reduction of the timing or reduction of the area on those particular path, but we have not considered the other things which are associated in the whole timing closer calculation. So, that we will be seeing continuation of this particular lectures so.

Thank you for today class, again we will meet on the next class.