Architectural of Design of Digital Integrated Circuits
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Lecture - 46
Issues in Timing Closure (Contd.)

So, welcome back to the course on Architectural Design of ICs. So, in the last class we have seen the Cordic architecture. So, today we will discuss about actually few other topics are left which is again we will see that how one FFT or that means, a bigger circuit which is any transform circuit like a FFT; FFT DST and then DCT; some kind of transforms or some kind of system approach if you could take as an example; at the time how we can design that that we will see.

Apart from that whenever we are talking about this architectural design mostly we are in the digital design side right. So, at that time we have seen several architecture we have seen; that means, optimization all these things we have seen. But what we have not considered till now that is the timing issues or the issues which are related in this mostly in the digital design part. So, that we have not seen till now ok.

So, today we will see this Issues in Timing Closure; what are the issues are available or what are the factors which basically degrades the performance of the though; that means, why I am telling that or why you need to that means, know about this factor because whatever optimization you have done right. But still if your whenever you are making your chip at that time; it should be perfectly in the working condition; that means, whenever your; that means, after the chip have got fabricated your chip should be work properly ok. So, whenever during the testing phase; it should be tested ok.

So, that is why it is not that for any other issues so, you have made this optimization for area, power, speed all the things we have made. But if your chip is not working because of some other factors, then whatever optimization you have done for your designing your system that is not at all meaning anything ok. So, that is why whenever you are designing at that time some of the issues also you have to be give your mind.

So, today we will discuss actually not in details I actually I can describe because itself this timing closure itself it takes so much of time or so much of; that means, effort to

learn this particular procedure, But I can give you some of the over view or some of the basics what you have to know, but if you want to learn or if you want to know more, then you have to search in the; that means, internet for the latest up gradation in this particular direction. Or if you are interested then also please you can also let me know that I am interested; then please I will that means, try to help you whatever is my limit ok.

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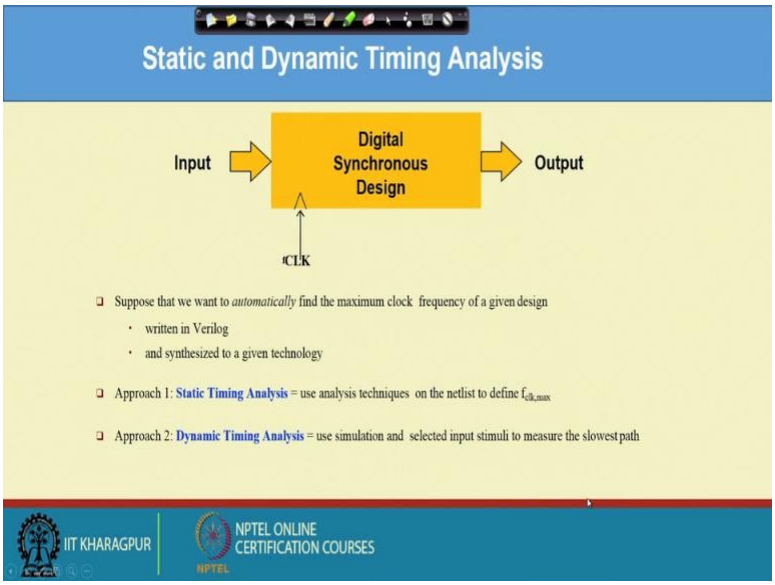

So, today we will start or we will see the issues which are related to digital design ok. So, in digital synchronous circuit; actually in digital design there you may find two type of circuit one is this synchronous circuit another one is asynchronous circuit.

Why I am telling? Actually apart from that actually that is not the case in digital design it is the starting that there are two type of circuit; one is this combinatorial circuit another one is sequential circuit. In sequential circuit you might find two type of circuit that is one is synchronous circuit another one is asynchronous circuit ok. So, what is synchronous circuit?

Synchronous circuit means in the system there will be one single clock ok; that means, all the; that means, the corresponding sequential elements which are present on that particular design, both will be clocked by the same clock ok. So, that means, depending on the same clock all the that means, sequential element they will change their state; it is the not that, but in case of asynchronous there you might find more than one clock. That

means, one clock that may be run at f 1 mega hertz or f 1 hertz or f 1 Giga hertz and another clock in different frequency which may be f 2 or it may be more than that.

So; that means, there is the operation of the sequential element that is not synchronous in case of asynchronous circuit design. So, when actually both has some of the advantage ok. So, where to use synchronous design where to use asynchronous design again itself it is a; that means, a; that means, technical knowledge you know ok; so, but I will give brief idea where you can use this synchronous design and where you will you can use asynchronous design.

So, whenever we are doing this timing analysis; timing analysis means why I required to do this timing analysis? Because to meet the; that means, whatever to find out this f clock. So, in this particular system you see this f clock is the clock basically which is connected to each of the synchronous element, which is present within this digital synchronous design right; so, what will be the maximum achievable clock frequency for this particular design, so that you only able to know by doing this timing analysis.

So; that means, suppose if you see that this if you just have noticed that suppose one that whenever we are talking about the processor; let us say Intel Pentium 4 that may be run at let us say 2.8 Giga hertz. So, 2.8 Giga hertz has a clock frequency where that processor can run. So, why it is needed? Because depending upon that clock frequency now higher the clock frequency; that means, the corresponding computation time which is related to the this your instruction fetching or your instruction to be executed on the CPU or in the processor that becomes lesser ok.

So, that means, you can do the processing or you can do the computation in the processor in a faster way; if the clock frequency is on the higher side ok. So, that is why our mostly our; that means, primary intention always is to do or to maximize this clock frequency ok.

And whenever we have to calculate these a clock frequency; we have to do this timing analysis. How you can do? Timing analysis can be done in two ways one is static timing analysis another one is dynamic timing analysis ok. So, what is static time analysis? Static timing analysis is it uses these analysis techniques on the net list to define this f clock max ok. But in the dynamic; that means, here whatever is corresponding critical

path. Critical path means from the input to the output which part it is taking the maximum time that is the critical path for your system.

So, that particular path how much time it is taking? So, 1 by that time is basically your frequency or the maximum achievable frequency. Then you can ask that if that is; that means, if I make it lesser; that means, if the time period suppose that critical path requires the time of let us say 10 nano second, but if I make that clock frequency of 9, 9 nano second period.

So, at that time what will happen? So, at that time what will happen? Before the execution of that path your data will be changed that the input side; though your operation is still not; that means, it that is yet to be completed because it is required 10 nano second. But at the input what we are doing? You are changing the input at 9 nano second or before that 10 nano second.

So, at the time what will happen? Though the operation is still yet; that means, that is not completed, but you are changing the data means it will take the next data for the computation again ok, so; that means, at the output you will not get the proper result. So, that is why this it actually that is not all for all the things; it is not the case that the critical path. Critical path basically corresponds to this considering the gate delays only gate delays and net delays only.

So, if you consider this gate delays and net delays for that particular path; so, it is not that only because of those factors the critical path is 10 nano second, it may be more than 10 nano second ok. So, why a there is this more than their 10 nano second? That we will see ok, but in dynamic timing approach this dynamic analysis approach what we do? We use this simulation base timing analysis.

Simulation analysis means we keep some of the; that means, selected input stimuli means some of the; that means, what I said that that for static timing analysis the input is not defined; that means, the combination of what will be corresponding combination of input that we have not considered. This is here we do the rough estimation based on this the available information from the gate delays and net delays which is depended on the totally on the library in that means, the from the library I will get those information and based on that I can calculate this what will be the timing requirement for that.

But in dynamic timing analysis what we do? We basically gives a selected set of stimuli; selected state of inputs or the combination of inputs to check what will be for that particular or for those particular combination what will be the timing requirement for this particular circuit ok? So; that means, what? And why I need this; this dynamic timing analysis? Because in during the testing how you can do the testing; during the testing phase what we will do?

We will give some of the test vector to the circuit for properly whether that is properly working or not. So, during that time whenever we are you; that means, giving the proper; that means, in the real time whenever you are giving the inputs; so at that time circuit may fail. So, that is why from the beginning if we check by you; that means, providing some of the input combination to the design and then if we do the timing analysis.

So, at that time the probability of that failure that becomes reduced or my intention is to reduce those; that means, the probability of that failure ok. So, that is why we do timing this dynamic timing analysis. So, this is the 2 condition where we use static timing analysis and where we use dynamic timings analysis.

But for the particular; that means, for any system design which is has to be like in the; that means, chip format or if it is has to be run on the real time. So, at that time both timing analysis we have to do whether that is static timing analysis and that is the timing analysis ok.

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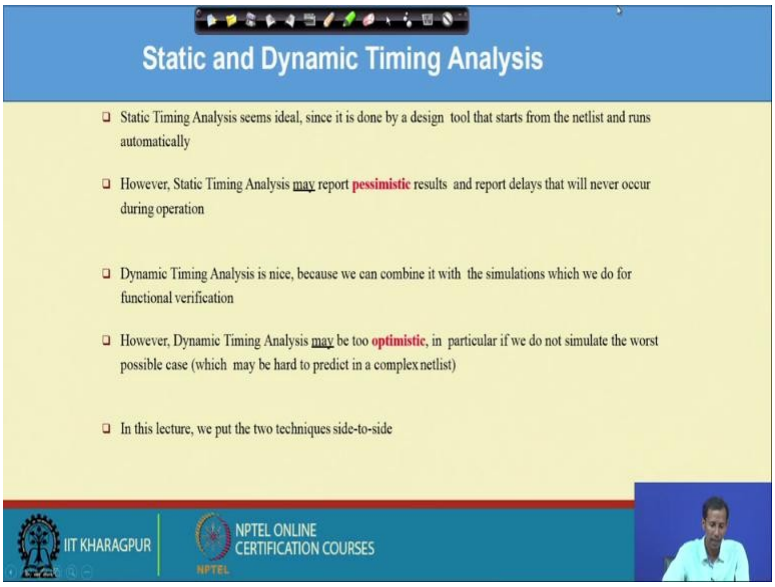

So, here you see this static timing analysis seems ideal; since it is done by a design tool that start from the net list and run automatically ok. Means what? What I said? That based on the library information about the gate delays and net delays, the tool itself it calculates the corresponding timing requirement for that; the critical path or for that the system design. However, this static timing analysis may report pessimistic results and report delays that will never occur during the operation ok.

So; that means, here whatever results we will get that is one rough estimation of the; that means, this circuit; that means, the delay information ok. So, that is why this report may be, that is why it is says that report may be pessimistic results. But in case of dynamic time timing analysis this is; that means, dynamical timing analysis what we do; when we do? Or why we do?

Basically to check what will be the timing requirement whenever we will test it in the real time environment. So, that is why this dynamic timing analysis is very much important because we can combine it with the stimulation, which we do for the functional verification not only for the functional verification during the testing; whatever test vector we will give. So, those stimuli we can put now; that means, at this stimulation itself now we can put and then we can check the timing analysis of the timing requirement for that particular design.

However, this dynamic timing analysis may be too optimistic and in particular if we do not simulate the worst possible case. So; that means, here when this will be; that means, too much optimistic because it is not the case that all the time we can provide all the test vectors and the end we do dynamic timing analysis. Why? Because if the size of the test vectors.

Suppose for a 64 bit at a design ok; so, for a 64 bit adder design; so, what will be the number test vectors? That is 2 to the power 64, so 2 to the power 2 to the power 64 number of test vectors application of that; generation and then application and then do the simulation, it will take too much of time as well as too much of effort. So, on that particular case, actually those who are working on a testing area; so, they at that time see that whatever is the optimized test vector to produce or to that means, testify the circuit whether that is working properly or not; that means, based on the reduced set of or

optimization is done one test vector itself so, that the number of test vectors becomes lesser.

But still I can check all; that means, the possible functionality working or the proper functionality of the design. So, what will be that number? What will be that optimum number? Those who are working on the testing area, so they basically work on that what will be the minimum number of test vectors and what will be the combination of the test vectors ok. So, and then for that your might system will not failure. So, those type of things do who that means, who the people working on the testing and verification area ok, but this two particular case we use for any VLSI chip design ok.

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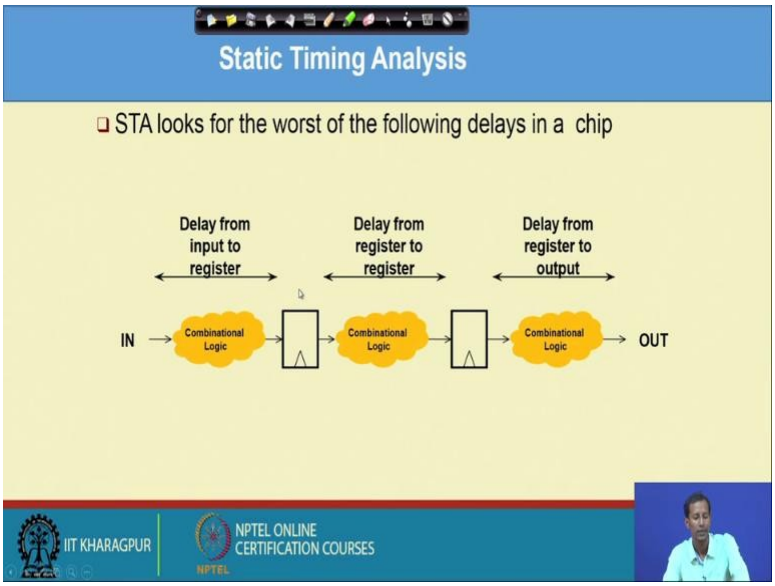

So, this static timing analysis; what is the idea of static timing analysis? Suppose I am having the input to the output, whatever the systems that is the block diagram representation of the, that system we have seen in the earlier slide ok.

Now consider one particular that inside of that system design ok. So, inside of this system if there are these 2 are the registered or the sequential elements and they are being connected inside between this communicational logic; 3 communicational logic this is c 1 this is c 2 this is c 3. So, then this is the application of the input; so, this is the delay form input to the register which is happening because of this combinational logic.

Then this delay form register to register and considering the corresponding factors or the corresponding logic which is available in combinational logic. And delays form register to the output, which is again passing through another combinatorial logic. Actually why these 3 are different and when these 3 will be much. If these registers are not there at that time this total delay will be this c 1 the delay of comb this c 1 delay of c 2 plus delay of c 3.

But as I have put this registers in between that means what? I am this data dependency has became now lock dependent. Clock dependence means though there is a change; actually in combinatorial circuit what happens? If I change any of the input, the output automatically tries to change or the corresponding logic elements; they starts their operation. But in sequential element unless and until you are finding the edge of; that means, whatever the logic whether if it is edge triggered. So, unless and until it is finding the edge; it will not start its operation so; that means, now what? It is depending on the clock, it is not depending on the data.

But in sequence combinatorial circuit; if you change any signal; so, automatically that will reflect at the output. But in sequential element if you find the edge then it will go for checking the whatever; what is the value present at the data. So, based on that data, now the output will change. So, that is why now this is which is getting the highest priority, the clock 1.

So, that is why this is clock dependent; not data dependent sequential element got it? And that means, basically based they for that particular property, if we put the registers in between; so, that becomes this at that time this c 1 c 2 c 3 that became individual to each other ok. So, now we have to calculate the timing analysis for this ok.

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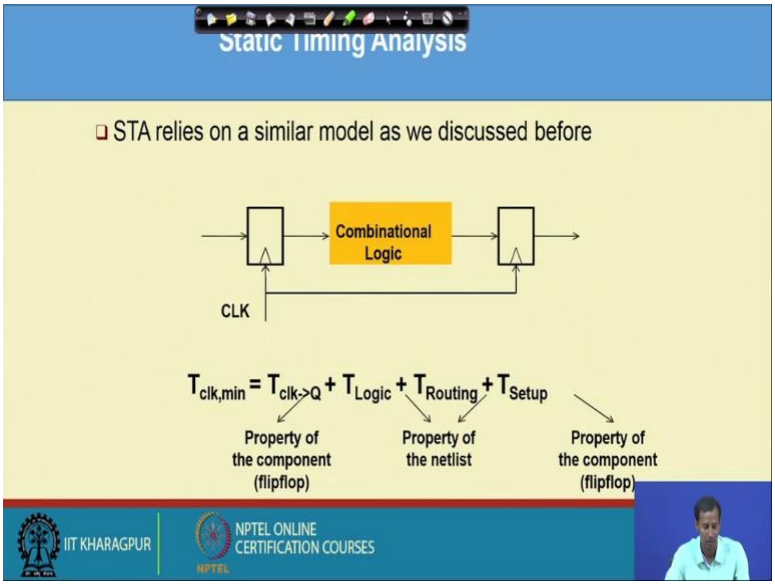

So, this STA how you can calculate? So, that means, whenever there is; so there are input to the registers, then register to the register, then register to the output ok. So, here you see inside of this register to register whatever is the logic; so, that will be considered as the timing requirement; minimum timing requirement for the corresponding clock.

So, then what will be the corresponding value for this? The value for this will be T clock to Q; T clock to Q means? What is the meaning of this? This is the delay of the flip flop itself. The delay of the flip flop itself means from clocking to the delay; that means, the output which is the Q; it has actually if you just remember the that corresponding; that means, internal structure of flip flops. So, 4 NAND gate are there right so; that means, it has to the clock has to pass through 2 levels of this AND gate; sorry the NAND gate.

So; that means, it also it has some of the flip flop itself has some of the delay for propagating this clock to the output ok. So, that delay is basically mentioned over here, this is T clock to Q. Then whatever is the this logic delay or the corresponding gate delay for this combinational circuit; that will be again considered or that again it will come to this part.

Then this routing; routing means this is nothing, but the delay which is associated for the; that means, net delay. Net delay means as they are being connected from gate 1 to gate 2 or gate 2 to gate 3; as the wire is connected, so because of the wire it also as for the wire there is this RC component. So, because of that it also take some time to the

signal; that means, for the signal to traverse from one point to another point or one node to the another node through that particular wire.

So, those delay will also be considered in this case. So, that is this T routing and then again there is another; that means, delay which is also associated for this computation of this minimum clock period which is this T setup. So, what is setup? What is setup time what is whole time? I think that is basically mentioned or that can be recalled in the or that is mentioned whenever in the basic digital design. But still we will again we will discuss what is the setup time and whole time; we will revisit that ok.

But this T setup that is one of the requirement for this particular flip flop; why that is required? Ok; so that we will see later of this presentation ok.

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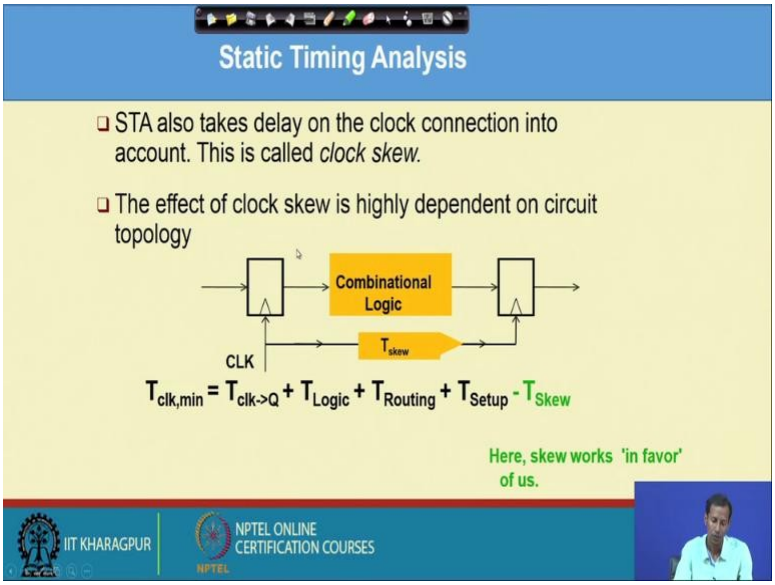

So, after that; that means, all these particular things will come whenever we are computing this T clock minimum. But then again if the clock has some of the skew; so, if the clock has some of the skew means what?

What is the meaning of clock skew? In synchronous design it you might have to be very much causes because as it is clock is synchronous to each of that means, sequential element. So, at that time so many factors are basically associated with that; one of them is this clock skew then not only clock skew clock jitter is also there.

So, what is clock skew? What is jitter that we will again we will discuss that during; that means, in the other way other slides. But here actually for the timing being if you consider if this clock T clock; that means, this if this clock has this skew, then and that is in favor. In favor means if from this part to this part, this clock skew is basically positives.

So, at that time this T skew will be minus from the corresponding delay; why? Because here skew works in the favor of us; that means, favor of us means favor of the circuit now it works. So if in favor of circuit it works as this direction the clock direction is basically traversing from this side to this side. So, that is why this clock skew; that means, the data is also flowing in this direction and clock is also flowing in this direction. So, at that time it is favor of us, but if the clock is basically supplied in on the opposite side of the data suppose in this direction data is supplied.

But in the opposite direction if the clock is supplied; so, at that time this skew will not be in favor of us, that will be against of us or the against of us means against of the design. So, at that time this T skew also be you will be added for finding out this T clock minimum. So, why actually what I said in the beginning that these things or this static timing analysis that has been done through the EDA tool automatically right?

So; that means, whenever this depending on this kind of fact is the EDA tool itself automatically computes what will be the corresponding values of T clock minimum considering each of these factors. Now each of these factors how we will get? This T clock to Q, the delay for this flip flop that, it we will get from library; how many levels or what are the; that means, gates are connected for this logic delay.

So, that again you can compute from the library or you can get the information from the library itself. Then what will be the net delay? Again that will be again from the library itself, what is the set up requirement of for the flip flop again that comes from library. And then what is this clock skew then again that is also you can get from the information provided to you only so; that means, all this information is already stored in the library.

So, the tool itself it fetch those data and it computes based on this equation and it shows to you that this is the minimum clock period requirement for your design ok. So, here you see that STA takes delay on the clock connection into account, which is called as this clock skew. The effect of clock skew is highly depended on the circuit topology; that

means, how you have what topology you have used for the circuit representation that is a important factor over here for this Q.

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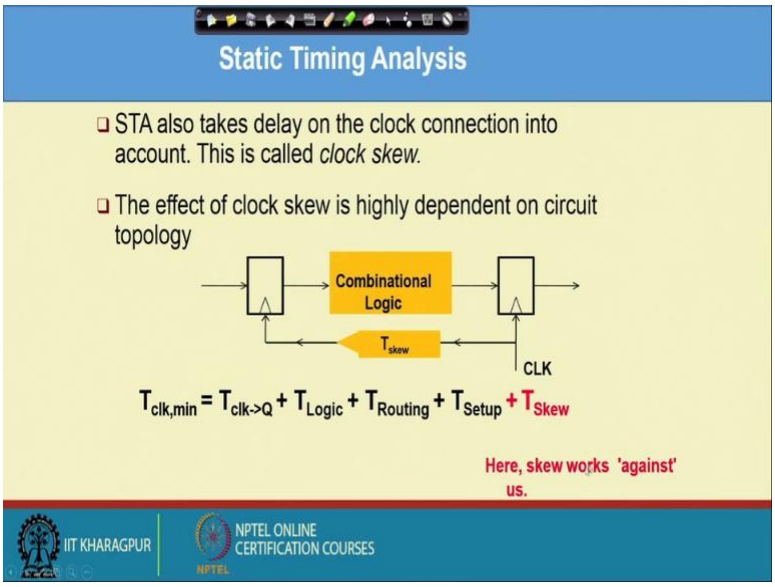

So, if you just see that if I make this; that means, if I supply this clock in the opposite direction of the data; so at that time clock skew will be added to this; that means, this corresponding equation ok. So, here you see skew works against us ok.

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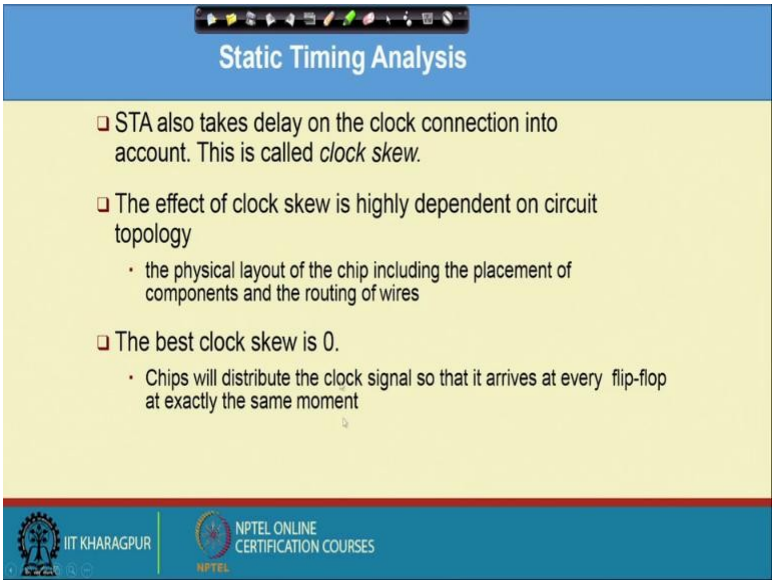

So, the effect actually the effect of clock skew is highly depended on circuit topology that we have already seen. But the physical layout of the chip including the placement of

the components and the routing of the wires; that means, routing of the wires means how this clock is; that means, in which direction I am supplying the clock that is dependent for computing this skew.

So, if it is against the data; that means, opposite to the data; then it will be added if it is same direction with the data; so, at that time it will be subtracted ok. And the best clock skew is 0; chips will distribute the clock signal so that it arrives at every flip flop at exactly the same moment. Suppose in a chip 1000 sequential elements are placed and you have only one clock source that; that means, the; so, the clock will be connected to one pin.

So, from that pin now you are supplying to 100; let us say sequential element. From that particular point to reach the maximum or there that; that means, the farthest sequential element present from that particular p. So, it will take the maximum net delay or the maximum for traversing that clock to that particular element. So; that means, at that time skew will be high enough for that supplied or those; that means, that particular part ok.

But what I said? Skew is sometimes it is better, sometimes it is; that means, not it is worst case condition for our circuit design ok. So, but in case in the ideal case if you consider this clock skew is 0; that means, clock skew is 0 means each of the clock each of the sequential element has been connected to the clock in a uniformly distributed network. That means, from suppose from clock connected to the 1 and clock connected to the farthest element they takes same amount of time.

If they take same amount of time at that time this clock skew or we can consider that as a 0. So, clock skew means is a time gap between the closet one to the farthest one. So, this is the; that means, this concept of this timing analysis static timing analysis and ok. And this clock skew is an important factors; not only clock skewed it then setup time and then through this clock to Q then this T logic.

So, during optimization what we actually till now what we have done? This combinatorial design or the combinatorial logic part, we have done reduction of the timing or reduction of the area on those particular path, but we have not considered the other things, which are associated in the whole timing closure calculation so, that we will be seeing continuation of this particular lectures ok.

So thank you for today’s class; again we will meet on the next class.