Architectural Design of Digital Integrated Circuits
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Lecture - 60
Design Tips for Basic Circuits Design (Contd.)

So, welcome to the course on Architectural Design of ICs. So, in the last class we are seeing the sequence detector example ok.

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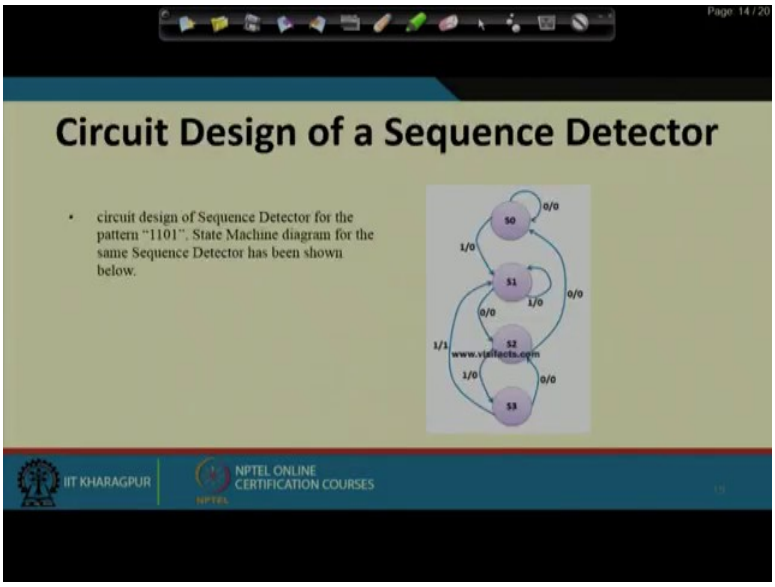

So, in sequence detector example; we have to detect the corresponding sequence of 1 1 0 1 ok. So, what we did is that, first we have developed the finite state machine which will detect this sequence 1 1 0 1 ok. So, once we have developed or once we have actually this draw the corresponding finite state machine and finite state machine as we have to detect this 1 1 0 1 sequence. So, depending on that only we came to this finite state machine. If this sequence is different, so at that time this FSM will also be different.

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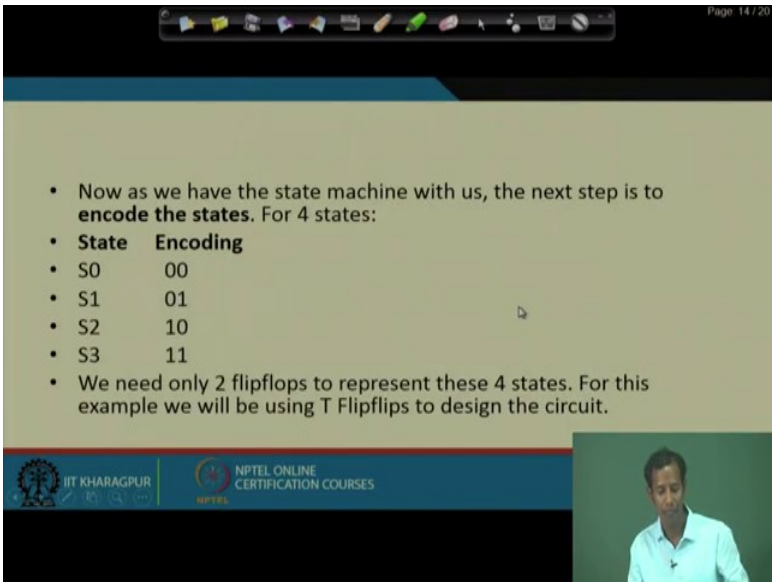

So, after that as we have to detect the sequence of 4 number sorry 4 bits. So, that is why we are having 4 states. Now, what we have to do is that we have to encode this 4 state by this S 0 to 0 0, S 1 to 0 1, S 2 to 1 0 and S 3 to 1 1. So, as we are having 4 states so, we need 2 flip flops. So, using 2 flip flops we can easily; that means, build the corresponding circuit of it. Now if I have to detect sequence of 5 bit. So, at that time the minimum requirement of this flip flop will be.

So, at that time there will be 5 state so, 5 state means at that time we have to consider 3 flip flops for designing the corresponding circuits ok. So, and then for this example we will be using T flip flop for designing the circuit. So, now, how to, what will be the logic? How to know that this is the logic which will be implemented this particular sequence detector.

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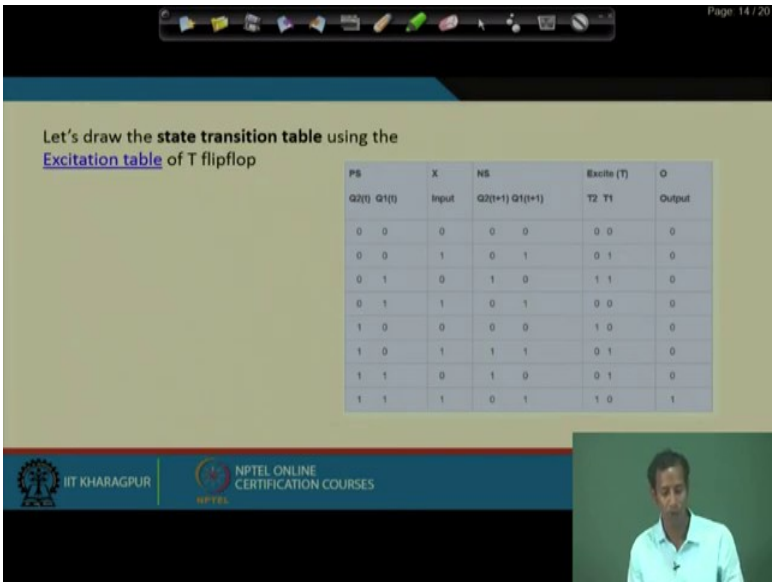

So, now next what we have to do? We have to do we have to draw the corresponding excitation table of T flip flop. So, from this T flip flop excitation table so, as we are having this S 0 0 and like here this S 0 is 0 0 and it is having two branch; one for 0 another for 1 ok. So, then if I consider this is 0 0 0 0 for state 0, if the input is 0 then it will go to the next state or it will remain in the same state.

If it is depending on this, when this is 0 0; that means, the input is 0. So, at that time the output is 0 and again it remains in the same state. So, that means; the present state is this 0 0, if the input is 0 0, the next state will be also of 0 0 ok. And then when this present state is 0 0 and x; that means, the input is 1 so, at that time the next state will be going to the S 1 so, which is 0 1.

Then for this state S 1 which is 0 1 if the input is 0. So, at that time it will go to next state which is corresponds to this it will go to S 2, S 2 is nothing but, this 1 0 whether this input is 1. So, at that time again it will remain on the same state which is 0 1. Then again for state S 2 which is 1 0 if it finds that the input is 0. So, again it will go to start from S 0 depending on the corresponding that FSM what we have drawn earlier.

So, 0 0, then if it is 1 0 and the input is 1 then it will go to the S 3 state which is 1 1. So, something like that we have just derived these particular equations from these tables from the state diagram or this FSM. So, actually, depending on the excitation table of T flip flop now, for this next present state to the next state depending on this excitation

table. Now, we can actually derive as we have to develop or we have to design the circuit using d flip flop that is why we have to use the excitation table of T flip flop ok.

So, depending on this now, what will be the present state what will be the next state depending on this; this will be its the value of the excitation table of T flip flop ok. And what is the output? The output is here you see for all these is 0 only when this S 3 finds it is input as 1 then only it produce the 1; that means for these particular for 1 1 1, the output is 1 in rest of the case all are 0 ok.

So, when this q 1 is the present state 0 to 0 T flip flop, this is 0 0 to 1, this is 1, this is 1 to 0, again 1, 1 to 1 this in T flip flop this is 0, 0 to 0 0, 0 to 1 1, 1 to 0 1 and 1 to 1 1. So, for Q 2; so, 0 to 0 0, 0 to 0 0, 0 to 1 1, 0 to 0 0, 1 to 0 1, 1 to 1 0, 1 to 1 0, 1 to 1 sorry 1 to 0 that is again 1 ok.

That means the Q 1 t to Q 1 t plus 1, corresponds to the excitation table this value we came from the excitation table of T flip flop ok. So, once we have developed this will be the corresponding output. So, now we need to put it in the Karnaugh map for the logic simplification ok.

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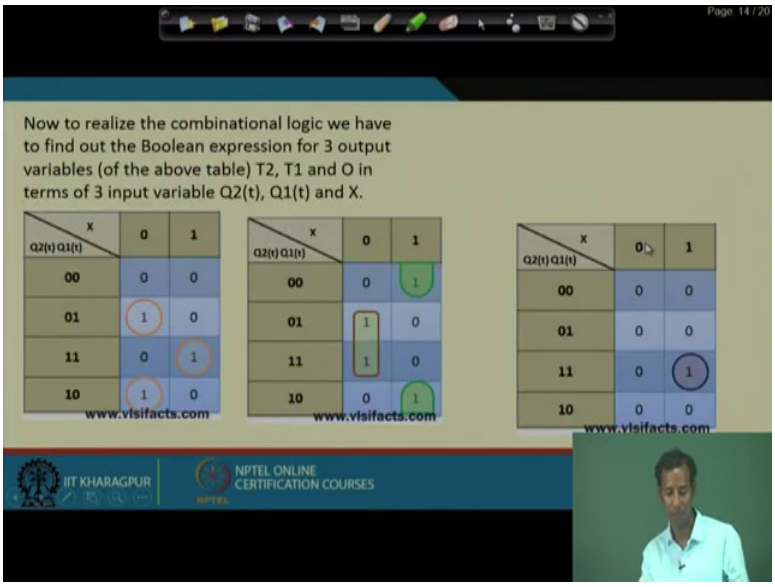

So, now, whenever for this Q 1 Q 2 and for X, whether that is 0 or 1. So, we can get the corresponding T 2 3 table; one for T 2, one for T 1 and one for this X which is sorry for

O. So, this is for O where only for this 1 1 1, this is 1 and for this for T 1 we have having this Karnaugh map of this and this and for T 2, this is something like this.

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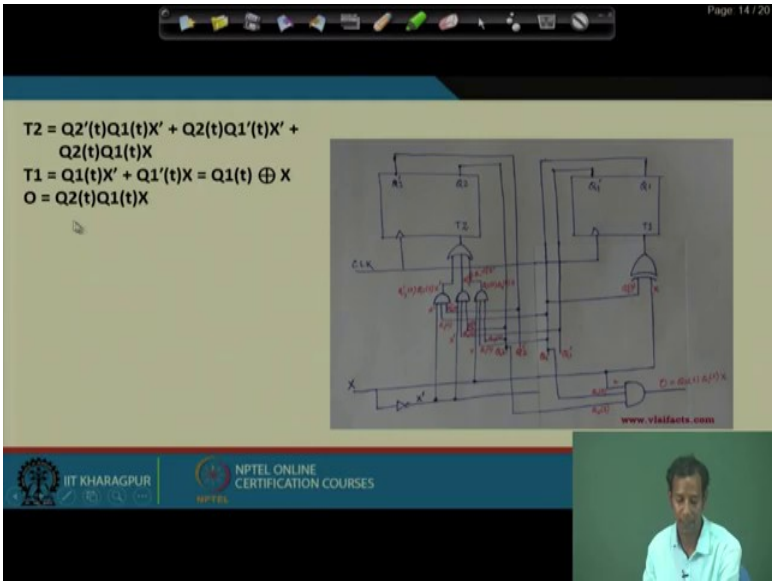

So, depending after placing or after designing this Karnaugh map we will get the corresponding logic of T 2 as Q 2 dash t Q 1 and X bar. So, T 2 means this one. So, Q 2 Q 2 bar plus Q 1 sorry, Q 2 bar Q 1 and X bar for this this is Q 2 Q 1and x, for this; this is Q 2 q 1 bar X bar. So, T 2 will be Q 2 bar Q 1 X bar Q 2 Q 1 bar X bar and Q 2 Q 1 X for T 1 this is what this is Q 2 this is Q sorry, this is Q 1 Q 1 X bar plus Q 1 bar X ok. So, Q 1 X bar is for what Q 1 X bar for this one 1 1 and this is common for 0. So, here Q 1 and X bar and for this it is Q 1 bar X.

So, this is nothing but, Q 1 XOR with X and for the output. So, for the output the logic is Q 2, Q 1 and X. So, once we derive the equation of O; that means, this is the output of T 1 and T 2. Now if we develop the if we draw the corresponding circuit based on these three equation we will get the output as this one and then the T 2 and the T 1 will be the inputs to this particular T flip flop where; that means, this is for T 2 which corresponds to this particular equation this is the t 1 input which corresponds to the XOR gate.

And finally, we will get the sequence detector. Now these particular circuits will work as a sequence detector of 1 1 0 1. Now, if it is been asked that you have to detect one different sequence, so, at that time starting from making the state diagram and then using the states; that means, this excitation table you make the corresponding; that means, then

again using the Karnaugh map you will get the expression for T 2 T 1 and the output and then you draw the corresponding circuit of it to get the sequence detector of the corresponding whatever has been asked to detect the proper sequence. So, this is the steps how we basically design one sequence detector ok.

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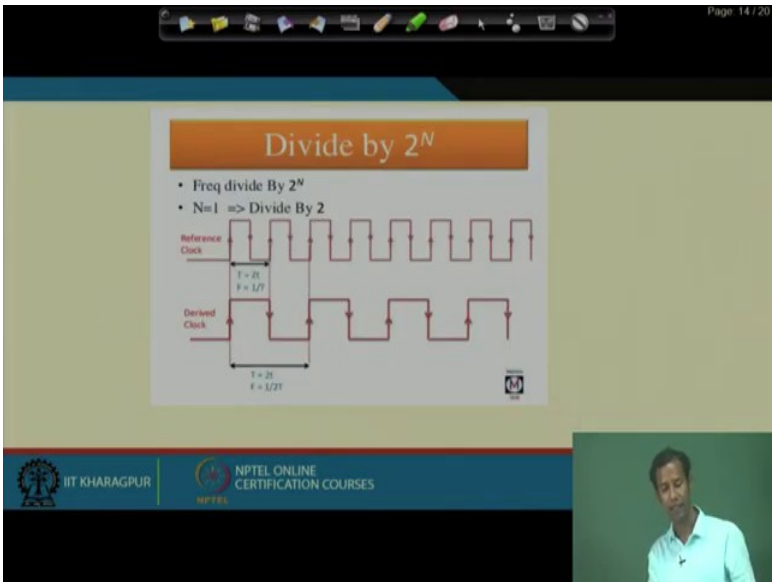

So, then again, we will see actually initially we have seen that multiply by 2 clock, multiply by 2, multiply by 4, multiply by 8, that everything we can do. Now, we have to design divide by 2 to the power N ok.

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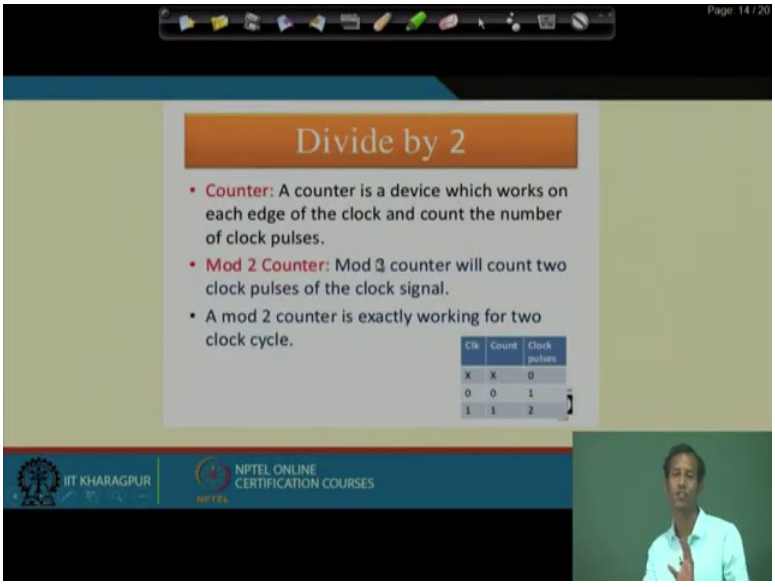

So, divide by 2 to the power, let us consider now N equals to 1; that means, divide by 2 counter. So, how we can do? We need one counter this mod two counter which will only count 2 clock pulses of the clock signals. Sowhen this clock is 0 and the count is 0 the clock pulse is 1 and when this is 1 1, the clock pulse will be at 2.

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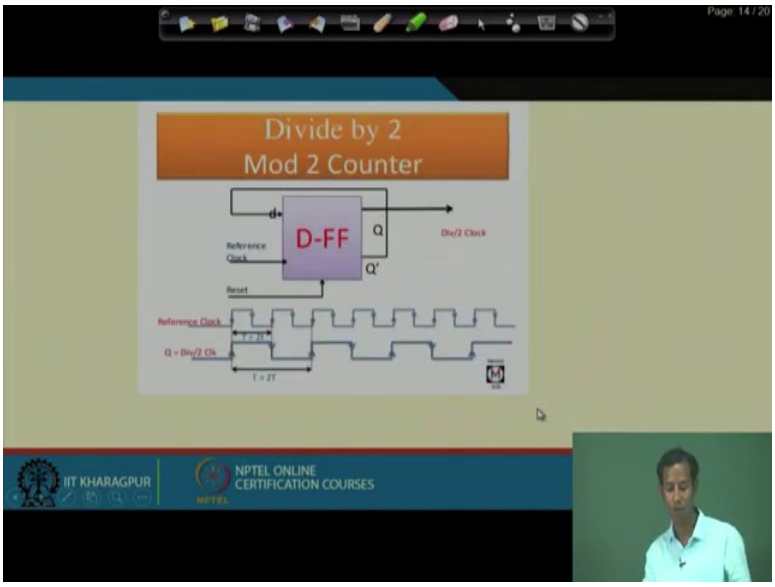

So, how to design only by that; that means, D flip flop only one single D flip flop you can make the divide by 2 counter sorry, divide by 2 clock generator or if this is nothing but this mod 2 counter. So, what is that? The Q bar is basically input to the d. So, this is the reference clock so, reference clock. So, initially what will happen? Initially, if this is 0 then whenever it finds the edge, so, Q 1 will be 1.

So, it will be just gone to the next. So, when it finds that Q bar equals to 1 and this is 0. So, at that time at the very next edge what it will be the Q now, this is the d input which is 0. So, now, this is 0 this will be 1 initially, after that again when it finds that next edge at that time what it will be it will be just 1. So, Q bar will be Q will be 1 and this Q bar will be 0. So, this Q bar will come over here at the d.

So, at that time it is 0, then again it is 1, then again it is 0, then again it is 1, then again it is 0. So, something like this with these particular things will be toggling ok. So, toggling depends on the corresponding clock edge. So, as it is finds if this data is changing for one particular clock. So, that is why if you see this is nothing but the divide by 2 clock ok.

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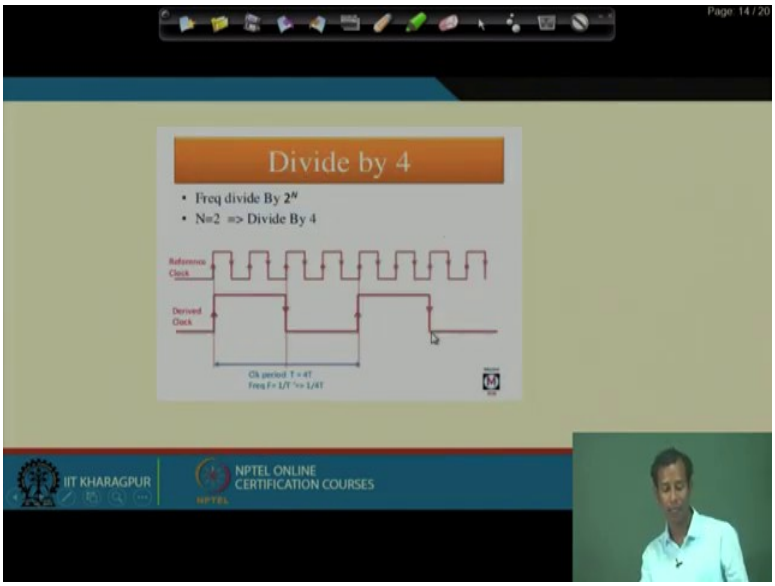

Now if I have to make the circuit of divide by 4 clock ok. So, whenever this N value is 2; so, at that time I have to divide the clock by 4. So, how we can do? That means, at that time the corresponding signals will pass 2 clock cycles to make it.

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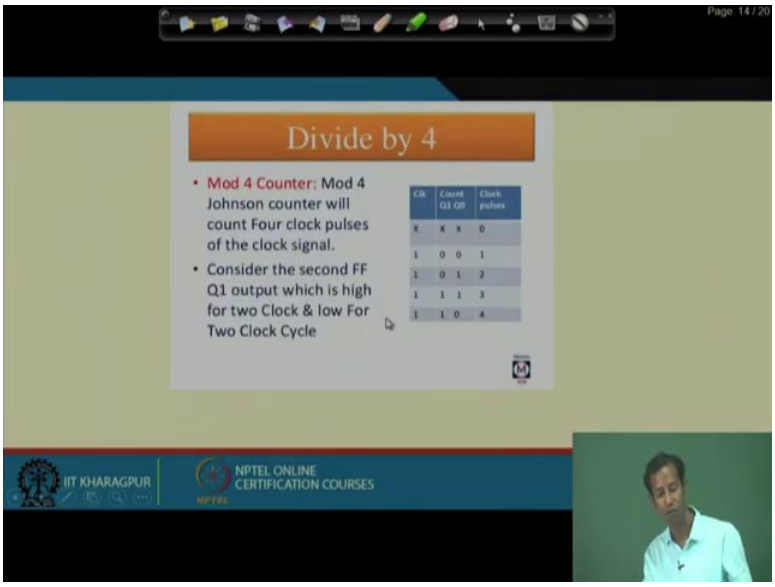

So, at that time what will be it is circuit? We need so, initially for divide by 2, we need mod two counter here we need mod 4 counter. So, mod 4 counter means this the last count will be 1 this 1 1 ok.

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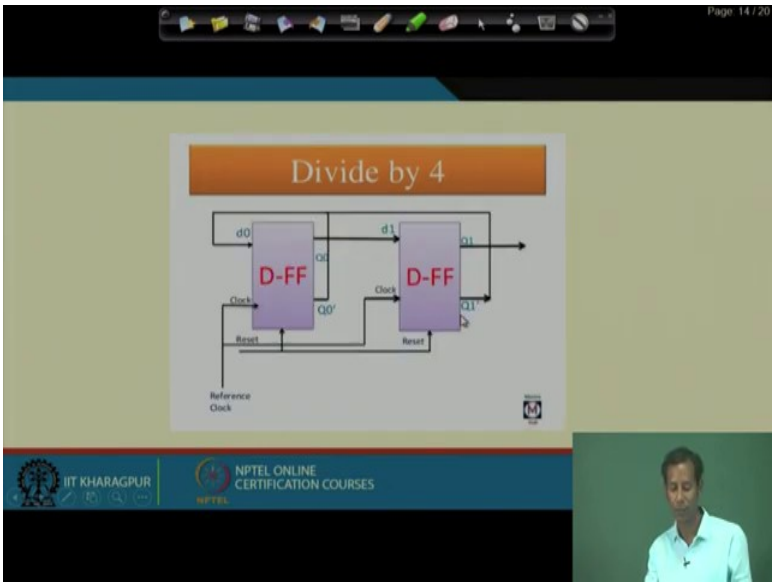

So, 1 1 means here you see initially this Q 0 is connected to d 0 and this Q 1 is also connected to the d 1 of this.

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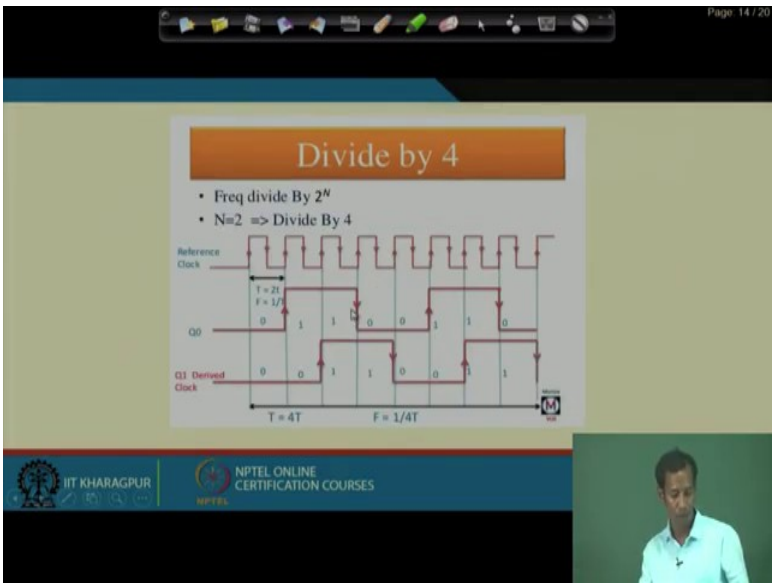

Now, in case of divide by 2 only one, the T counter; that means, this 1 T flip flop is enough. Now in divide by 4 if you passed if you pass this divide by 2 again 1 another d flip flop. So, then again it will be again it will be divide by another 2. So, now it will make as or now it will become as divide by 4 clock ok. So, then if you just see that this is the Q 0, this is the; that means, reference clock.

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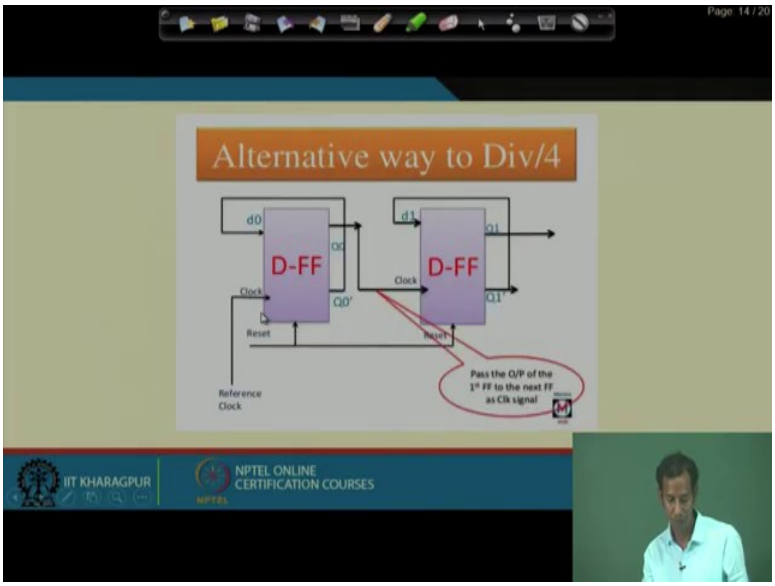

Now this is the Q 0 then this is the Q 1 and Q 1 now if you just; that means, if you just make this then this is the output; that means, this corresponding Q output is now the clock; that means, whatever this divide by 2 clock, if I pass to the next step t flip flops as the clock. So, then it will be the output d output will be nothing but the divide by 4 clock.

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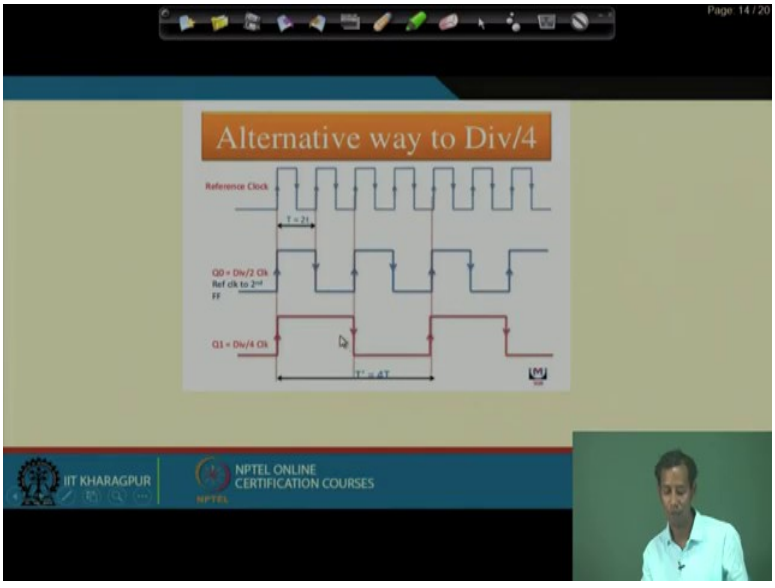

Here you see this is the reference clock. So, from this Q 0, we are getting this divide by 2 clock then that is the clock for the second T flip flop, then again this will be again divide by 2 which will make the divide by 4 of this reference clock ok.

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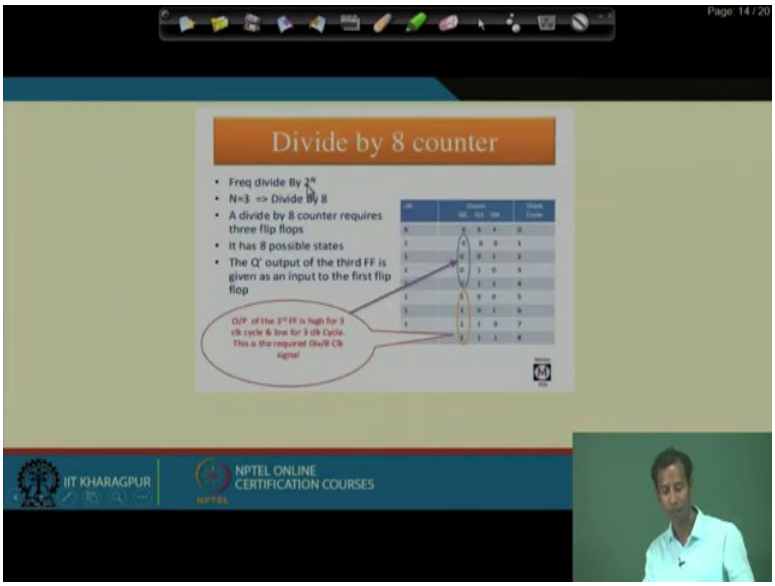

So, then again divide by 8. So, how you can design divide by 8? Divide by 8 means it you will be having four clock pulses sorry 4 here and then again four for the lower; that means, for 0.

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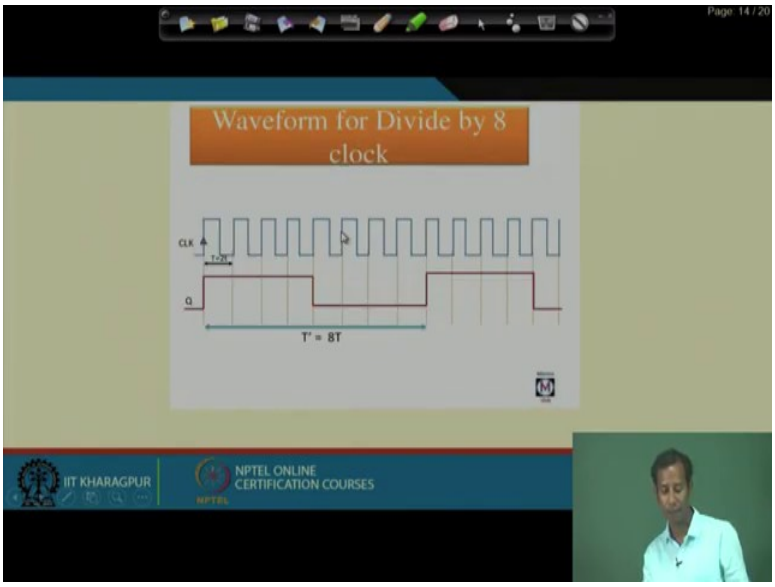

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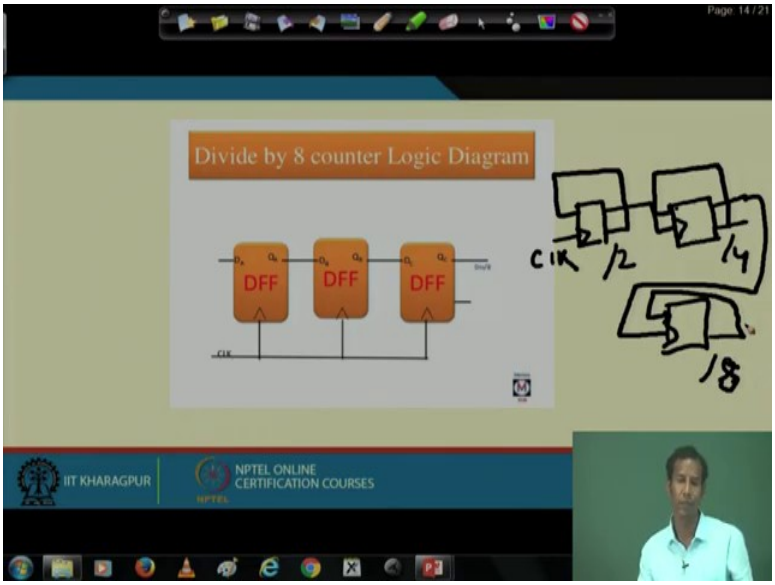

So, what we can do? You will be having this you will be at that time what it you will be what you can do is that for you will be having the clock signals then you will be having this, then the output from that it will be just as the clock signals to the next one. So, this is the reference clock ok. So, this will produce divide by 2 then again if I connect this here. So, this will produce the divide by 4.

Now this again this if I connect this to particular clock to the third one and again this is here so, now, this is divide by 8 ok. So, that means, after the first T flip flop, it will be divide by 4, then again the output from here that will be the clock for the next one it will produce divide by 4, then again that is the output from that that is the clock to the third one which will provide you the divide by 8 ok.

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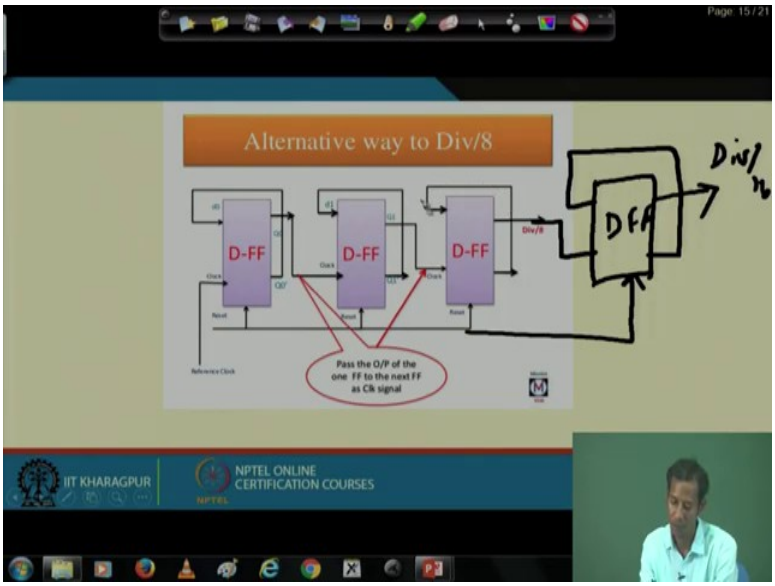

So, in this manner we can you can actually this develop divide by 8 as well as divide by here you see this is nothing but this Q 0 is connected over here for the first flip flop you are getting divide by 2, for the second flip flop you are getting divide by 4 for the third flip flop you are getting divide by 8.

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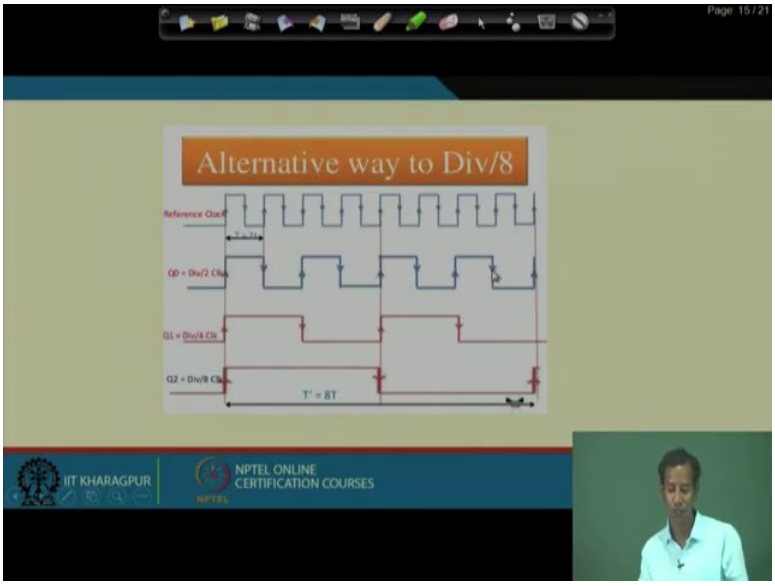

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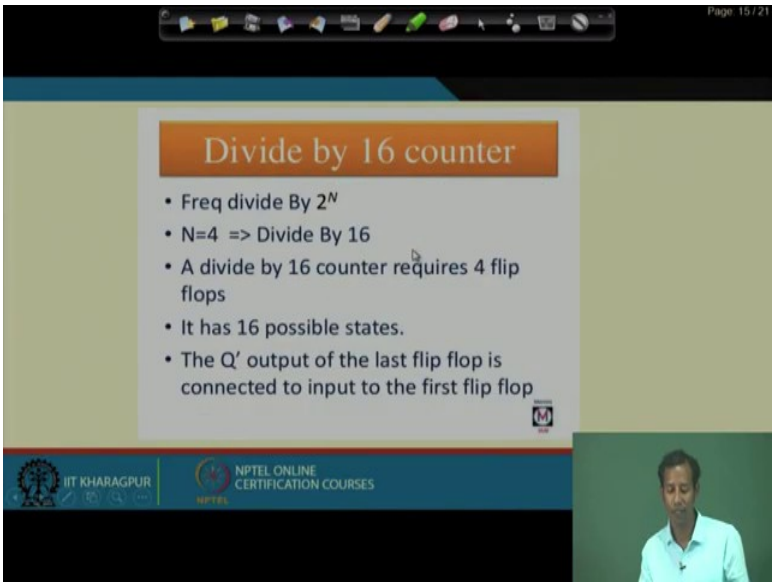

So, the same manner if you want to divide by 16, you will be having or you need 4 flip flops.

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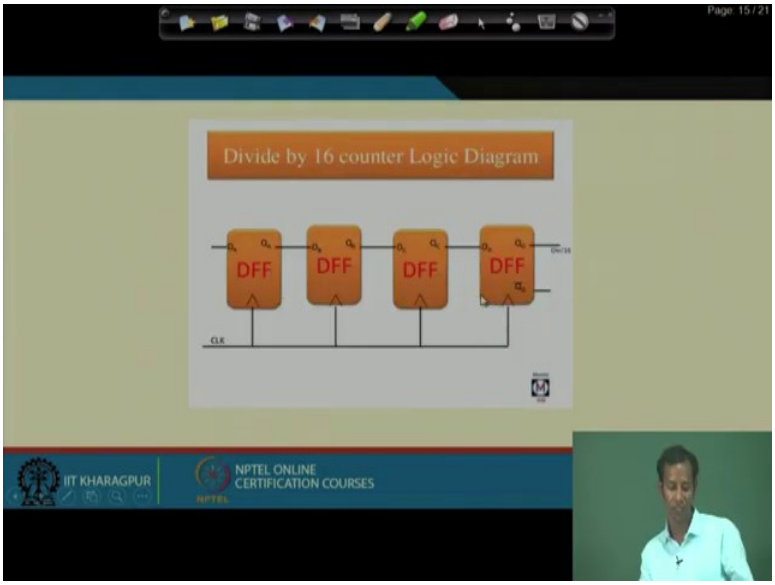

So, 4 flip flops; how they will be connected? So, in the same manner; now the output, now the output of this will be connected to the that another flip flops over here where this is the clock and the output will be something like this which will produce this is divide by 16 and this is here is the reset signal which is coming to the system. So, all this is nothing but the D flip flop.

So, D flip flop; that is why this Q bar is connected over here ok. If you use T flip flop then at that time this with this if you connect then it will be no problem. So, in this manner we can design any of this divide by 2, divide by 4, divide by 8, divide by 16. So, this is very much easy if you need divide by 32, you add another flip flop it will be again divide by 32.

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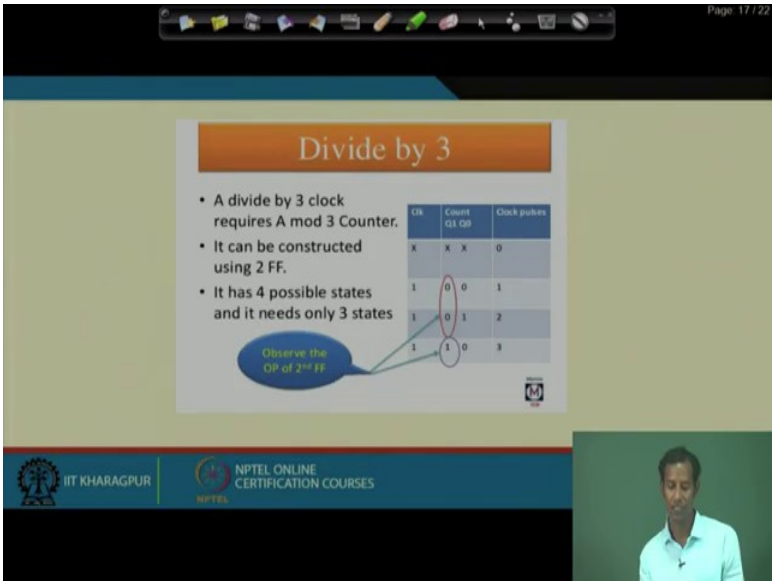

Now, suppose we have to design that divide by 3 ok. So, at that time that is not that much easy just like whatever we did in case of divide by 2. Whenever it is power by power of 2 divided by power of 2, at that time you connect the stage you increase the stage, you will get the corresponding output. But in case of this divide by 3; that means, when the power is not of 2 at that time you need one for divide by 3 clock requires one mod 3 counter ok

So, and it can be constructed using 2 flip flops it has 4 possible states and it needs only three states to be used ok. So, what are these 3 states? The 3 states are these 1 0 0, 1 0 1 and 1 1 0 ok.

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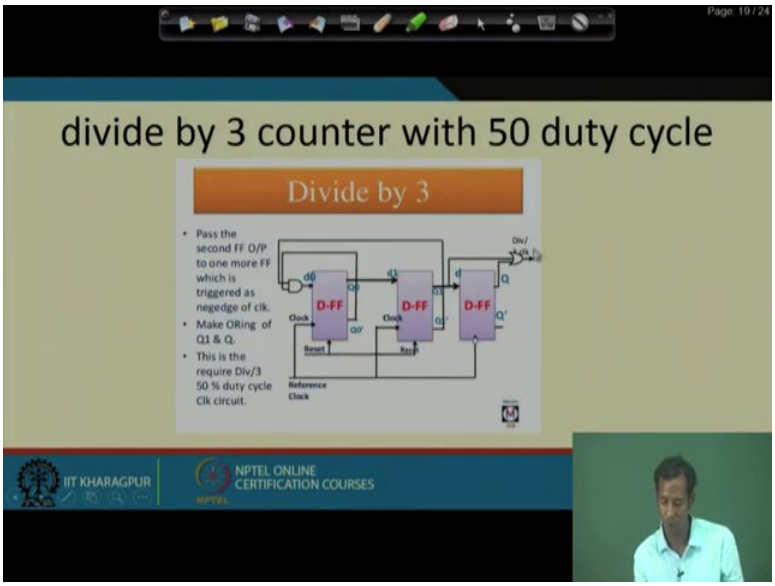

So, now if you just make this, at that time what it says that observe the output of the second flip flops that for these two case the Q 1 is all time it is 0 and here it is 1 so; that means, this is the terminal count. Now based on that if you just connect this like, you are having the in case of only mod only by 2, at that time what is there? That means, you have to connect these two here ok.

So, whenever you are having this; that means, finally, you are having that up to mod 3 so; that means, mod 3 where from you will get? Mod 3, you will get from the corresponding the second flip flops output. So, here one and this one if it is ANDed and it is the input to the first flip flop then you will get the corresponding that; that means, the divide by 3.

But here I need that divide by 3 and with 50 percent duty cycle ok. So, 50 percent duty cycle whenever you need so, at that time you need one extra of these particular gates which is required to make the duty cycle of 50 percent. What is the logic then? Then you have to OR with this and the corresponding third flip flops output. If you do that then this circuit will gives you the divide by 3 with 50 percent duty cycle.

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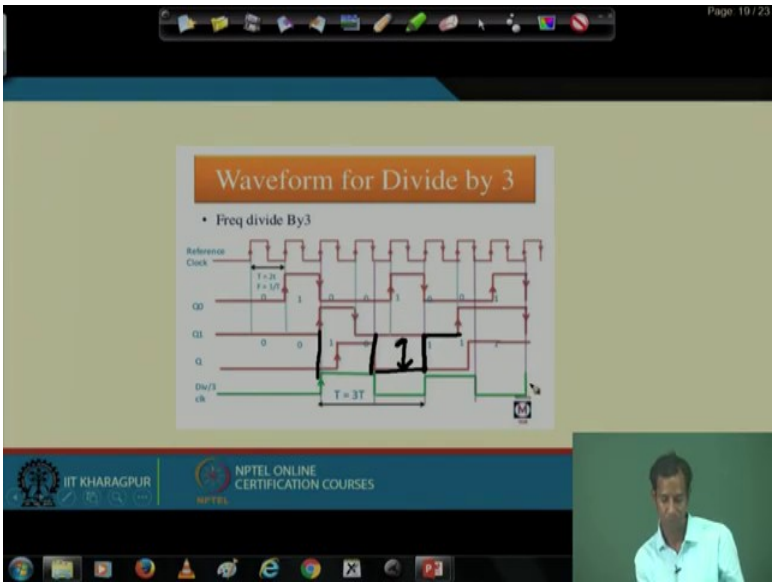

So, here you see if you see the; that means, timing diagram. So, this is the reference clock so, the Q 0 will be dependent on what this Q 0 bar and Q 1 bar so, depending on that the Q 0 value will be something like this and what is the Q 1? Q 1 is nothing but, Q 1 is nothing but the Q 0, which is 1 bit 1 clock cycle shifted. So, this is nothing but this ok. And, then you will be getting the corresponding Q ok.

So, what is this Q? Q is the output from the third one. So, Q is dependent on the Q 1 ok. So, now, Q 1 again that is shifted so, Q 1 is shifted means; depending on the corresponding this the flip flop delay it will be just after that means, Q 1 is now here Q is also shifted by the clock to Q delay. Then the output is basically the OR of this Q 1 and Q. So, Q is this one and Q 1 is this one.

So, whenever I need so, at that time as this is OR so, for this particular this will be 1 and in this two both of them Q 1 and Q both of them are 0. So, the value will be 0 over here then again at this Q 1 and Q 0, Q 1 based on the values of Q 1 and Q you will be getting the divide by clock 3 output as this one, then again at this you will be having both of them are like 1 1. So, at that time again you will get that output as 0.

So, if we do this so, based on this Q 1 and Q you will be getting the corresponding divide by clock 3. Now as you see that this is basically the sequence is now that 1 2 and 3 ok.

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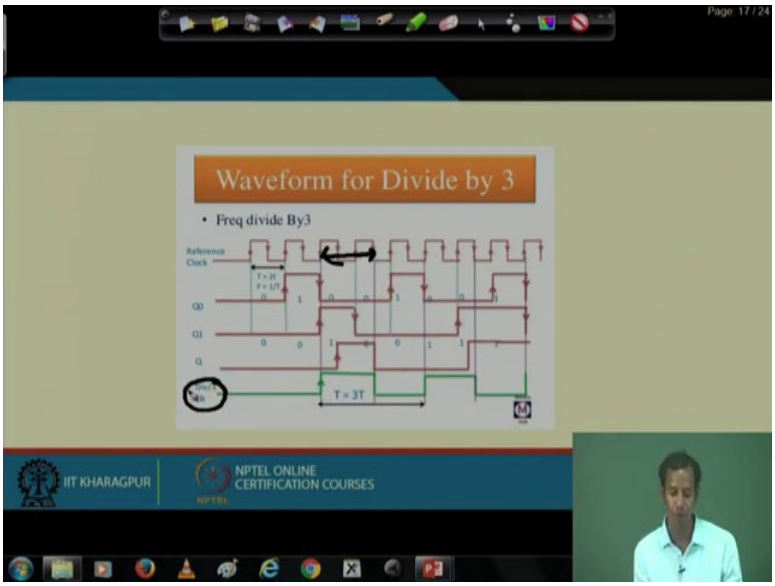

So, the 3 clock divide by 3 means; the total it requires 6 clock cycles ok. So, how 3 clock cycles sorry, 1 2 and 3. So, 1,2, 3, clock cycles it requires 2 which will be produced by this divide by clock 3 output here from here ok. So, this is the circuit for divide by 3 with 50 percent duty cycle. And what I said is that you have to use this extra gate to make it 50 percent duty cycle otherwise you do not have to use that.

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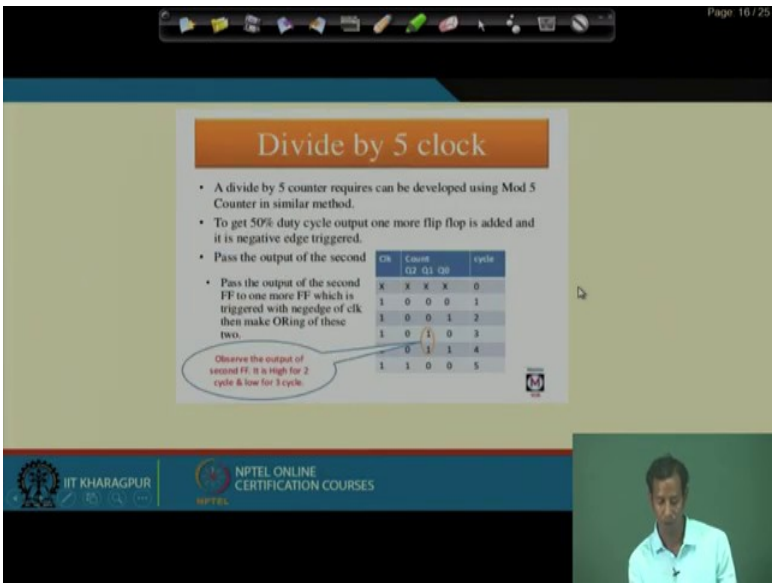

Now again another circuit I need which will be using this divide by 5 ok. So, a divide by 5 counter requires can be developed using mod 5 counter in similar method to get 50

percent duty cycle output, one more flip flop is added and it is negative edge triggered and pass the output of the second flip flop, means depending on this Q 1 you have to pass the corresponding logic.

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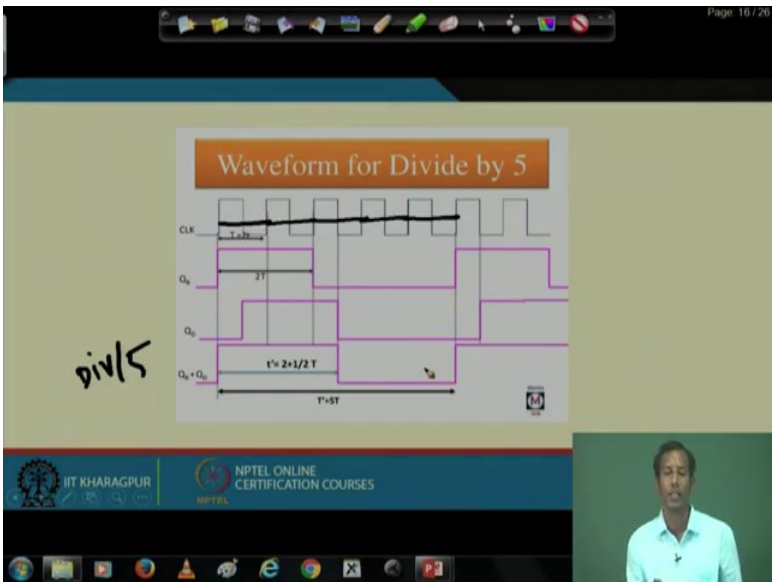

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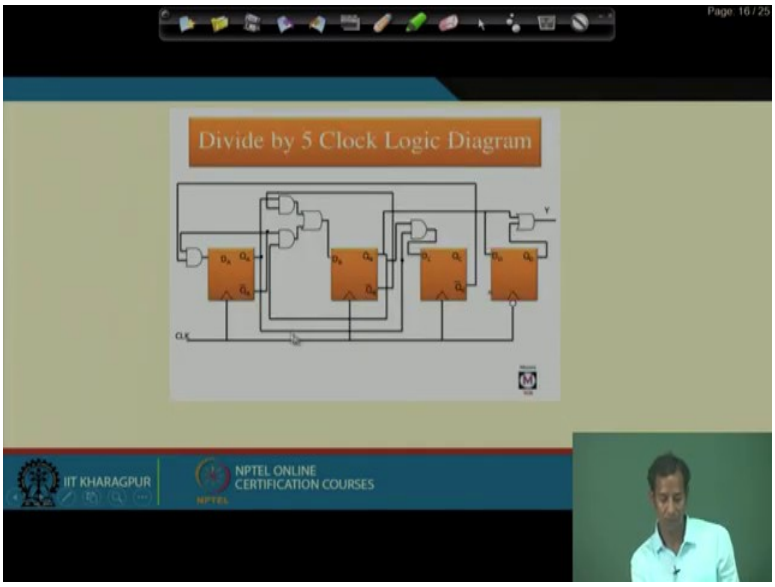

So, here is that that means now, this is the circuit is something like this. So, here in this you are basically calculating this is nothing but the mod 5 counter. Now you are having one extra this delay oh sorry, extra amount of this gates which will produce this divide by 5 with 50 percent duty cycle.

So, what is that? That means, here it will be Q B and Q D, then depending on this Q B and Q D, now you will whenever we will OR those at that time I will get the corresponding function something like this. So that means, here actually 1 at these particular edge 1 and 0. So, 1 within this this is 0 0 so, it is 0 so, we will get this the divide by 5 with 50 percent duty cycle based on the mod 5 counter over here and then the additional XOR gate sorry, additional OR gate to make fifty percent duty cycle.

So, and here you see actually we are having 1, 2, 3, 4 and 5 clock cycles. So, that is why this and this is the generated output of divide by 5 with 50 percent duty cycle ok. So, now, this is the technique for designing any; that means, the clock divider circuit by not in the power of 2 by 3 or by 5, by 6, by 7, by 9. So, we will see up; that means, we today we have seen divide by 3 and divide by 5.

Again in next class we will see how to design the other clock divider circuit where we can use different value like 6, 7, 9, 10 so, something else how to design them and all of them with 50 percent duty cycle ok.

Thank you for today.