Architectural Design of Digital Integrated Circuits
Prof. Indranil Hatai
School of VLSI Technology
Indian Institute of Engineering Science and Technology, Shibpur, Howrah

Lecture – 63
Low Power Digital Design Tips (Contd.)

Hello everyone. Welcome to the course on Architectural Design of ICS. So, in the last class we are seeing this Low Power Design Tips. So, initially we have discussed why we need to consider about this power consumption in VLSI circuit design and then what are there actually the sources. So, the power consumption sources are there in digital CMOS design.

So, we have we have already seen that there are two type of power; one is the dynamic power another one is the static power. In dynamic power you are having two type of power; one is this switching power and another one is this; the internal power and in static power you are having the leakage power.

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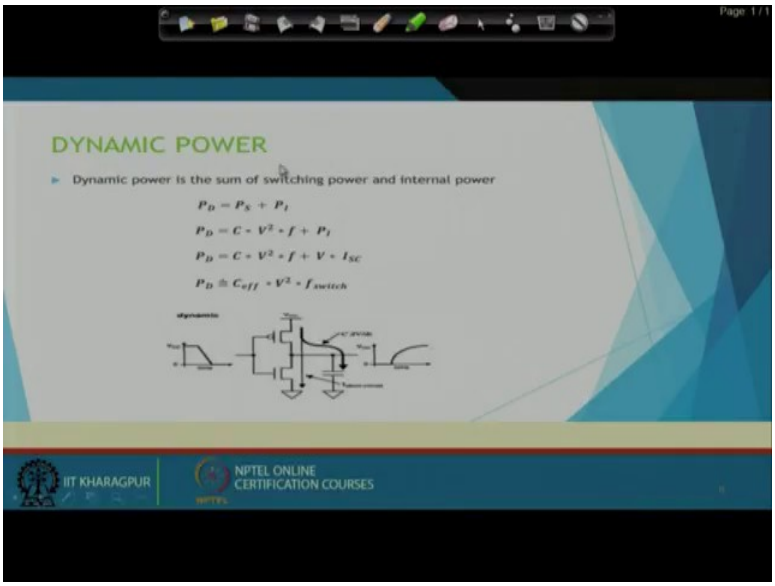

So, now we will see that the corresponding equation for dynamic power. So, as we have already discussed that dynamic power is the sum of the switching power and the internal power. So, if I just write that equation in the equation form if I just write, then P D the dynamic power consumption will be the PS is the switching power plus this PI is the

internal power. So, the switching power I can write that is C V square f and the PI is V into I SC, I SC is the short circuit current.

So, the total power will be C effective star voltage square into f switching. Why? Mainly actually this particular contribution of this internal power is very much low in compared to the dynamic power contribution to the overall dynamic power consumption. So, that is why it is not equal you can write that as this is the major contribution. So, that is why you can just omit, this particular term this will be in let us say in nanowatt; where whether this would be in milliwatt switching power should be in the range of milliwatt.

So, this actually this short circuit current is basically whenever you are having this ground to sorry this power to ground one connection for a short time. So, which creates this short circuit current and being because of that short circuit current, you will get this voltage into short circuit current as the internal power source.

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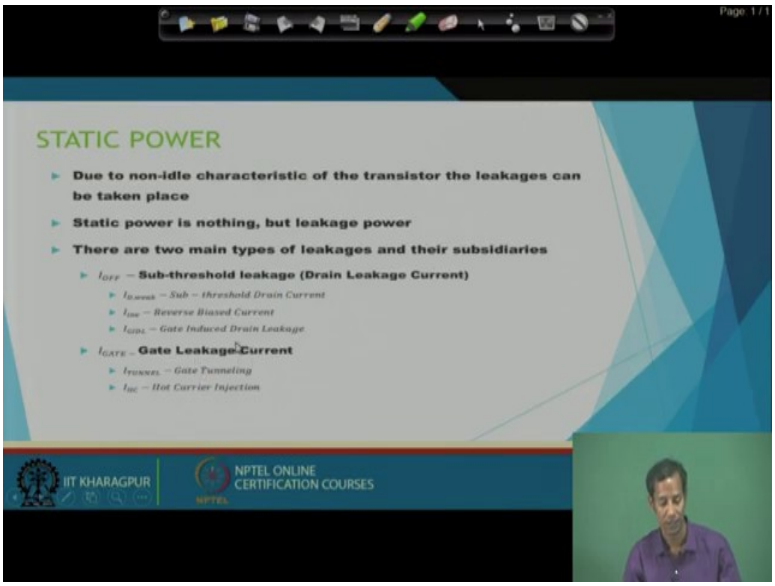

Then, the static power, the static power consumes due to non ideal characteristic of the transistor that leakages can be taken place. Static power is nothing but leakage power. And there are two main types of leakage and their sub subsidiaries. What is that? That is I OFF and I gate then what is this I OFF is that, that is the sub threshold leakage or this drain leakage current. This I OFF basically mainly depends on the contribution of this ID weak which is the sub threshold drain current, I invert which is this reverse bias current

and I GIDL which is gate induced drain leakage. So, all these currents are basically if you know more about the CMOS device ok.

So, at the time you might be actually the semiconductor device, if you know then you will be finding that these are the; that means, the currents which are already there as we are choosing the VLSI circuit design on CMOS technology. So, whenever we are basically reducing that; that means, the gate length day by day, to let us say nowadays a 3 nano meter people are trying. So, whenever we are reducing this particular gate channel length. So, this power consumption is becoming dominant day by day ok.

So, then the other power consumptions actually the other power consumption is that, this gate leakage current which actually happens because of this I GATE I tunnel which is nothing, but the gate tunneling and I HC which is the hot carrier injection. So, all these are because of the properties of this CMOS device what we have chosen for VLSI this circuit design.

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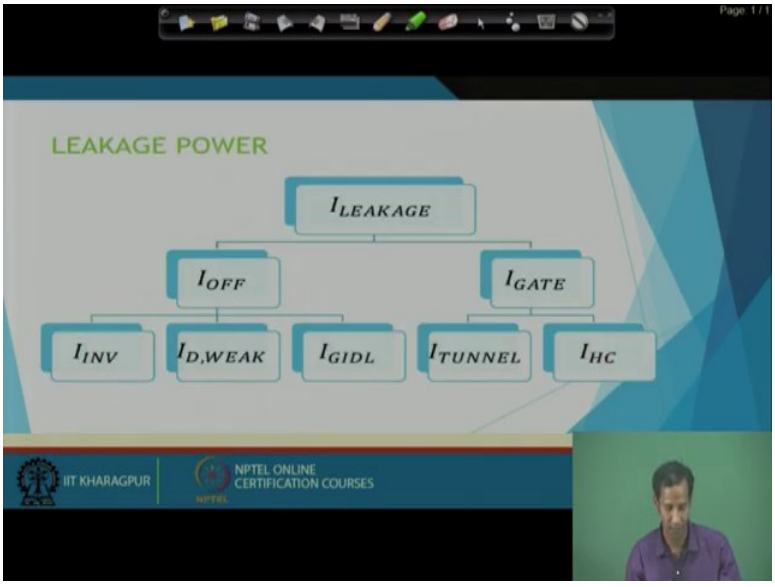

So, if I just actually make the chart so, then I leakage it is having I OFF plus I GATE ok. So, I OFF contributes is the summation of the contribution from I inverter reverse bias current ID weak that is the sub threshold drain current. And then, I GIDL GATE induced drain leakage current then the I GATE current is basically the tunneling current gate tunneling current and the hot carrier injection current.

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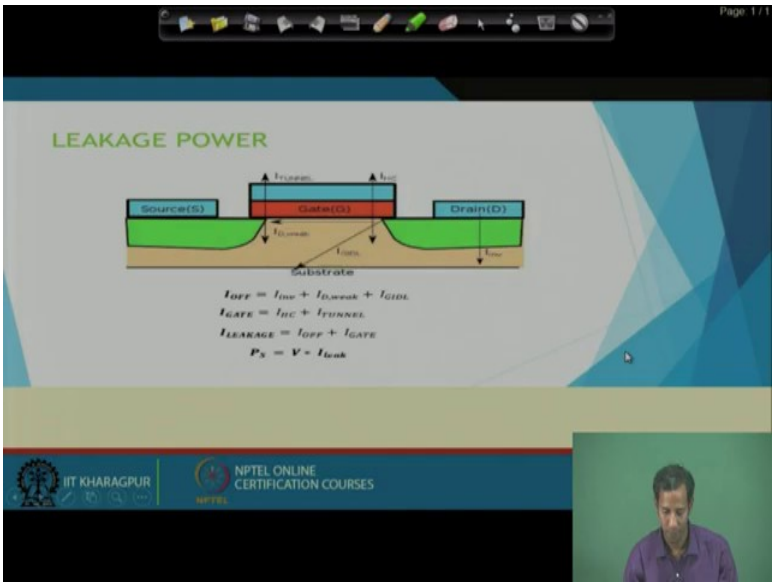

So, actually what happens is that, because of this at the gate level we are getting this ID week, which is the sub threshold current then at the gate again in this particular day extend the tunneling is happening. So, because of that this we will get this gate tunneling current and then we will get it because of this actually body we will get one current consumption which is nothing but this I GIDL gate induced drain leakage current. And then we will be having this I inverter which is this reverse bias current and then we are also having I HC, which is the hot carrier injection current.

So, all of these actually contributes to the nothing but the I leakage. So, the power consumption will be the voltage into high leakage. So, then this I leakage which is the contribution of several other; that means, that the contribution from this reverse bias current or this GIDL or HC or this I inv; that means, reverse bias current. So, because of this technology scaling this I leakage is becoming more and more day by day. So, which consumes this leakage power consumption to be a major concern which we should consider while we will design our system.

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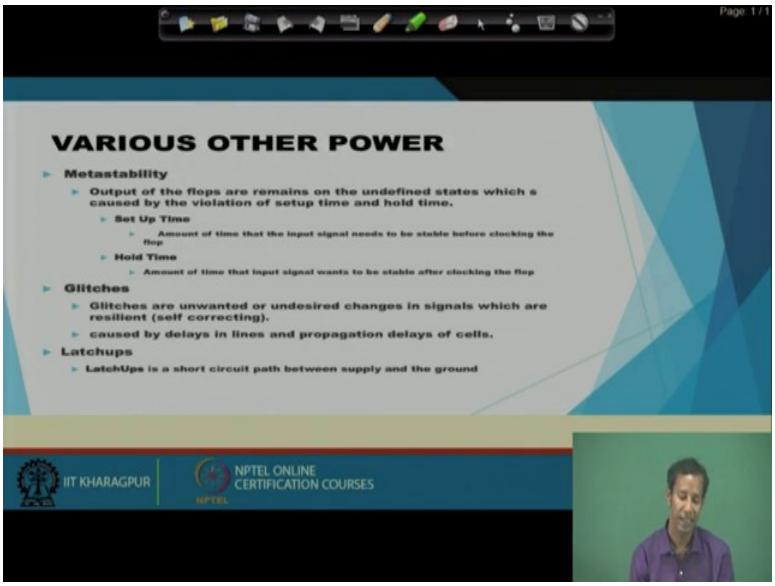

So, then there are other actually various power one of the power is that meta-stability. So, output of the flops remains on the undefined state, which is caused by the violation of setup and hold. So, we know what is the set up and hold and in digital systems, when we can get this meta-stable state, that also we have already seen ok. So that means, if we get 1 meta-stable state in in is digital circuit design so, at that time it can creates a lot of power consumption into the circuit.

Then actually we will be having these glitches. Glitches are the unwanted or undesired changes in signal, which are resilient or self correcting caused by the delays in lines and the propagation delay of the cells. That means, the delay actually this glitch we have already seen glitch how we can actually because of the delay of the gate or delay of the net between two if two signals are basically arrives at the gate inputs at different time.

So, at the time they may cause some of the glitch. So, glitch in a digital VLSI system design that is not at all appreciable; because we have already seen that in case of the what type of hazards we are having or we can get whenever we do this this logical optimization or something like or this gate level optimization. So, at the time we can get these glitches which can cause or which can totally destroy the circuit's performance very badly. So, that is why this glitch also contributes some of the power consumption in the overall power consumption of your circuit design.

So, then the latchups, latchups is a short circuit path between the supply and the ground ok. So, these latchups are basically what we consider as the internal power. So, this is the contribution from the it will if latchup happen. So, at that time it will contribute to the internal power of your systems design.

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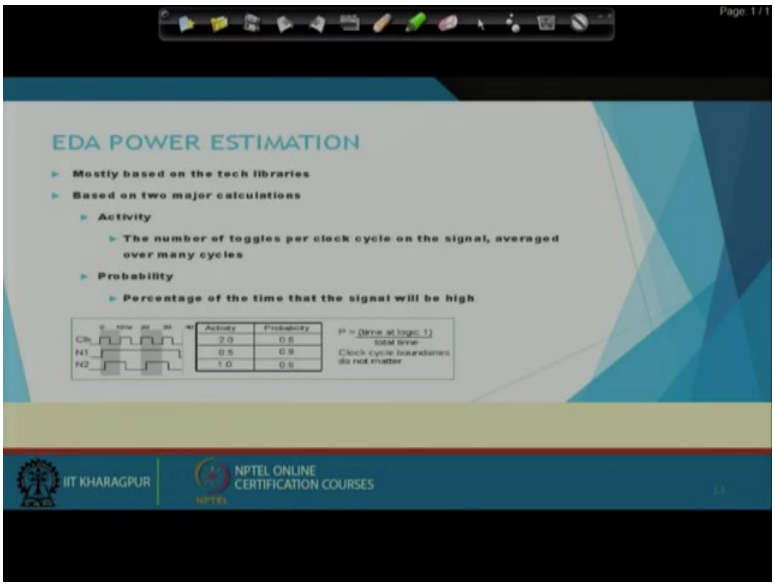

So, the power estimation mostly based on the tech libraries ok; that means, how the EDA tool suppose in EDA tool how they calculate the or how they estimate the power. Mostly it is based on that technology library and based on two major calculations; one is this activity and the second one is the probability. So, what is this activity? Activity is the number of toggles per clock cycles on the signals and averaged over many cycles.

Then, the probability is the percentage of the time that the signals will be high. So, based on these two approaches actually this activity as well as this probability they calculates the overall power consumption of your total circuit. And actually this is the rough estimation which has been done on the beforehand. But in actual power consumption which is happened whenever you will develop the IC or you will get the IC in the physical form ok.

So, suppose here we are having one clock signals how period let us say 10 nanoseconds and we are having two signals N1 and N2. So, at that time we have to; that means, set the activity as that ok, the number of toggles per clock cycles on the signals. So, the number of toggles means this N2 is basically toggling 2 times and the then actually the

probability is the percentage of the time that the signals will be high ok. And then here activities for N1 signals what is the activity; that means, for how many clock cycles it is toggling that we have to check, then depending on this particular equation.

Now, we can calculate or the tool basically calculates the rough estimation about the power consumption ok. So, this is how in EDA tool basically does the power consumption.

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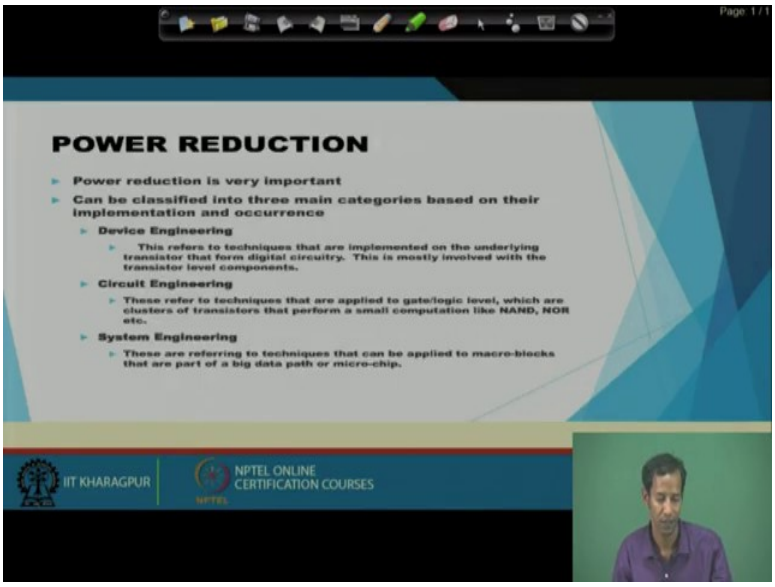

Then actually whenever we got the information about the power consumption then we have to also be thinking about the power reduction technique. So, why I have already discussed or I have already told that, I need to be actually design the circuit in such a way. So, that the power consumption should be lower and the device can run for a very longer time or the system design which we have designed that is much more beneficial to the users.

Whenever we design in the system that will be actually we design the system intended to towards the users. So, whenever the users will be benefited by reducing the power or they can get the benefit in terms of their electricity bill or they can run; that means, for a longer time the device once they charge and then they can run for a longer time.

So, that type of device we should be focus on for designing. So, that is why we have to know once I know that ok, this is the power consumption of my circuit. So, at the time

can I basically reduce the power consumption? So, what are the things we have to know for reducing the power? So, power reduction techniques are very much important and can be classified into three main categories based on their implementation and occurrence.

What are they, the device engineering the circuit engineering and the system engineering? So, the device engineering means actually the what we can say is that in VLSI design flow actually you are having this let us say this physical layout and then we will be having this gate in; that means, gate level information you will be having that this device level information.

So, every of this level, transistor level, then the device level. So, every of this level you can apply the power reduction technique. So, that is why this in device engineering also how we can apply the; that means, power reduction technique; this refers to the technique that are implemented on the underlying transistors that form digital circuitry this is mostly involved with the transistor level components ok. So, the transistor itself because as you can see that transistor itself it is having so many power factors like this I GIDL then ISC I HC I inverter.

So, these are the so, if you can improve the device performance ok, so, then at that time that power particular power reduction you can do or that low power you can do; that means, a leakage power reduction you can do. Then the circuit engineer not only leakage power the main the sort; that means, the switching power also you can do while you are working with the device level engineering. Then, the circuit engineering refers to the techniques that are applied to gate level or logic levels which are clusters of transistor that performs a small computation like NAND, NOR etcetera. That means, while you are designing this basic cell of the standard cell if I say.

So, at that time you can apply this circuit engineering or you can apply the low power techniques to make. So, the lower level if you can achieve the power reduction let us say by factor of x and those transistors or those gates will be used in your main system for million times or 1000 times or 10,000 times. So, 10,000 times advantage you will get, while you are basically reducing the power at the device level or at the circuit level ok. So, and you will go up in the VLSI design flow. So, the more actually this less reduction you can achieve in system design sorry in power consumption. Then in system

engineering these are referring to the techniques that can apply to the macro blocks that are the part of a big data path or microchips.

So, for the like whatever actually we are seeing that architectural optimization of each of this block; let us say adder then the multiplier then the divider then this codec block then the FFT block. So, all are basically intended that architectural changes these are like micro; that means, the macro blocks bigger blocks.

So, there also we can change something some architectural changes or some; that means, logic level changes to make that thing useful for low power application.

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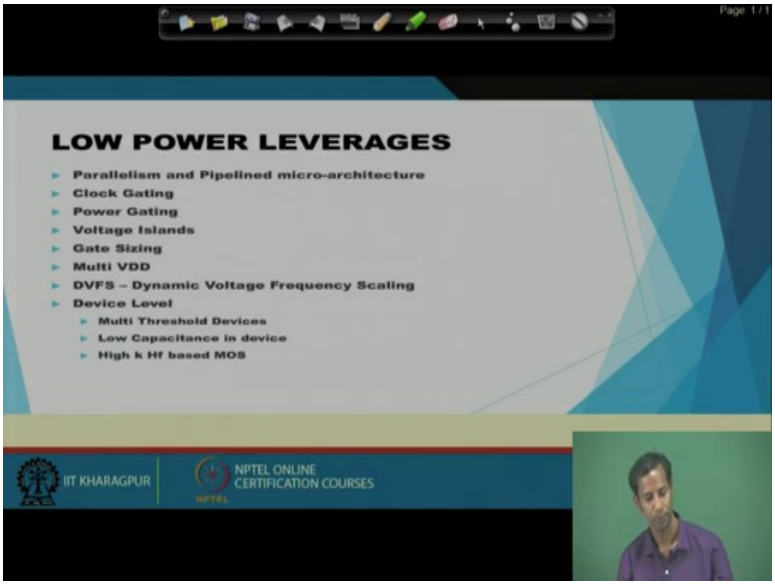

So, other actually the low power techniques there are several techniques to achieve this low power is that one of this; that means, major techniques we use is that parallelism and pipelined micro architecture. Then, there are clock gating options, there are power gating options, there are voltage islands, there are gate sizing, there are multi VDD approach, there are this DVFS Dynamic Voltage Frequency Scaling.

And, in device level you are will be having this multi threshold device, low capacitance in device and high k H f based MOS. That means, not only this generic CMOS with high k of actually the CMOS device at the time it will be changed to reduce the corresponding circuit; that means, to reduce the corresponding power at the device level.

So, if we can use or if you can reduce the power at the device level means what, we can achieve the power consumption advantage in a bigger way; rather than we are doing the at the top level which is the system level optimization for the power ok. So, then this this multi VDD or this gate sizing these are the circuit level power reduction techniques whereas, this parallelism pipelined or the clocks gating these are the system level power reduction technique that we can apply.

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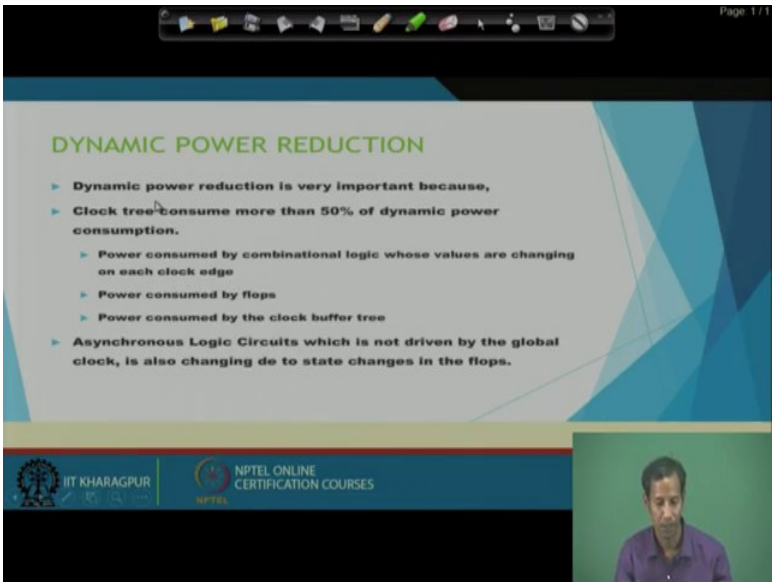

So, then dynamic power reduction. Dynamic power reduction is very much important because the clock tree path consumes more than 50 percent of dynamic power consumption. And, power consumption by combinational logic whose values are changing on each clock edge power consumed by flops power consumed by the clock buffer tree. Asynchronous logic circuit which is not driven by the global clock is also changing due to the state changes in the flops.

So, all these are basically the source of dynamic power. Now, one point is that clock tree consumes more than 50 percent of the overall dynamic power contribution why? Because the power is basically distributed throughout your entire chip and this clock tree is one of the; that means, path which will be; that means, active for all the time inside your chip; because clock is continuous to your system ok. So, continuous system means it will be continuously supplying the corresponding clock signals to the all the sequential element in your circuit.

So, that is why so, clock signal means what? Depending on the; that means, frequency we have chosen sometimes it is 1 sometimes it is 0, sometimes it is 1 sometimes it is 0. So, there is switching continuous switching in the clock signals and it is basically supplied to the clock tree network is distributed throughout your entire chip. So obviously, it will create it will consumes more power dynamic power.

So, that is why this statement is written as the 50 percent of the dynamic power consumption because consumes because of the clock tree buffers sorry clock tree synthesis. And then some of the combinational logic if you are actually if you run the combinational logic. So, at the time combinational logic means what? Whenever the inputs are available at the; that means, input end immediately the output changes its behavior ok. There is a lot of state the output depending on the logic the output state changes ok.

So, which again creates the switching very fast in combinational circuit, but whereas, these flip flops they has to wait for the clock. So, when the clock edge occurs then only it actually switches the data otherwise it remains silent or remain idle. So, but the each every flip flops and or this clock tree buffer they also consumes the power which contributes to the overall dynamic power consumption of the circuit. So, then one of the major technique to reduce this power consumption is this clock gating. So, what I say is that that dynamic power consumption clock three synthesis is the major contribution of overall switching power.

So, that is why if we can kill the switching, that all the time actually though the circuit is in the idle mode, but still I am supplying the power which is unnecessarily consuming the power. So, that is why to kill that if we use the circuit technology which is named as this clock gating clock gating means what? Whenever I need; that means, the device is in idle state the clock is also idle, the device is in an active state the clock is active. So that means, every of the clock and every flop the clock signals of the sequential element now they will be gated with one enable signals; the clock will be now enabled which is known as this gated clock.

So, the major clock gating is the major dynamic power reduction technique as we can reduce the clock tree say; that means, clock tree power consumption to a great extent; that means, we will; obviously, we can reduce the dynamic power consumption to a great

extent. And gate the clock as much as the flip as the flip flop which is not necessary to be toggled, otherwise in every clock cycles flop will toggle and dissipate more power. Local clock gating has a new enable to every flip flop where clock gating is necessary. But with complex VLSI design it is not sustainability use local clock gating, we need to derive a logic for new enable with the current logic.

So, sometimes what happens is that you can actually do this local clock gating. Local clock gating means some of the sub block or sub-sub blocks also you can do the clock gating locally to that means, place them in the dormant mode whenever they are not functioning. So, but in in in present days; that means, complex VLSI circuit design it is very much hard to find out those blocks and then again do the local clock gating ok. So, that is why it is not that much easy it is not that you cannot do it is impossible to do it that is not that much easy.

So, if you can identify and then you can you can just do the local clock gating then you will get the advantage in the overall dynamic power consumption ok.

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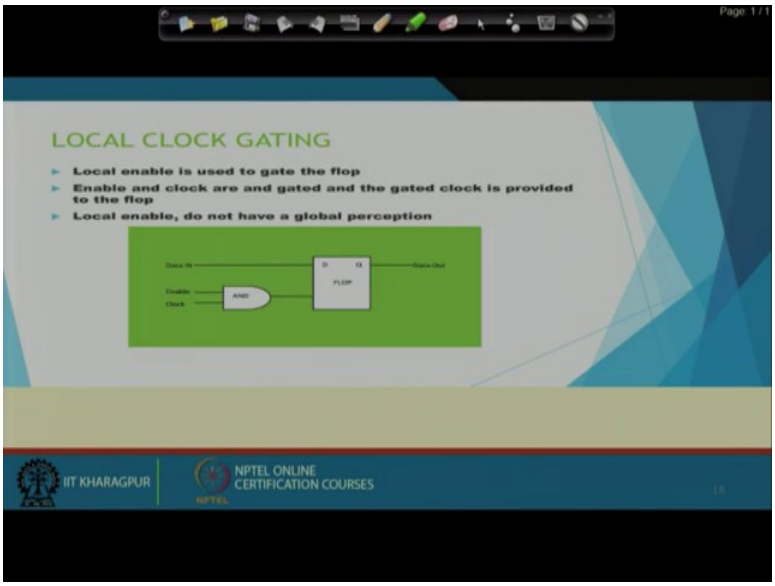

So, what is this local clock gating is that, local enable is used to get the flop and enable and clocks are AND gate and the gated clock is provided to the flop. Local enable do not have global perception; that means, what? This particular enable signal will be actually enable signals when this enable signal will come? This enable signal will come depending on the corresponding.

Let us consider one particular example that, suppose we are having one let us say one this system on chip, which is having this video processor as well as the audio processor; that means, video processing block audio processing block and then we are having some let us say this other processing blocks.

So, if one condition applies that whenever this video processing block is working at the time, the audio processing block that may not be active. So, at the time I will not activate suppose we are using only the video we are focusing only or where we are working on the video processing block, we do not need to activate the audio processing or it will be never used. Whenever I use video processor so, at that time I will be never using the audio processor block.

So, at that time instead of using this audio processing block; that means, inside of the chip what will happen the as the power supply is already or the clock or everything is already there. So, it will be also activate and it will contribute some of the power consumption to the overall dynamic power consumption. So, at the time what I will use I can say that for this particular condition, whenever I really use video processor. So, at the time you kill or you shut down the total audio processor block.

So, that the power consumption becomes very much minimal at that time. Because we have so, at that time this local enable signal will be activated, whenever I put this condition that whenever I will use video processors at the time you please stop the clock connections to all the blocks which are available in audio processor.

So, this is just one example it is not that the whenever I will use video processor so, at that time I have to reduce I have to stop the audio processing it may happen. So, that is the example of local clock gating. So, this is how actually we do the local clock gating in digital circuit design ok.

So, at the time the enable signal will be local, it is not it will be not globally or it will not be the enable signal which we have used in the top module block or the main module block ok. So, this clock gating is one of the techniques which is majorly used for dynamic power consumption reduction. Later on again we will see the water there the other techniques to reduce the power consumption.

Thank you for today's class.