Architectural Design of Digital Integrated Circuits
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Lecture – 64
Low Power Digital Design Tips

Hello everyone, welcome to the course on Architectural Design of ICs. So, in the last class we have seen that the major contribution of the power consumption related to the dynamic power consumption ok. So, that is why we have that clock gating technique and this clock source is a 50 percent of the major contribution of the dynamic power consumption.

So, that is why we have used to reduce the corresponding dynamic top power consumption. What we can use? We can use one technique which is named as clock gating technique to reduce or to that means, minimize the dynamic power consumption by reducing the clock network power consumption.

So, at the time we have seen some of; that means, the local clock gating also we can do; that means, the overall actually the top level also we can do some clock gating, but in local clock gating also it is possible. So, but the problem with these recent trends or the recent VLSI design is that it is so much complex. So, local clock gating sometimes it will be very much complicated to do that.

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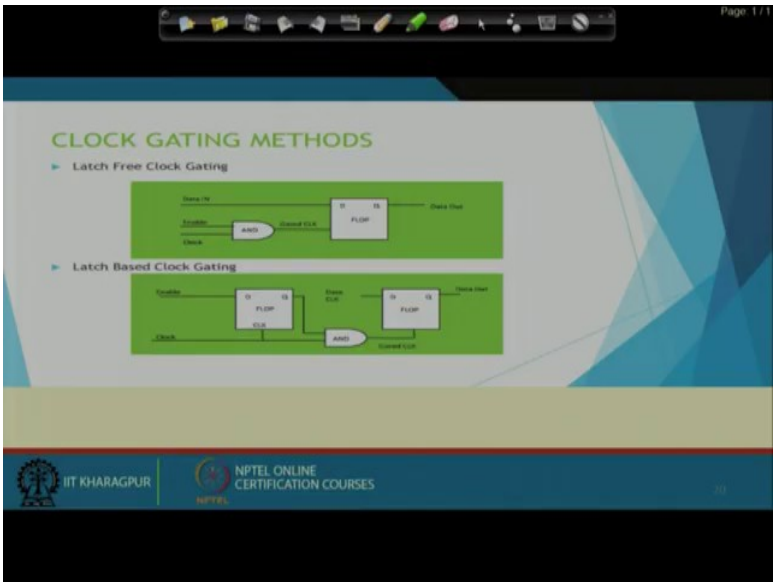

So, the clock gating methods there may be of two type 1 may be of latch free clock gating and another one will be latch based clock gating. So, as you see whenever these enable signals is coming directly. So, enable signal will be generated from some kind of combinational logic ok. So, that depending on these particular equation or these particular condition, the enable you just activate the clock gating to the corresponding flip flops. So, that will be the logic.

So, whenever these enable signal is as these enable signal is coming from one combinational block. So, at that time it must be having some of the delay or if the signals itself, if it is actually, contagious or if it is not accurate or if it is having some glitch or something else. So, at the time the whole operation should be problematic.

So, that is why we can also have the clock gating option which will be this latch base clock gating. So, latch based clock gating means the enable signals are now it is not directly coming from any combinational circuit. It is coming by passing one d flip flop and then this clock is basically and it with the corresponding enable signal and then we are putting that gated clock to every other sequential elements of my circuit design. So, this is that the clock gating method in two different approaches we can take.

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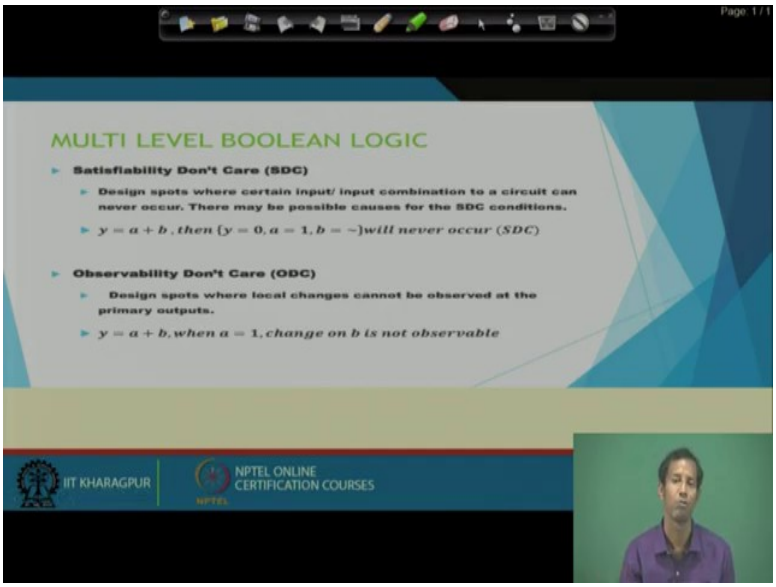

Then actually how we can do is that; if we can reduce the multilevel logic if we can optimize this multilevel logic we can also achieve low power consumption.

So, how one of these multilevel Boolean logic optimize actually why we are doing this multilevel logic optimization. So, the one of this is that satisfiability DONT care condition and another one is this observability DONT care condition. So, in Karnaugh map whenever we do this optimization of this Boolean logic using Boolean logic or you, we this logic level minimization whenever we do we generally do using K map.

So, in K map; if the if I find that that there is the DONT care. So, at the time we take common of that DONT care means if I if there is 1. So, we consider that as 1 if there is; that means, if it is making one pair with 0 s at the time we can consider that particular things as 0. But this logic minimization can create the problems of power consumption.

So, to remove that what we can do this satisfiability don't care, here the designs spots where certain inputs combine is the combination to a circuit can never occur and then there may be a possibility of causing for this SDC or this satisfiability DONT care conditions. So, it is that if y equals to a plus b then y equals to 0, a equals to 1 and b equals to; that means, don t care will never occur SDC; means what? If one of these my OR gate input is 1. So, at that time whatever is the value of b y will never be 0.

Whenever these OR gate input is 1 so, at the time these y will be 1 it does not depend on the other input. The same things happen in actually this in case of suppose this is one if this is one AND gate. So, at the time if one of the input is 0, whatever the value of the other gate? The y will be never 1, it will be always 0. So, that type of condition is known as this satisfiability DONT care condition. Then the observability don t care condition is what the design spots where local changes cannot be observed at the primary inputs; means what? Actually if I can take this particular example when a equals to 1, change on b is not observable.

So, means what this is the satisfiability so; that means, the output will never be 0 for if a equals to 1 and here in this the same thing if a equals to 1, I cannot never observe what is the; that means, state for b, whether that is 0 or 1 all the time the y should be 1 ok.

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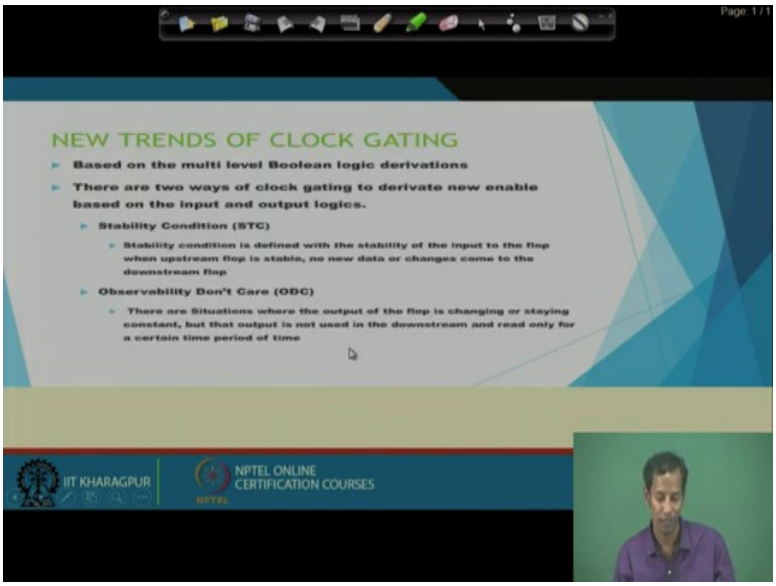

So, this is basically used for this Boolean logic, multilevel Boolean logic. So, what are the new trends of clock gating is that based on this multilevel Boolean logic derivation; there are two ways of clock gating to the derivative to derive new enable based on the input and the output logic.

The one is that stability conditions and the other one is this observability DONT care. So, what is there in stability condition? Stability condition is defined with the stability of the input to the flop when upstream flop is stable no new data or changes come to the downstream flop. And then in observability DONT care there are situations where the output of the flop is changing or staying constant, but the output is not used in the downstream or read only for a certain period of time.

So, that means, based on these satisfiability condition or observability condition we can have the clock gating options in we have divided in two category; one is the stability condition another one is this observability DONT care condition

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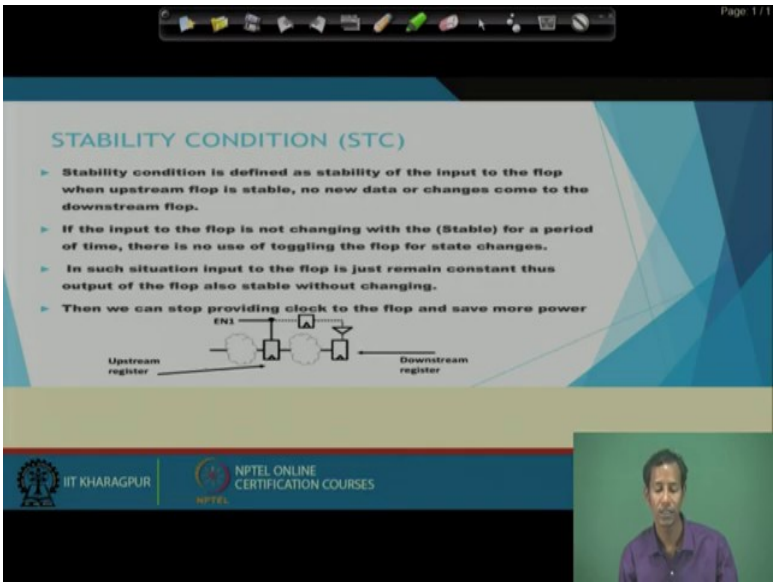

So, what is the stability condition is that; suppose, we are having the corresponding this logic something like this. So, here is this corresponding registers so, we are having these enable signals here. Now stability condition is defined as the stability of the input to the flop when upstream flop is stable, no new data or change comes to the downstream flop. So, that means; this is stable no new change is coming to the downstream registers. If the input to the flop is not changing with the stable for a period of time there is no use of toggling the flop or state changes ok.

In such situation input to the flop is just remain constant thus output of the flop also stable without changing then we can stop providing clock to the flop and save more power. Actually means what, if as the data is basically passing from these to these like as there is the connection. So, at the time depending on the activity of the upstream registers, it is not actually based on the corresponding stability condition over here I can take the decision that you do not you whether you activate these particular registers clock or not.

So, depending on the corresponding as we know that actually if I say this that whenever this particular a is 1; so, y will be never 0 ok. So, this is the satisfiability condition. So, here also if I find that this particular satisfiability will never occur; that means, the output will be never occur to 0. So, at that time we do not have to be at the time activating the downstream register which is taking the input from the upstream registers.

So, by that technique we can use or that is nothing but, one clock gating witch will generate the enable signal ok. So, this is the condition there if you find these particular condition you do not activate the little registers. So, if I can do then we can save much more power.

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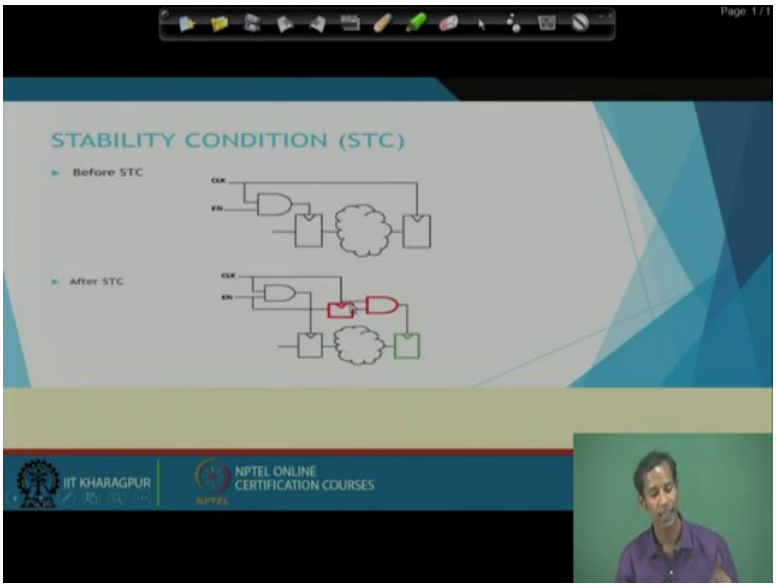

Then, you see the stability condition circuit so, suppose this is enable and then clock going to these particular these; suppose this is the clock gated signal clock gated registers. Now, after the satisfiability condition; the signals will be now it will be just this enable going to that and then again for the next registers what we have done?

We have done these corresponding clock gating based on the that one registers because of this and then we are having the corresponding and gate over here which is coming to the downstream registers that if I find that there is this satisfiability condition happens. So, at that time you do not change the clock or; that means, the clock will remain idle at that time for the downstream register or registers ok. So, by this clock gating techniques now we can save more power.

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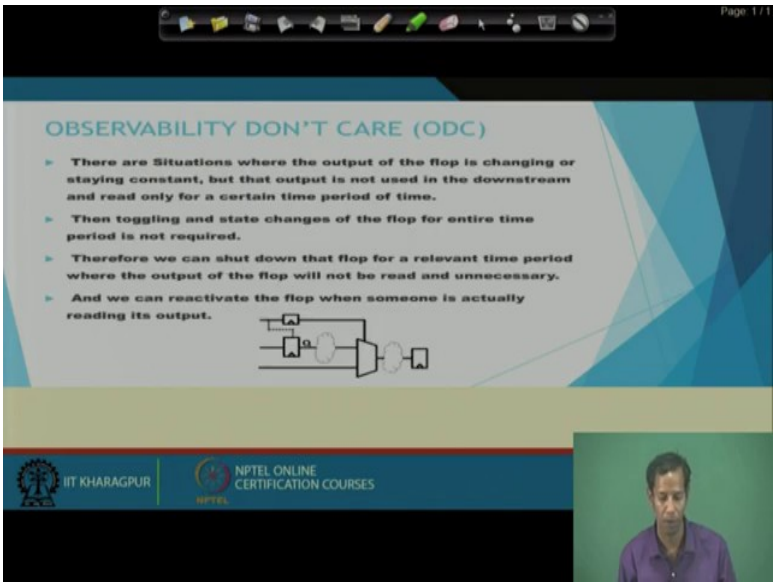

So, then observability DONT care condition; there are situations where the output of the flop is changing or staying constant, but the, but the output is not used in the downstream and read only for a certain period of time then toggling and the state change of the flop for entire time period is not required means what.

Suppose the output of the flop; that means, the primary flop it is changing, but it is changing and for the downstream it is used for a very short time. So, at the time do not actually means what suppose one of the data which is coming over here, they are basically staying constant for a long time. So, instead of in at; that means, in the next flop instead of taking the same data again and again on this; that means, every clock cycles what I can say that for this much of period the data is constant. So, you take one in for one clock cycle you take the data then you stop that operation.

Stop basically taking the data input at every of this clock to find out what is the data at every clock. By this technique; now at the time the switching activity if I can reduce for the next flip flop, at that time I can get the advantage in terms of power consumption.

So, which these particular enable signals, now I can generate based on the observability condition, I can observe that if this a is 1 so, though it is it does not depend on whether that you know or gate if a is 1, it does not basically look there like that whatever is the condition of whatever is the signal for b, I do not have to look about.

If I find that a is 1 so, automatically y will 1 assigned to 1. So, by that type of technique these observability condition that is observed I observed that this is the phenomenon and based on that I am taking or I am generating the enable signals to stop the other registers. And therefore, we can shut down the flop that are relevant time period where the output of the flop will not be read and read any unnecessary data and we can reactivate the flop when someone is actually reading it is output; that means, whether whenever that output is basically changing or it is reading.

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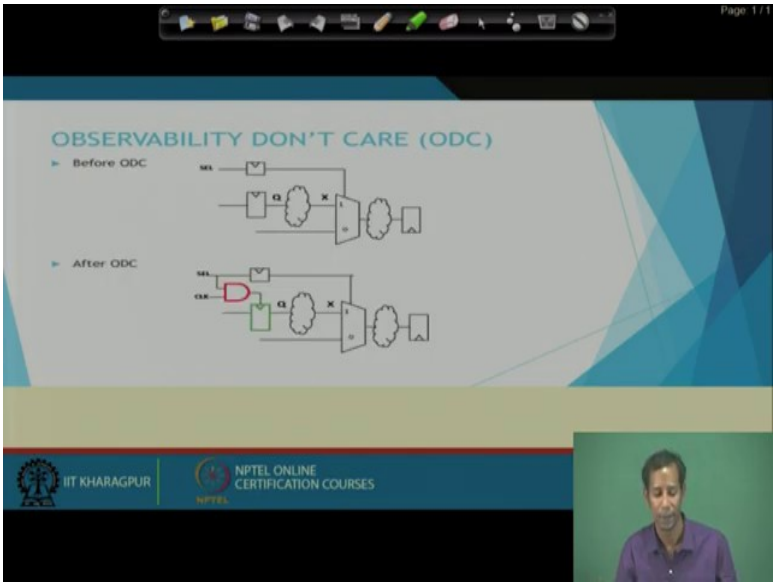

So, if I see the corresponding architecture, here this is before this observability DONT care. So, after observability DONT care is that we have to consider this select ANDed with this clock and then again it is going to the corresponding registers. So, these registers is enabled that ok. So, you take the corresponding input whenever there is some enable condition based on the corresponding lines over here or the signals over here.

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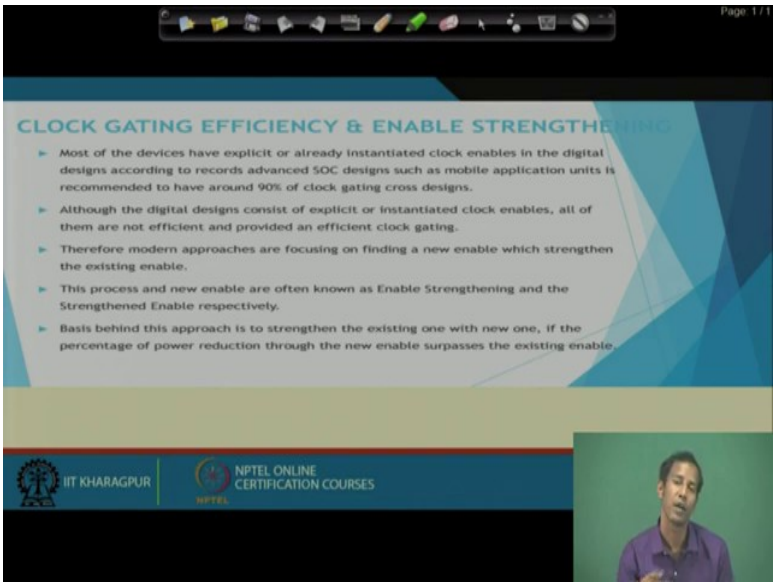

So, by this satisfiability DONT care condition or observability DONT care condition we use we apply that along with this clock gating technique and we can achieve or we can save much more power in dynamic power consumption. So, then this clock gating efficiency and the enable strength is that most of the devices have explicit or already instantiated clock enables in the digital design according to records, advance system on chip design such as mobile application unit is recommended to have around 90 percent of clock gating across the design.

As this clock gating is the; that means, major technique which we apply to reduce the dynamic power consumption. Although the digital design consist of explicit or instantiated clock enables, all of them are not efficient and provided an efficient clock gating. Therefore, modern approaches are focusing on finding a new enable which strengthening the existing enable.

So, these process and new enables are often known as enable strengthening and the strengthened enable respectively basis behind this approach is to strengthening strengthen thus existing one with the new one if the percentage of power reduction through this new enable surpasses the existing enable one.

So; that means, what I say if that the earlier days we are having only single; that means, clock gating technique which is; that means, based on that enable signal. Now you can enable or the clock get every of this. Now what we can do? You can local clock gate based on this satisfiability condition or this observability DONT care condition. Now you can make new

enable signals to make the clock; that means, to make the clock gating technique more efficient for power reduction.

Then again you can actually have you can generate more efficient way that what will be the enable actually in it says that in nowadays in mobile processor 90 percent is basically 90 percent of the sequential elements are used this clock gating techniques to reduce the power consumption because this in mobile your you need the power consumption very much low.

So, we have to find out the new techniques to do this clock gating enable signals generation so that, we can reduce the power in a better way.

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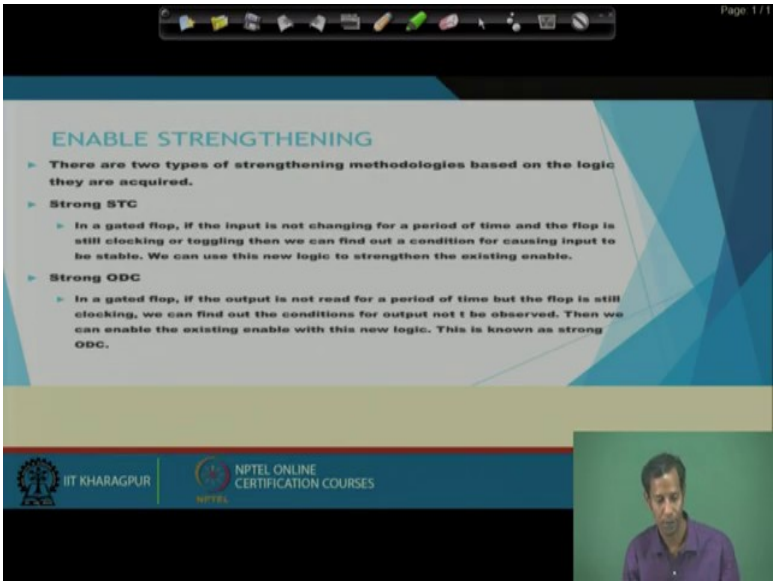

So, then what is these enable strengthening? So, enable strengthening is that there are two type of strengthening methodologies based on the logic they are acquired. Strong STC and strong ODC. So, what is that? Strong STC is the satisfiability this STC is the stability condition based on the satisfiability DONT care condition and this strong ODC is the strong observability DONT care condition.

So, the strong STC says that in a gated flop if the input is not changing for a period of time and then the flop is still clocking or toggling then we can find out a condition for causing input to be stable and we can use this new logic to strengthen the existing enable. So, in strong ODC what you can do is that in a gated flop if the output is not read for a period of time, but the flop is still clocking we can find out the condition for the output not to be

observed. Then we can enable the existing enable with the new logic this is known as strong ODC.

That means that; this STC and ODC whatever we have used we can strengthen or we can generate one new enable signals to make sure that these particular enable signals is depending on these condition. For STC if the input is not changing for a long time and in ODC if the output is not reading for a long time. So, at the time I can just say that you please stop the clock at this particular flop. So, that it will remain just silent or it will remain idle. So, that the switching activity will never happen and it can reduce the dynamic power consumption.

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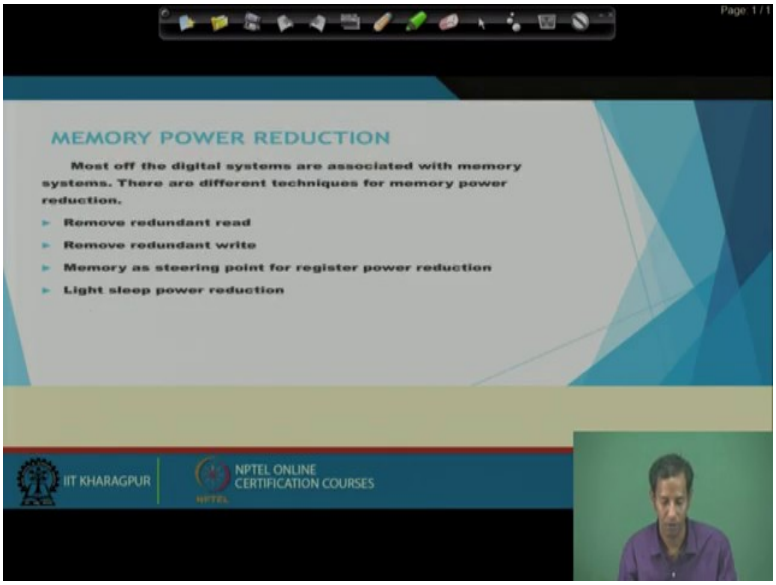

Then another approach in digital system is the memory power reduction. So, why memory power reduction in most of the case the memory reading and writing they are the major source of power consumption, because the memory blocks are very much power hungry. So, that is why if we can; that means, reduce the memory power consumption, then also we can get; that means, the reduction in the overall power consumption.

So, how we can get the memory power reduction? We can get the memory power reduction in different techniques like, remove the redundant read, remove redundant write, memory at steering point for the register power reduction and light sleep power reduction. So, these are the techniques or these are the methods which we use to reduce the memory power consumption.

So, I said that for reading and writing the memory, we actually consume lot of power. So, if we can remove the redundant power which is unnecessarily if I read or if I write something on the memory. So, if I can remove that at the time I can achieve more power reduction at the thing at the VLSI circuit.

So, we will see one of the examples where this particular thing is very much necessary. Because recent days, VLSI system design all of the VLSI systems design said they need innovation at these kind of things; that means, how we can generate or how we can using new techniques how we can reduce the power consumption or how we can reduce the are consumption or how we can improve the speed of operation.

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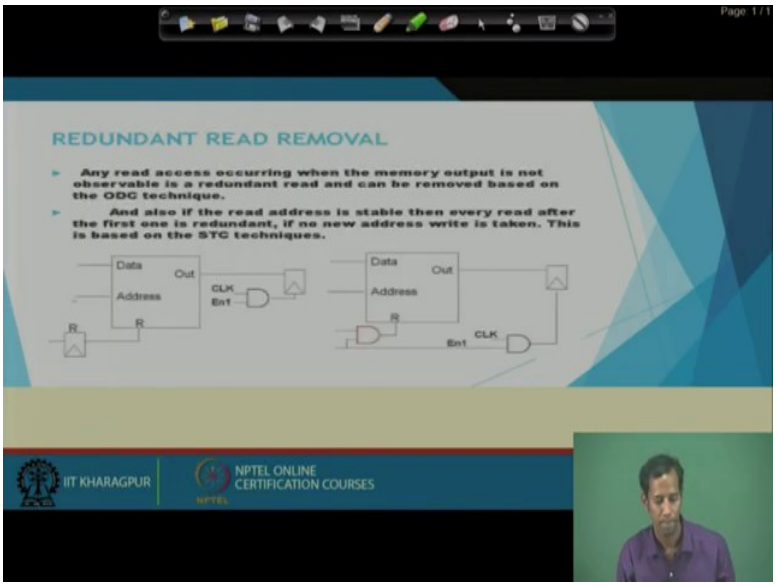

So, how you can do this redundant reads removal is that suppose, this is the actually memory and now if you just this address if the address is already gated with some enable signals. So, this is not the address, this is the R signal ok. So, what is this R is that read ok. The read signal is basically if it is gated so, it will remove the redundant read means what we put enable signal that for this particular case you read otherwise you stop reading from the memory.

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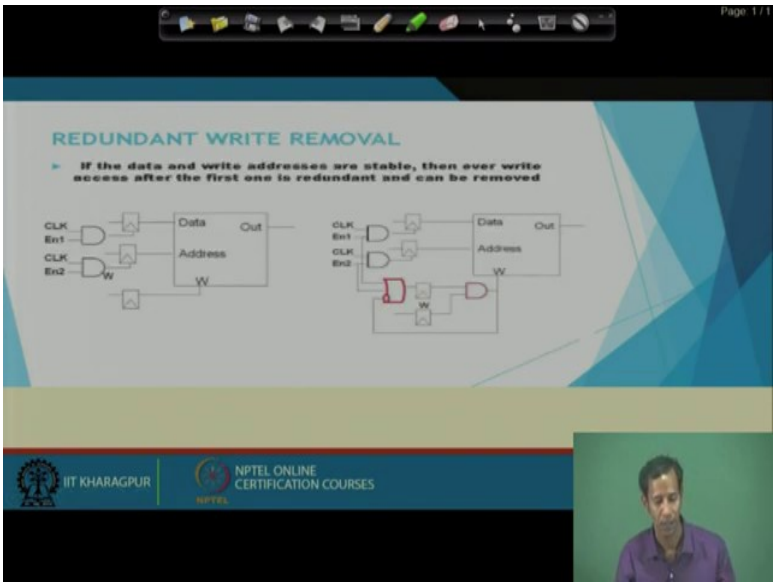

So, any read access occurring when the memory output is not observable is a redundant read and can be removed based on the ODC technique so; that means, these particular signals will be generated based on the this ODC technique which is the observability DONT care condition. So, and also if the read address is stable then every read after the first one is redundant. If no new address write is taken this is based on the STC technique.

That means by this now I can remove actually that whether because based on this ODC and STC technique I can remove the redundant read and write option in the memory. So, then again redundant write removal, how we can do this redundant write removal? If the data and the write address are stable then every write access after the first one is redundant and can be removed ok.

So, here you see this is generating these address. So, now, this write address is basically enabled with this enable 1 and enable 2 along with the corresponding the; that means, this the other condition that if this is fixed, this write address is fixed then do not write anything because only one particular location again the rewriting will cause more power.

So, once I write if the addresses remain same. So, at the time do not write the data and that this you see the data is also enabled based on this. So, actually this is the technique which we have applied for redundant write removal.

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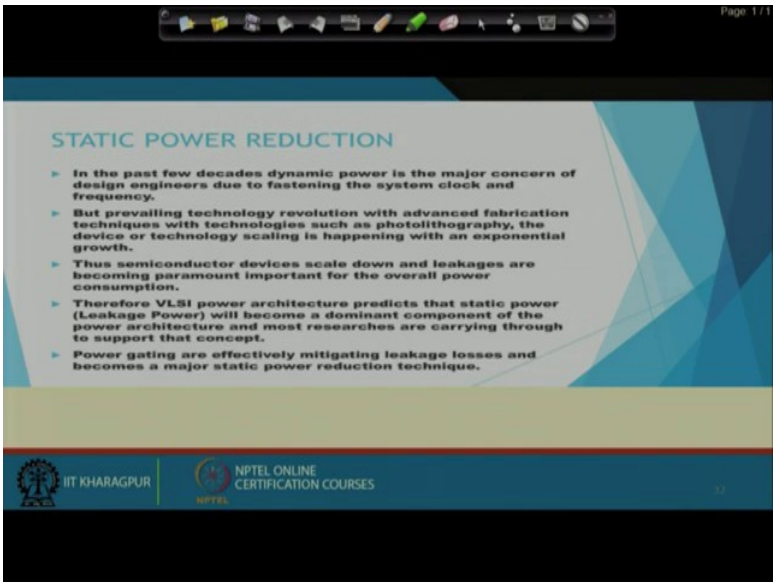

Now the static power consumption, static power reduction. So, till now we have seen the techniques to reduce the dynamic power; that means, whether there is clock gating or this memory power reduction, but here actually we will now, we will consider on static power reduction technique.

So, in the past few decades; dynamic power is the major concern of design engineers do to fastening the system clock and frequency. But prevailing technology revolutionwith this subthreshold, with this sub threshold voltage design or this; that means, the because of the technology scaling, now we are in the era of 3 nanometre ok. So, this prevailing technology revolution with the advance fabrication techniques with the technologies such as photolithography that and the device or the technology scaling is happening with an exponential growth.

Thus semiconductor devices scale down and the leakage are becoming one of the major important factor for overall power consumption. So, therefore, VLSI power architecture predicts that static power will become a dominant component of the power architecture and most researchers are now carrying through to support that concept. What actually as we have technology we are changing; that means, we are shrinking the gate length channel length means what we are basically providing more area to the design.

But accordingly whenever we are getting so, at the time we are increasing day by day we are increasing the more power consumption in the leakage in terms of leakage. So, that is why

everybody is now basically focusing on to reduce these leak, how to reduce this leakage power. So, power gating are basically effectively mitigating the leakage losses and becomes imagine major static power reduction technique.

So, there in case of dynamic power, we are using this clock gating technique, but to reduce the power consumption; that means, static power consumption we have to use this power gating technique ok. So, using these power gating technique we can reduce though actually it is becoming one major of the actually contributed to the overall power consumption of the VLSI circuit, but using this power gating now we can reduce the power to a certain extent ok.

So, what is the power gating how we can do the power gating and what are the other actually feature what are the other technique we use for; that means, this power consumption through lower the power consumption that we will see in the next class and.

Thank you for today.