Architectural Design of Digital Integrated Circuits
Prof. Indranil Hatai
School of VLSI Technology
Indian Institute of Engineering Science and Technology, Shibpur, Howrah

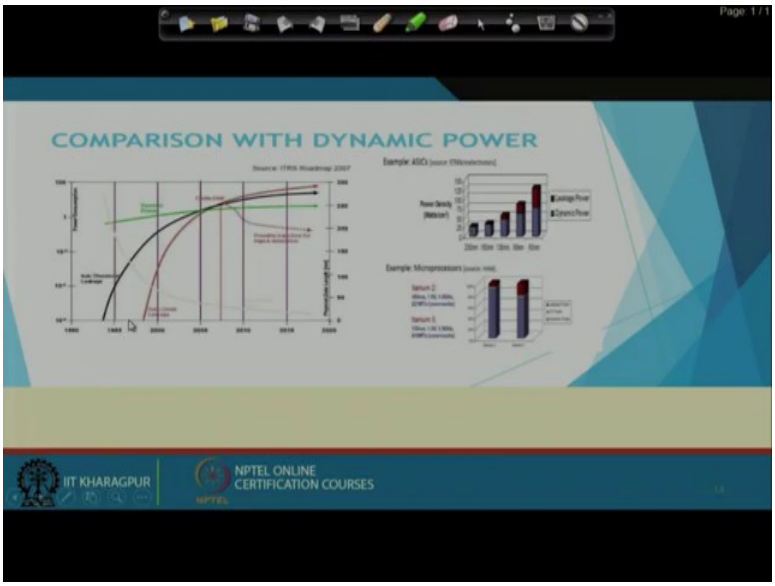
Lecture – 65
Low Power Digital Design Tips (Contd)

Hello everyone, welcome to the course on Architectural Design of ICs. So, we are basically discussing the power reduction methodology for low power VLSI design. So, we have seen that clock gating is used for dynamic power consumption reduction and then we have used some of the; that means, static power reduction technique to reduce the leakage power.

Now, actually if we see the comparison of because, with the recent days technology scaling or this voltage scaling. The leakage power will become becoming major part of this contributor to the power overall power consumption, over the dynamic power.

So, to see that actually if you see the corresponding ITRS road map so, you see that this green colour line is the actually this dynamic power consumption whereas, this leakage power consumption. They are over powering or with this dynamic power consumption.

(Refer Slide Time: 01:20)

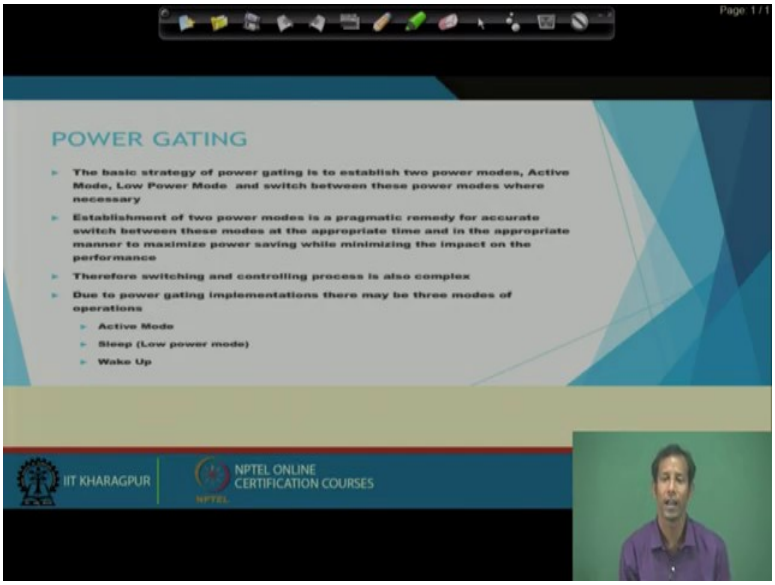


So, actually day by day if we you if I see that with this technology scaling, how this leakage power and dynamic power are becoming effective in the major power

contribution is that in 250 nanometre technology, the leakage power is very much small or it is very much trivial in compare to the dynamic power consumption.

But, with this 65 nanometre technology, you see actually this it is coming almost half-half; that means, 50 50 percent contributed to the leakage power as well as the dynamic power consumption. So, with the recent activities this is up to 65 nanometre technology with the recent 3 nanometre technology or 7 nanometre technology, if you see. So, at the time major contributor will be their leakage 1, rather than the dynamic power consumption ok.

(Refer Slide Time: 02:17)



So, that is why this leakage power reduction, we can use this power gating technique. So, what is there actually in power gating technique is that, the basic strategy of power gating is to establish 2 power modes. Active mode and low power mode and switch between these power modes where, it is necessary.

The establishment of these 2 power modes is a pragmatic remedy for accurate switch between these no modes. At the appropriate time and in the appropriate manner to maximize the power savings, while minimising the impact on the performance. And, therefore switching and the controlling process is also becoming complex. So, due to this power gating implementation, there may be 3 modes of operation, the active mode or the sleep mode or the wake up mode.

That means, actually what we are discussing is that. Nowadays, if your mobile is in use. So, at that time it consumes the power more; that means, at the time you are using the dynamic consumption is more. But, whenever your device is not used for let us say for long time. So, at that time the major power contributor is the major power consumption source is the leakage power.

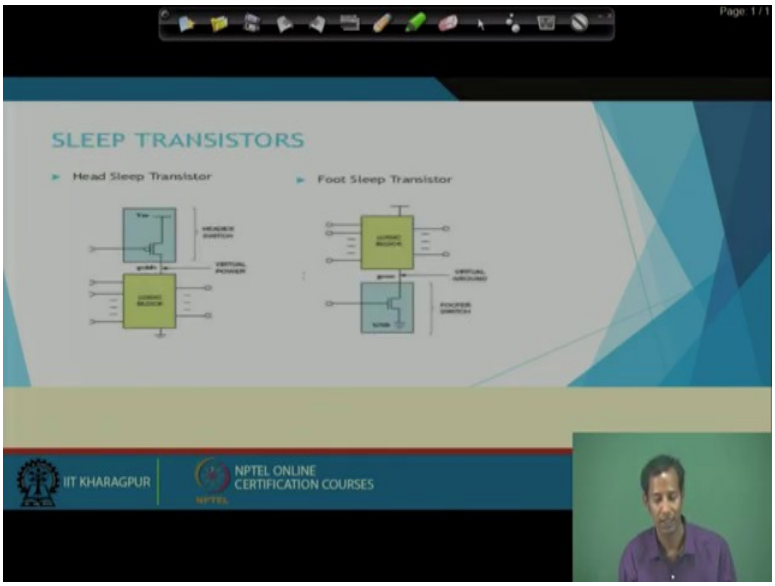
So, if you can reduce this leakage power or if you can put that and nowadays actually if you see the laptops are also coming like that or if your phones are also like that. If you just if you are not using the phones or if you are not using the laptops. So, at that time after certain period of time, let us say 10 seconds or 1 minute, the laptop or phones got into the idle mode. The display is also shutdown some of the; that means, the processing blocks also they are getting shutdown. So, why because whenever they are not in use then, why to supply the power to each of these modules.

So, that is why, if I can create 3 mode; that means, whether there is active mode or wake up mode or the sleep mode. In sleep mode means, it is in the low power mode; that means, the system is like whenever we are like we sleep. So, at that time our body part is basically working but, it is like in the dormant state.

So, it is the dormant state, which we provide in the circuit level itself. So, whenever it is not in use. So, the minimal voltage will be applied to the each of this particular device; that means, the corresponding circuits or to the corresponding gates ok.

So, that is why this power gating things we can apply whenever, we need to reduce the corresponding leakage current or this leakage power.

(Refer Slide Time: 05:19)



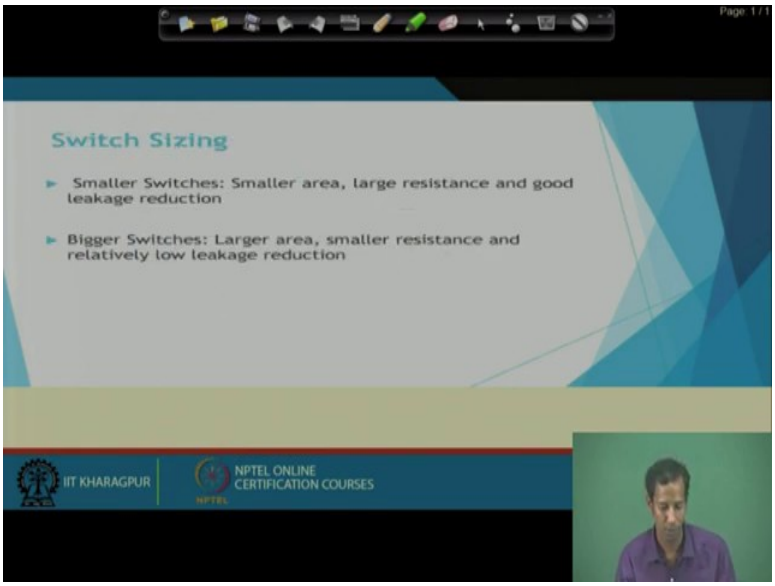
So, actually the sleep transistor is that this is head sleep transistors ok. So; that means, within this logic block, I am having one transistors which is basically connected with the VDD extra transistor, which is this connected with the VDD.

That means, whenever this mode is in suppose, if this is coming as that the corresponding it is in active mode, at that time the VDD will be connected to logic block. If it is in the sleep mode so, at that time it will be just open there will be no VDD connection, connecting to the corresponding logic block.

So, this is the; that means, head sleep transistors and for foot sleep transistors, it will be connected with the ground. That means, at the time there will be no such connection to the corresponding ground ok. So, that is why; that means, here this particular things this is the virtual power at that time, this is the virtual ground at that time.

So, putting these sleep transistors at the ground power supply as well as the ground. Now, I can make or I can activate whenever they need otherwise, it will be in the sleep mode, to reduce the corresponding power supply.

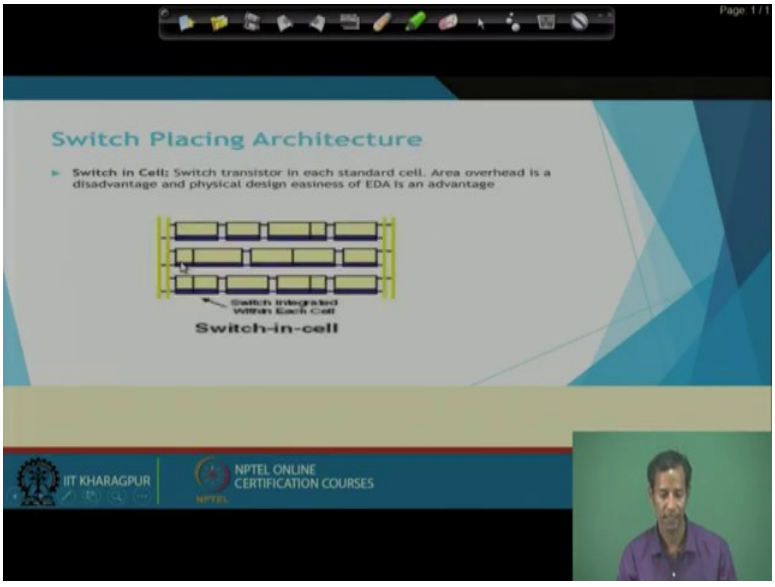
(Refer Slide Time: 06:41)



Then, another actually technique is that switch sizing so, smaller switches means smaller area, large resistance and good leakage reduction.

So, bigger switches require larger area but, smaller resistance and relatively low leakage reduction. So, that is why we will use the switch, if I can use the switch smaller switch than, I can reduce the corresponding reduction in the leakage in a great extent.

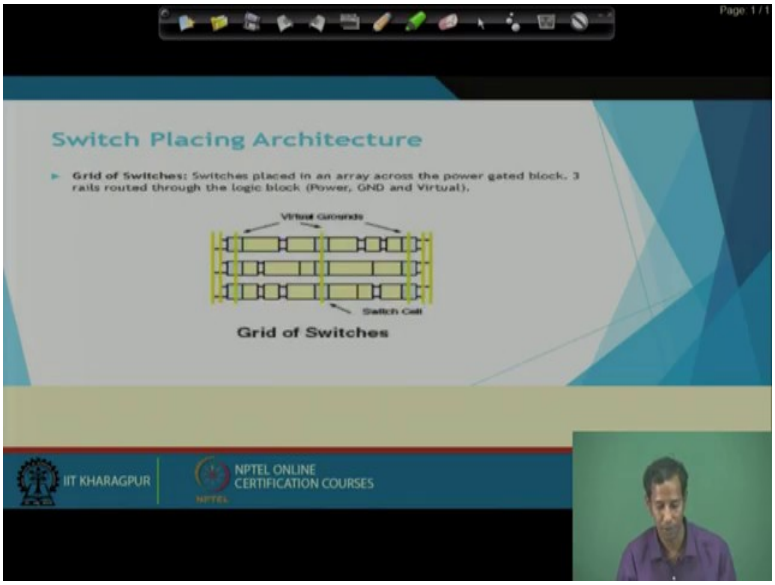
(Refer Slide Time: 07:15)



So, how in a cell how you can place the switch so, switch transistor in each standard cell area overhead is a disadvantage and physical design easiness of EDA is an advantage.

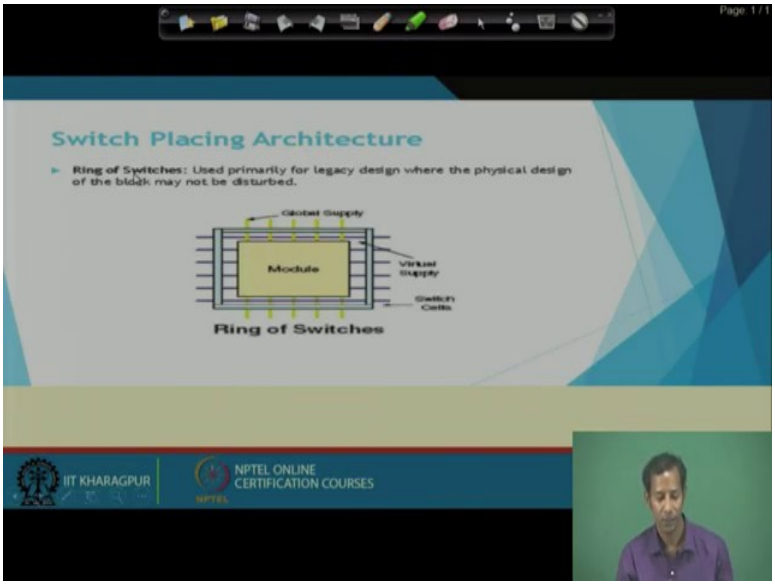
So,; that means, in every of this standard cell now, I can place this switch transistors to make it. That means, to reduce the corresponding this leakage power consumption.

(Refer Slide Time: 07:46)



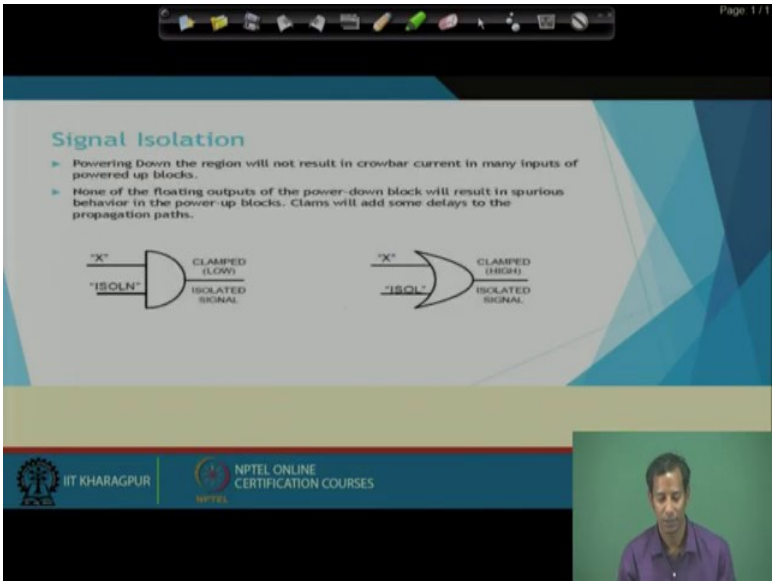
So, than we are having here this is the grid of switch, which we already placed in between this; that means the corresponding standard cell base design. So, grid of switch says that switch placed in an array, across the power gated block an 3 rails routed through the logic block. Why this is connected because, the virtual grounds or the virtual power, we have to create to make every of this blocks are like power gated.

(Refer Slide Time: 08:21)



Then, the switch placing architecture how we can place the switch so, you can create the ring of switch by putting them vertically as well as; that means, horizontally. So, the horizontal line will be the virtual supply and this is; that means global supply. And, in between of them and in between of this standard cell you can place the corresponding switch cell. So, low; that means, smaller switch cell very good reduction in the leakage.

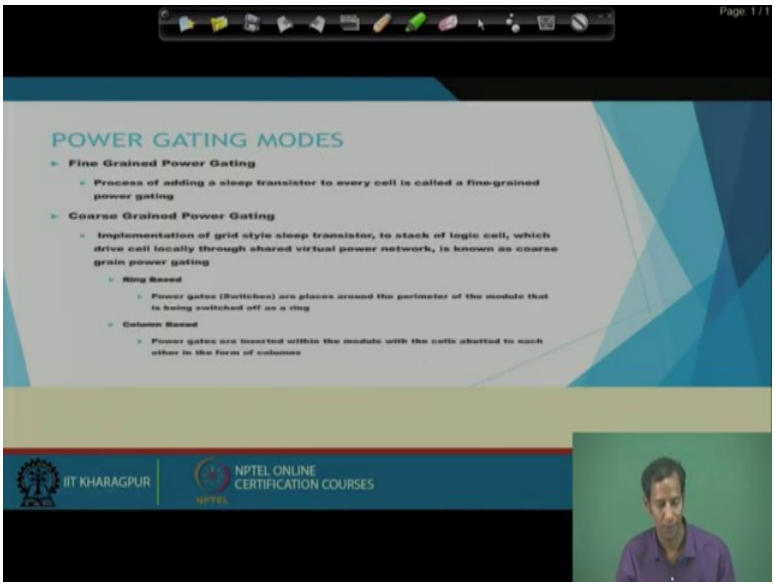
(Refer Slide Time: 08:55)



Then, actually we can do is that signal isolation. So, what is the signal isolation? Powering down the region will not results in crowbar current in many inputs of the powered up blocks. None of the floating output of the power down block will results in spurious behaviour of the power up blocks clams will add some delays to the propagation path.

So, what we are doing actually some of the; that means, blocks, if they need that signal to be isolated. So, at that time we can put this and gate by with this particular enable signal which is this isolation ok. And, then they will provide to the corresponding particular gates to reduce the power consumption.

(Refer Slide Time: 09:51)

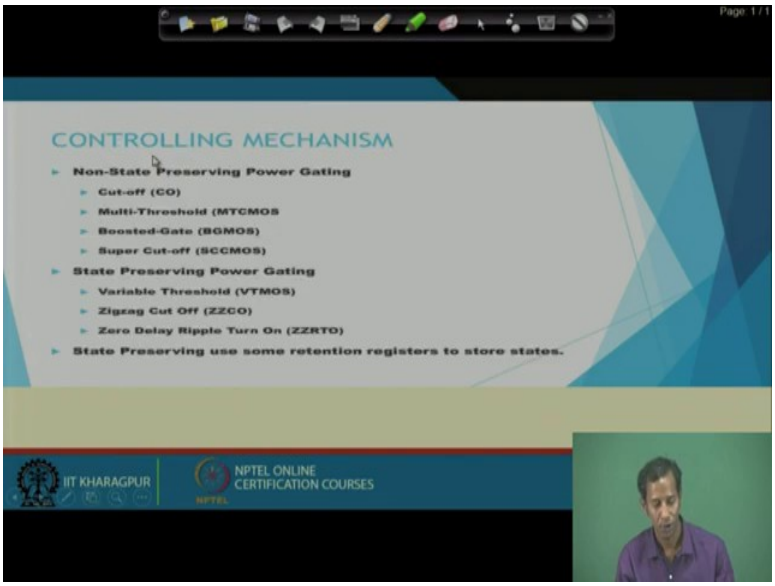


So, the power gating has different modes, the power gating modes are basically 2 fine grained power gating and the coarse grained power gating.

So, in fine grained power gating, the process of adding a sleep transistors to every cell is called as fine grained power gating. And, in coarse grain power getting is that implementation of grid style sleep transistor to stack of logic cell, which drive cell locally through the shared virtual power network is known as coarse grain power gating.

So, in coarse grain power getting, we are having this ring based and the column based. So, we have to switch actually whatever we have seen that we have to place the switch. So, we have the ring. So, this is the coarse grain power gating and another thing is that every of the cells, if it is power gated? So, that is fine grained power gating.

(Refer Slide Time: 10:45)



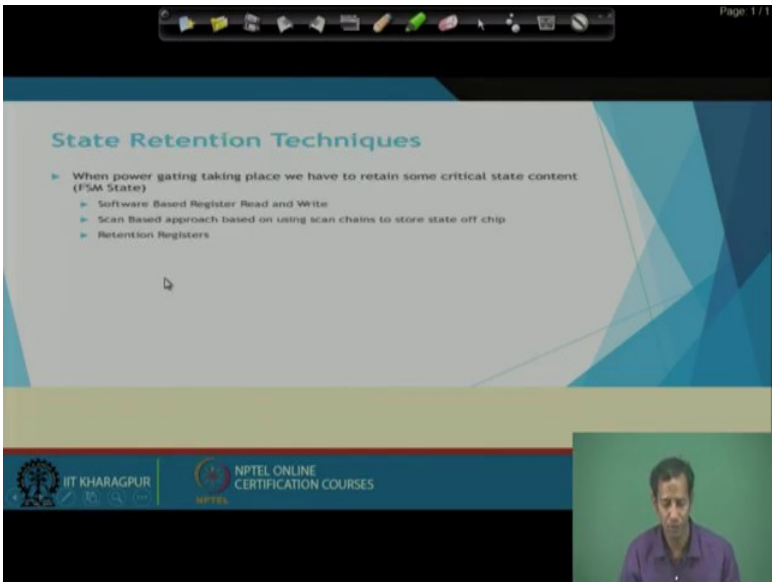
So, the 2 actually techniques you can for a complex circuit you can not apply this fine grain; that means, each of the transistor is power gated.

So, at the time it will create a too much of overhead because, we are putting some of the register and the controller part, we will be much more complicated at that time. So, then the controlling mechanism for this is that non state preserving power gating, the cut off multi threshold then boosted gate then, super cut off. The other one is that state preserving power gating is that variable threshold, zigzag cut off or 0 delay ripple turn on, state preserving use some retention registers to store the corresponding states.

So; that means, these are the controlling what I said is that power gating technique or the power; that means, the transistors or the sleep transistor whatever we put whether, that is head or tail. So, depending on that we have to control them that ok. If this is sleep mode then you please disconnect the ground power line or disconnect the ground line from the main block.

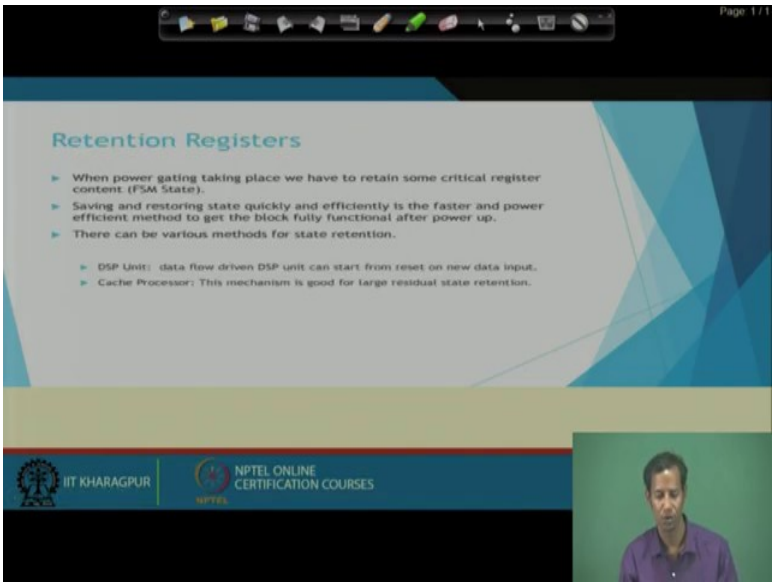
So, something like that we have to actually we to do this power gating control mechanism for this particular cells, which we use depending on different type of which is this cut off, multi threshold, boosted gates, super cut off. So, there are several other ways to control these particular transistors.

(Refer Slide Time: 12:15)



So, then state retention technique is that when power gating taking place, we have to retain some critical state content or FSM. So, software based register read and write, scan based approach based on using scan chain to store state off chip or the retention registers

(Refer Slide Time: 12:39)



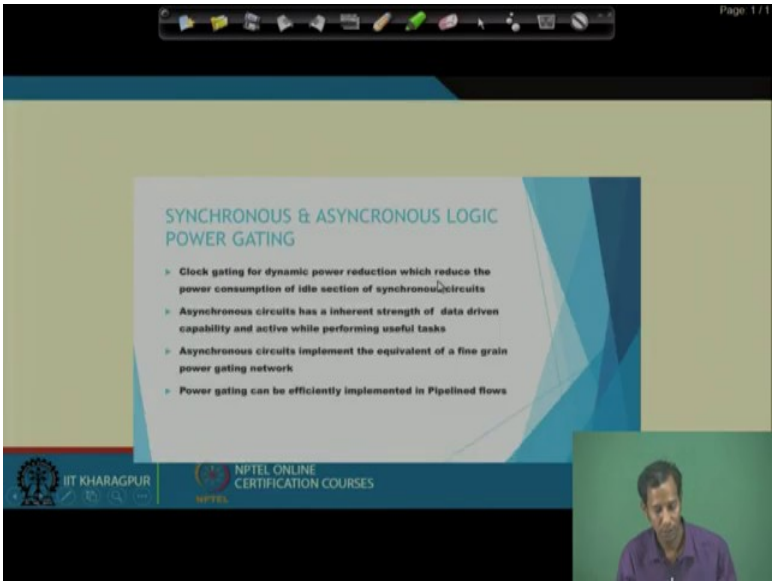
So, these are all actually the power consumption method and then this retention registers. What are these retention register says that? When power gating taking place, we have to retain some critical registers content and saving and restoring state quickly and

efficiently is the faster and power efficient method to get the block fully functional after the power up.

There can be various methods for state retention then, DSP unit, the data flow driven DSP unit can start from reset on new data input and the cache processor. This mechanism is good for large residual state retention means what actually whenever we are basically powering up the system design.

So, at that time in DSP what we can do, we can you can use the reset signals to basically get the new value or to retain the corresponding value in the resisters or in processors, we can use the cache memory to retain the corresponding state of each of this particular registers.

(Refer Slide Time: 13:46)

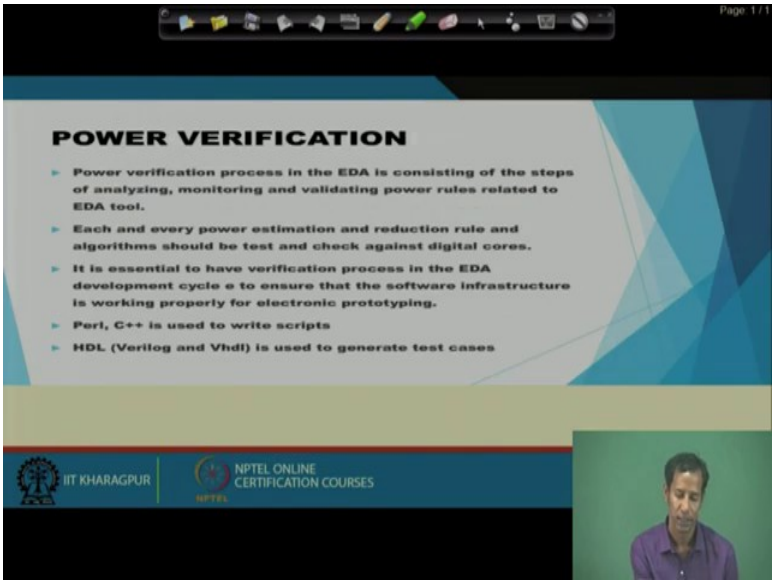


So, now then again another thing is that. So, how you can do this synchronous and asynchronous logic power gating. So, clock gating for dynamic power reduction which reduces the power consumption of idle section of synchronous circuit. Asynchronous circuit has a inherent strength of data driven capability and active while performing useful tasks. Asynchronous circuits implement the equivalent of a fine grain power gating network; power gating can be efficiently implemented in pipelined flows ok.

So; that means, all the synchronous circuit as well as this asynchronous circuit, we can apply this clock gating as well as the power gating. Whereas, this asynchronous circuit,

they can be much more they will be much more useful for actually power gating or their controlling mechanism for this power gating in synchronous circuit that will be much simpler than the asynchronous circuit.

(Refer Slide Time: 14:53)



Then, we need to verify the power like whenever actually we do the this digital circuit design. So, at that time we run some a formal verification or some verification method. To check that ok, if I apply this stimulus. Then, at that time what will be my; that means, expected output. If it is match then we can say that ok, we are getting or we have designed the proper design ok.

So, we do timing analysis, we do everything to get or to know that my design whenever it will comes in the physical form at that time it will work perfectly fine. But, still there is a huge gap between the real time performance and the virtual performance of my chip but, still which creates the yield.

But still actually we the people try to make the gap very much closer. So, that the virtual performance, it really or nearly close to the actual performance of the real time performance of my circuit design.

So, just like this actually this formal verification, which we do in the digital circuit design. So, we have to do some power verification method to. So, in the power verification process in the EDA is consisting of the steps of analyzing, monitoring and

validating power rules related to EDA tools. Means, what so at the time in the EDA tool. So, that is an automated process. So, in the EDA tool need to consider that ok.

So, that in which particular region, I am consuming of my whole chip, which region I am using most of the power. So, if I find that the memory is consuming suppose, inside in processor design the memory is consuming much more power or the video processor is taking much more power.

So, at that time I will try to consider how I can apply different techniques to reduce the power consumption on that particular block. Why because in the complex nowadays, this complex system design. There will be so many sub blocks ok.

So, if I IP based design. So, so many IPs are connected. So, among them which IP contributes to how much power in the overall power budget of my system overall system. So, that why I have to know and identify and then according to that I can take the necessary steps to reduce the power consumption to that particular block.

So, that is why we need one power verification tool. So, that the tool automatically does the power information, it will provide to me and depending on that particular report now, I can take my decision or I can take the steps against the corresponding report.

So, that is why each of this each and every of this power estimation and the reduction rule and the algorithms should be test and check against the digital cores. It is essential to have verification process in the EDA development cycles to ensure that the software infrastructure is working properly for electronic prototyping ok. So, another point is that still now, actually we are basically working or we are taking about hardware.

But, there actually I need one perfectly systems to be work perfectly fine. I need the perfect software's too. So, suppose 1 laptop you are using, if there is no such operating system, at the time you cannot use the laptop. Whenever, you put the operating system then, only your; that means, you can work or you are; that means, a whatever hardware is that. So, that is useful for you at that time only.

So; that means, software is also one of the major part which controls your hardware. So, that is why whenever we are we have done everything like ok, we have done this enable

signals and all these things. But, ultimately there will be the control will be in the hand of the software's.

That means, whenever the device will be in the; that means, ideal mode. How the device will know that I am not using or the any process is not running on the processors. So, that is job of the software's which will say that ok, if this particular process is not running in a laptop or in a mobile phone or in a any electronic system.

So, at the time you put that thing in the sleep mode. So, that activation signals or control signal will come from the software part only. So, that is why we have to verify these verification processes along with the software part and the hardware part. Both are together actually we need a verification to that everything is running fine; that means, whether we will put the hardware under the software.

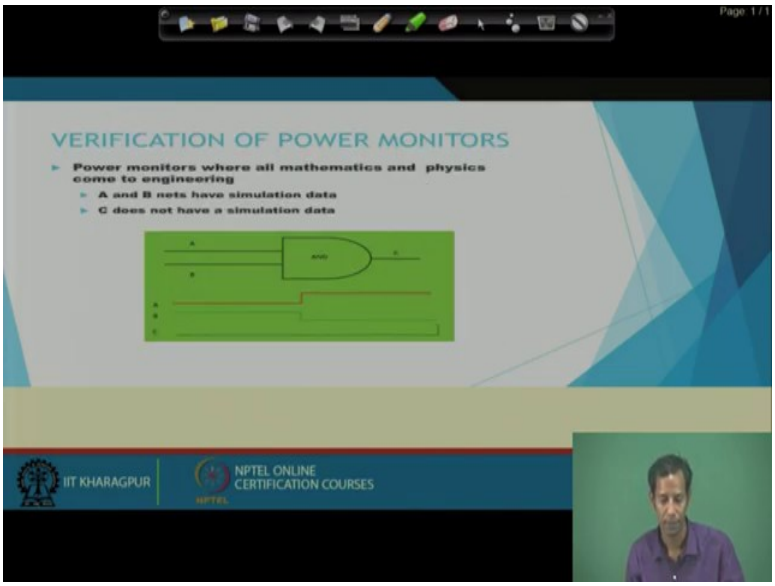
So, at the time it is working or the power consumption whatever we are claiming that it is reduced or it is increased or it is something else. So, at the time it is work perfectly fine. Perl and C plus plus is the language, which we use to write the script and then HDL hardware description language, the Verilog and the VHDL is used to generate that test vectors or the test case.

So, power they actually to verify; that means, what will be the power actually I need the test vectors. Why I need the test vectors? By applying the test vectors, I can get the corresponding actually switching activity of all the signals, all the nets which are present in my system.

So, whenever all this switching activities information I stored somewhere and then if I give that switching activities to the tool. Then, only it can calculate that based on these switching activities or based on these particular simulations; that means, based on this particular test vectors.

This is your; that means, activity and this is your power report of dynamic power consumption or the leakage power consumption or the switching power consumption or the; that means, glitch power consumption, if there is a glitch. So, glitch power consumption every power information at that time, it will be provided to you. Once you run the simulation and provide that particular; that means, the all these switching activity file to the power simulator.

(Refer Slide Time: 21:41)

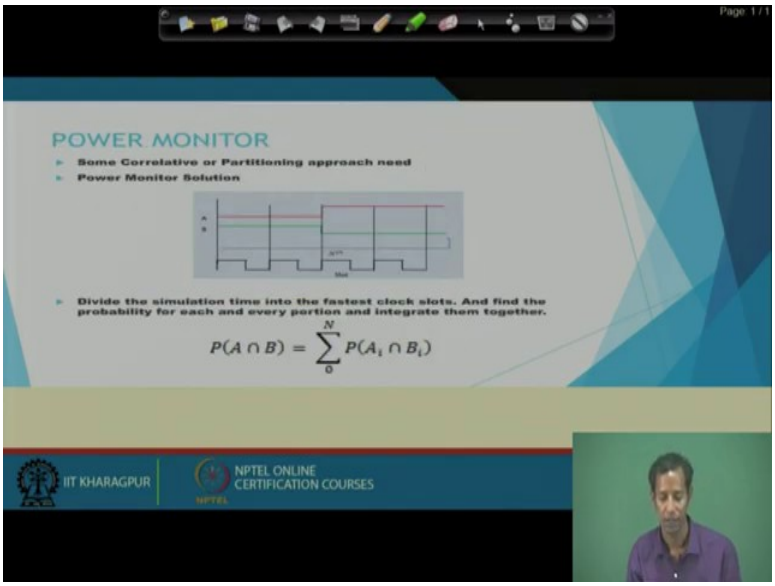


So, now how actually you can do verification of power monitors. So, this power monitors where all mathematics and physics comes to engineering. So, suppose consider that A and B nets have simulation data.

So, C does not have a simulation data. So, at that time this depending on this. Now, this verification how we can do just like in simulation what we can see that ok, we are having some applied some of the inputs, which will come as the; that means, the waveform.

So, here also if we can see that how much power I consumes in terms of actually this waveform that will be very much easy to interpret the meaning of the corresponding power signals or the power consumption ok.

(Refer Slide Time: 22:37)



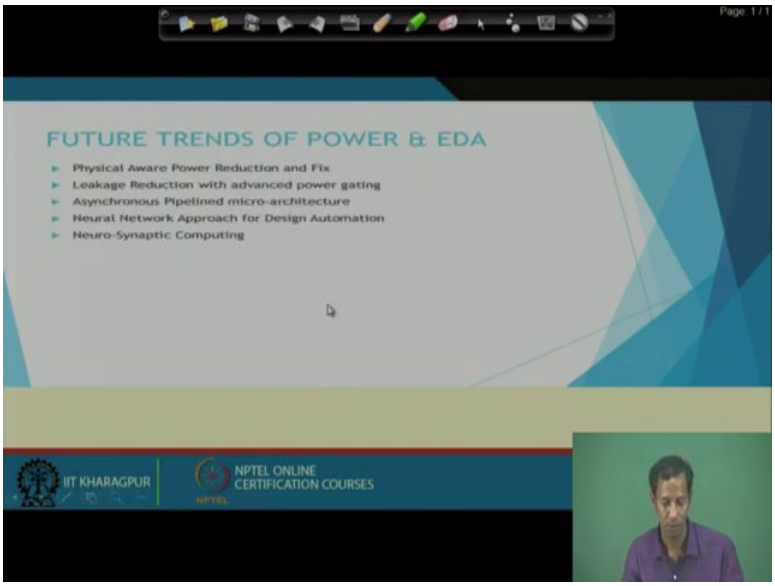
So, the power monitors is that. So, depending on this A and B signals. For this particular case, depending A and B are the 2 inputs, how they are changing. And, depending this is the switching activity of A and B. So, depending on this A and B signals. So, how this C is changing and how this C is contributing to the major power source that we will see through the power monitor.

So, here and power monitors some correlative or partitioning approach is needed and power monitor is the solution for checking or for interpreting the power consumption in a digital circuit in a very simplified way. And, divide the simulation time into fastest clocks slots and find the probability for each and every portion and integrate them together. So; that means, how we calculate the corresponding power is that, we find out the activity rate as well as the probability of that means, how much time the signals will be high.

So, depending on the activity and the probability both together, we can roughly estimate the power of the overall block. And, why actually here why is it is the integrating of the integration of each of these block means what? For each of these signals, what will be their probability and their what will be their activity rate, based on that based on this particular equation.

Now, they are trying to find out the power consumption report.

(Refer Slide Time: 24:15)



So, the future trends of this power consumption this methodology and the EDA is that. There will be 1 physical aware power reduction and then there will be some way to fix it, leakage reduction with advanced power gating techniques, asynchronous pipeline micro architecture then, neural network approach for design automation and neuro synaptic computing.

So, these are the future trends of power and actually these power reduction techniques in VLSI design. So, the first thing is that in every steps of VLSI, we need the power should be reduced. Whether that is we are in actually device level or whether we are in the; that means, the logic level or whether in the system level. So, every level we will try to minimize the power consumption by applying different techniques.

So, it is not that in EDA actually for designing the complicated circuit nowadays. We need the help of EDA; that means, a process will be automated. So, at the time, if we can develop some of the physical aware power reduction and then the fixing methodology inside of the EDA tool itself.

Then, the leakage reduction with advanced power gating option like this strong ODC or strong SDC options embedded with the EDA option EDA tool. Along with the asynchronous pipeline architecture as we said the instead of synchronous asynchronous circuit are a like they are more low power application. They will be applicable for more low power application or they can achieve more low power.

In and then the recent trend is that neural network or the artificial intelligence applied on the design electronic system design automations. That means, if I find that this is the artificial intelligence means what actually, if I can experience that ok, this is the previous situation I get ok.

At that time I have used this power gating of up to let us say 60 percent to the overall circuit. So, at that time if I find the same situation so, at that time without considering anything again, I will apply 60 percent power gating at that time to the overall circuit.

And, then we are having this neuro synaptic computing, which is again the emerging this artificial intelligence or the neural network approach. And, the neuro synaptic computing in the EDA tool for this power reduction or this to area optimization or to this speed in enhancement, all this to make a 1 efficient circuit design. All are the recent trends in the this VLSI design tool in the electronic design automation aspects ok.

So, with that this is the end of this power, this is the power reduction techniques. There are many and still people are trying to as this is a future trend. So, still people are trying to improve the techniques to which will be applied for reducing the power to a great extent. So, with that this is it for today again, we will see some other topic in the class.