Power System Protection
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Lecture 24
Protection of series compensated lines-part-I

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Welcome to power system protection course module on distance relaying. In this lecture we will address protection of series compensated lines, this is part 1.

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So, the coverage in this 1 will be concepts on the issues with series compensated line, protection perspective, current and voltage inversions and how these issues create problem in directional relaying and what is the solution approach that we will see.

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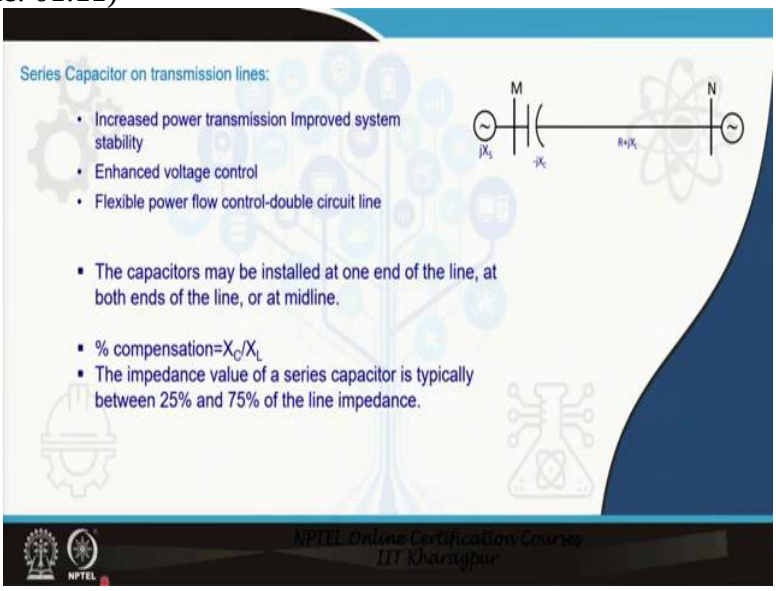

So, see this system, simple system, 2-bus system, we have now series capacitor in the system, series capacitors being $-jX_c$, the corresponding reactance as compared to the jX_l of the line or jX_s for the source, so this reduces the reactance of the network including the fault loop. This is being widely used for numerous reasons; number 1, it increases the power transfer capability because equivalent X of the transmission system reduces, enhanced voltage control as drop in the system, network system will be reduced, X equivalent (X_{eq}) decreases and $(I)_{Xeq}$ will be small so drop will also be small. Flexible power flow control, if you have a double circuit line and if we have a series compensation in 1 of the line, then if we switch on the series compensation in the circuit, then one of the line will be having more power than the other one.

Or if we have a controllable capacitor we can control as per the requirement. So, these capacitors can be installed at the line ends here at this end also or at both ends or can be installed at any intermediate point in the line. But generally, line ends are preferred because we do not need further more substation and so. Percentage of compensation is defined in terms of the value of X_C/X_L, the corresponding line to which it is connected, typical compensation level varies from 25 % to 75%, in special cases it may be more also.

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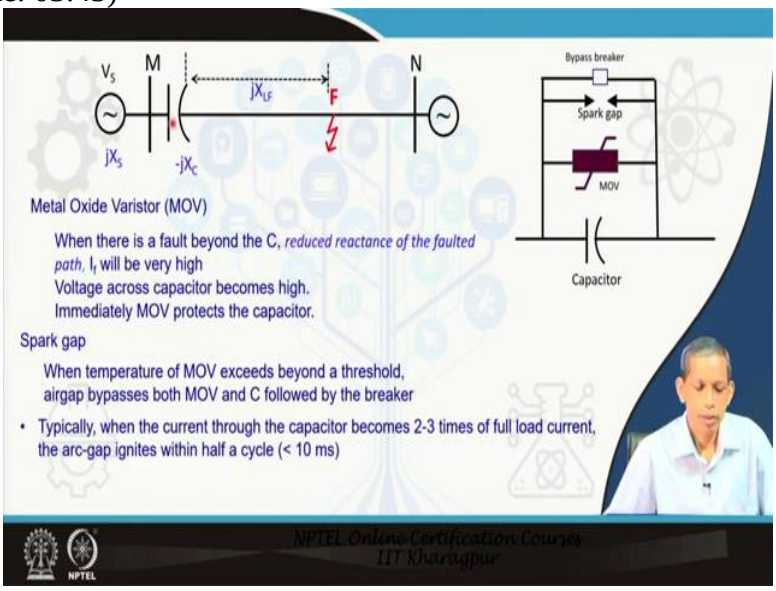

Now, for this capacitor, it has its own protection arrangement like each capacitor in each phase maybe a bank of capacitors connected in series and parallel to have the required capacitance for the particular compensation. These Bank of capacitances they are being protected by an arrangement as in the diagram. Metal Oxide Varistor (MOV), which happens to be a nonlinear resistor which functions whenever a voltage across the MOV increases, the resistance becomes significantly low and therefore, the current through the MOV becomes high. And this gives you a scope to consider to bypass the circuit to which it is connected. We have a spark gap, controllable spark gap and then we have a bypass breaker.

Now, what happens in this case, this is the line to which the capacitor is connected. So, if this side is source and this side is having a fault here in the network then the current path in the fault loop, the fault loop reactance becomes significantly low because of this $-jX_C$ and that is why the current becomes very high.

So, when the current becomes high through this capacitor, the I.X drop across the capacitor becomes very large during the fault and thereby the voltage across the MOV becomes high, so the MOV triggers immediately and the corresponding current, significant current passes through this and thereby the corresponding current through this capacitor decreases and the voltage is being clamped, this saves the capacitor from possible damage.

Now following this, the spark gap now functions, the temperature of the MOV increases, the energy content in the MOV increases and following a threshold on the energy associated, this spark gap is being ignited and this spark gap leads to a bypass of this MOV also. So, this spark

gap bypasses the MOV and the capacitor and thereby the corresponding voltage across becomes very negligible.

Following that the bypass breaker operates and this saves the corresponding capacitor from high voltage issue, and note that the corresponding capacitor, is in the circuit normal time, if a fault happens to be there and the corresponding current becomes significantly large, the corresponding capacitor is being bypassed by this protection arrangement.

So, the corresponding currents of the capacitor becomes when it becomes more than 2-3 times the full load current, the arc gap ignites and within less than 10 milliseconds, but before that the MOV also operates immediately. So, with this functionality of the protection arrangement of the capacitor, the corresponding relay at this bus will see the corresponding current and voltage pattern because the corresponding X of this capacitor will be modulated by this functionality of this MOV spark gap or the bypass breaker.

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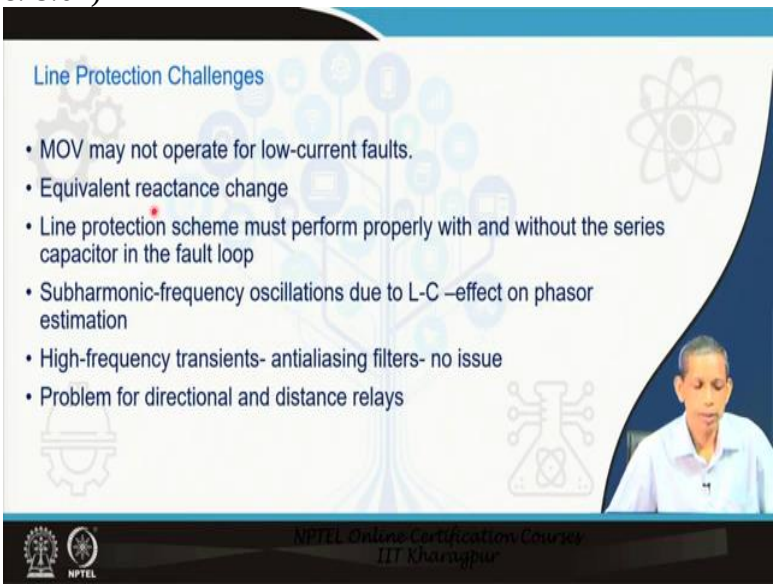

Now, this arrangement leads to transmission and protection, MOV may operate or may not operate, MOV will operate when the current become more than 2-3 times rated value in the fault path. But for lower current due to very remote fault or fault associated with any arc or higher resistance fault, the current may be low and then the corresponding capacitor may not be bypassed. MOV operates, following that the corresponding air gap ignites, this phenomenon leads to change in equivalent reactance and therefore, the corresponding current and voltage across the capacitor and so also at the relay point.

Line protection scheme must take care of these operations, so where capacitor maybe there in the circuit and capacitor may not be there because of the bypassing by this arrangement.

Furthermore, the introduction of C in the line which has the line has series inductance, so this LC combination gives us sub-harmonic frequency component oscillations therefore, in this signal as seen by the relay will be having these components and which will affect the phasor estimation process as we have studied in the phasor estimation by 1cycle DFT or so. So, the frequency response of that we have seen that sub-harmonic component affects the performance of the phasor estimation technique.

Furthermore, because of this air gap and the MOV operations, the transients will be introduced, higher frequency transient will be introduced in the signal, but we have an anti-aliasing filter and `before the processing by the digital components. Therefore, they do not have any issue to the numerical relay performance.

The challenges which we will see in the directional relaying or in the line protection perspective, 2 aspects; 1 in the distance relay itself, and we know distance relay also requires directional features, may be a separate directional logarithm also. So that we consider that component is also affected by this presence of this series capacitor in the circuit, we would like to analyse in this lecture, we will address only the directional relaying part, in the next 1 we will talk about distance relay.

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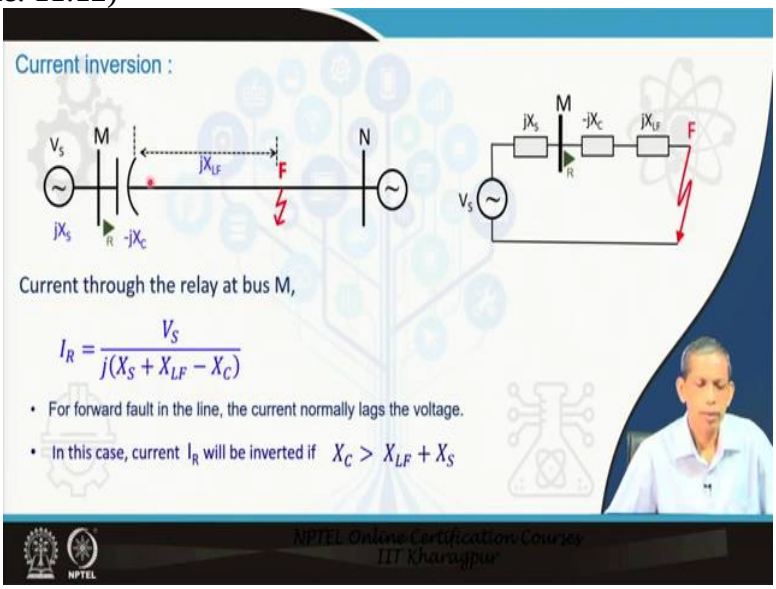

First phenomena which is being there which will be there in this series capacitor, presence of series capacitor we will try to analyse that, this phenomenon called current inversion phenomenon. Now, let us consider a system like this where we have a series capacitor at the M bus end, where we have the relay, already pointed out the capacitor can be at this bus also or both also or in the middle also, but this analysis also can be extended to any other position

of the capacitor. Now, a fault happens to be there at F point in the line which has a reactance up to from the relay bus to this fault point jX_{LF} and the corresponding capacitor having a reactance of $-jX_C$.

The equivalent circuit diagram for this system and becomes this up to the fault point, let's say 3 phase fault. So, we have V_s and the corresponding jX_S of the source and the bus and $-jX_C$, and jX_{LF}. So, this path now having an equivalent reactance of $jX_S - jX_C + jX_{LF}$, we have neglected resistance for simplicity.

Current to the relay bus at M for this situation will be $I_R = \frac{V_s}{j(X_s + X_{LF} - X_c)}$. Now normally this X_c is not present so we have $I_R = \frac{V_s}{j(X_s + X_{LF})}$. So, this part becomes a positive part and we say that the corresponding relay current lags the voltage by close to 90^0, ideally it should be 90^0.

Now, what happens in this presence of this X_C, this part there is a chance of this part can be negative. So, when this $X_C > (X_{LF} + X_S)$, this combination $(X_S + X_{LF} - X_C)$ becomes negative, so it means that as compared to the normal case, the corresponding current will be in anti-phase so that is what the issue.

So, normally we say that the current lags the voltage during a fault like this, but with the presence of X_C and if this condition is being satisfied, the current will lead and it will be around 180^0 out of phase to the normal current which we have seen in our earlier analysis because the corresponding current is being inverted, we call the phenomena as current inversion phenomena in a series compensated line.

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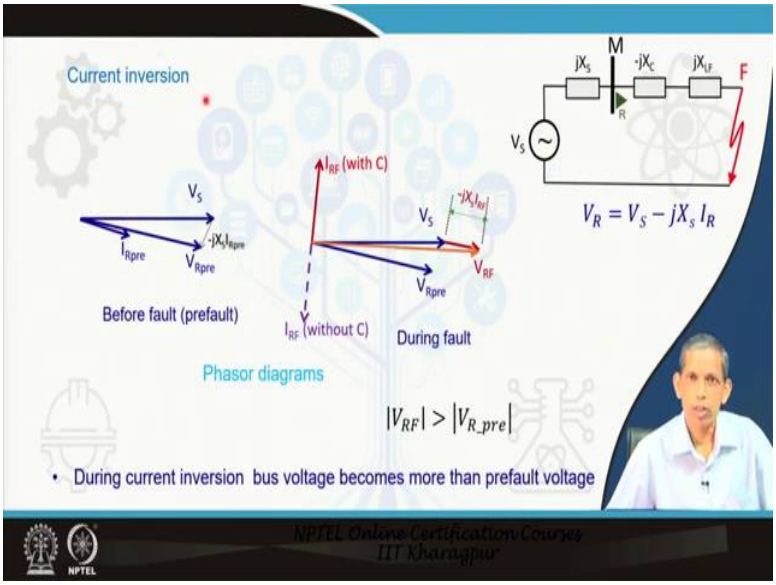

Now, for this 1 we like to consider this phasor diagram to have our clarity and to have our further analysis on different relay applications. So same circuit, suppose Vs this is Vs. So, we know $V_R = V_s - jX_s I_R$, so this relation, so Vs before the fault, the line was leading to certain inductive load or slightly inductive load or so, it is connected with the further line and so circuit will be like inductive circuit. So, therefore we can say that I_R ,Vs - $jI_R X_s$.

So, this I_R is considered as let us say I_{pre} is very close to this V_{Rpre}, with drop in this part will be leading to this I_{pre} , $jX_S .I_{pre}$. So therefore, if we subtract the drop then this will be $-jX_S .I_{pre}$ like this here and then this becomes equals to V_{pre}. So, before the fault the poison of V_{pre} lags the V_s by a small angle as you know, that is a pre-fault issue.

So, now come to the fault issue, so in the same V_s , now from the earlier analysis, we say that the current will be inverted so the capacitor would not be there, the corresponding current in the fault path will be lagging current almost 90^0 ideally, and then it will inverted because of that $X_C > (X_{LF} + X_S)$ and that leads to we can say the corresponding inversions to be the current directions will be like this with the presence of the capacitor if that condition is being satisfied, $X_L > X_{LF} + X_S$.

So, in that case, because you are talking about current inversion case, so in that case the corresponding current direction and fault current direction will be upward in this phasor position, and then you can say that the drop here you can say that will be as usual - $jX_S .I_R$ again.

So therefore, $-jX_S .I_R$. So, this part will be to the right hand side anti-clockwise, so this is minus $-jX_S .I_{RF}$ in this side. So, if we add these, Vs and $-jX_S .I_{RF}$, then the corresponding V_{RF} becomes

this. So, this is the position of V_{RF} what we see. The immediate conclusion we see here, because of this phasor position is in the upward direction the corresponding V_{RF} relay voltage during fault during current inversion situation becomes a larger value as compared to the pre fault voltage as compared to the pre fault voltage at the relay position so, this is the peculiarity we observed.

Normally, during fault time there will be a drop in the system, this part in the source side and therefore you can say that the corresponding voltage of the relay bus will be smaller than the pre-fault voltage, but now we see that a larger voltage due reason is the current inversion. So, during current inversion the voltage becomes more than the pre-fault voltage, but the current is now leading even though the corresponding fault is forward, (())(18:01) which is a difference. Earlier, without the capacitor we were considering that the corresponding current will be lagging to this voltage almost 90^0 or so.

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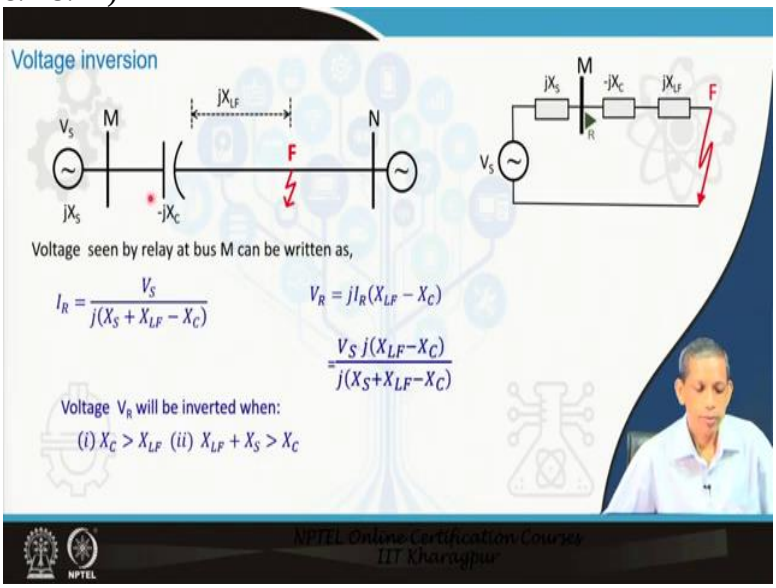

Now, we will go to another phenomenon called voltage inversion like we discussed on current inversion. Same system so you have relay here as we see here and then the equivalent circuit diagram becomes this. Now, what circuit condition leads to a different situation we would like to figure out that. So, voltage seen by the relay at bus M. Now, we will calculate the voltage seen.

So, already we have mentioned the IR through this is $I_R = \frac{V_s}{j(X_s + X_{LF} - X_c)}$, the V_R this voltage for the 3-phase fault case consider that this point voltage is 0 so therefore, the corresponding voltage of bus M will be $V_R = I_R \times j(X_{LF} - X_c)$, So this is the relation, so the

voltage at relay bus is V_R becomes this. If you substitute this I_R here, then in terms of Vs, the V_R becomes $V_R = \frac{V_s \times j(X_{LF} - X_c)}{j(X_s + X_{LF} - X_c)}$.

Now, what we see here that we will have a voltage inversion like the current inversion condition that $(X_s + X_{LF} - X_c)$ becomes positive but $(X_{LF} - X_c)$ become negative. Now how? If $X_C > X_{LF}$ so $(X_{LF} - X_c)$ becomes negative and this $X_C < (X_S + X_{LF})$. Once again that up to the fault point the corresponding impedance should be smaller than X_C first condition, second condition the denominator $(X_s + X_{LF} - X_c)$ becomes positive how, when the $X_C < (X_S + X_{LF})$.

So, this is a combination of the source side impedance plus the impedance of the fault point. If these 2 conditions are being satisfied, then what depends we see here. This part becomes positive, but this part becomes negative, J, J cancels out. So, finally, this becomes equals 2 with a negative sign V_s with certain value, whereas in normal condition, if this X_C is not there, then j, j cancels out and $(X_{LF} - X_c)$ becomes positive value, $(X_s + X_{LF} - X_c)$ becomes a positive value so V_R and V_s are very close to each other that we have learned.

But now, with that these 2 conditions we see here, $(X_{LF} - X_c)$ becomes negative, $(X_s + X_{LF} - X_c)$ becomes positive. So, there we consider a negative sign will come here, which is nothing but the anti-phase or the corresponding inverted voltage and that is the situation so that is the name voltage inversion. So, we see that current inversion for a particular condition of the circuit and we have voltage inversion for a particular situation of the circuit.

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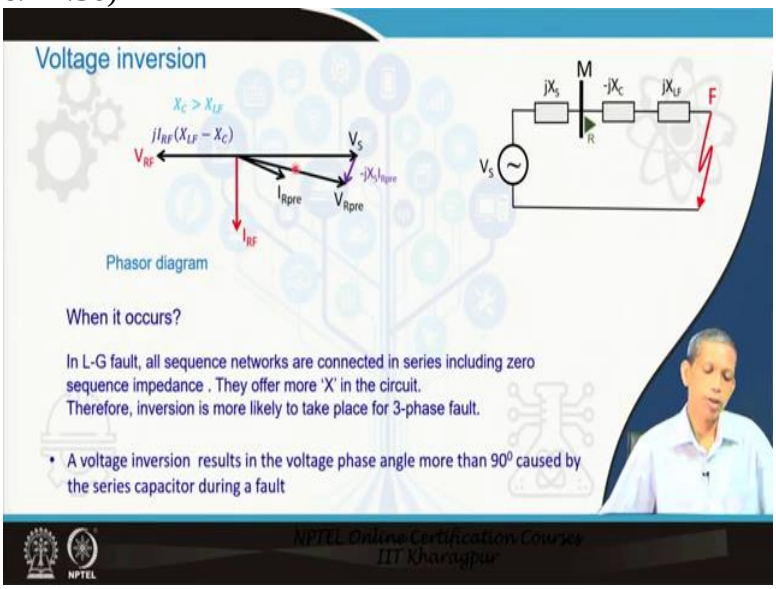

Now, similar to the current inversion for the corresponding phasor diagram for the voltage inversion, same network, so we have ($V_S - jX_s.I_{pre}$) so this becomes V_{pre} as observed by the relay bus by the relay. Now, the corresponding current through this path is lagging here, because of the denominator being positive, $(X_s - X_c + X_{LF})$ becomes positive so current will be lagging so this is a lagging current in this case, to this lagging current, if this I_R considered is this like current.

Now, our point is that the voltage here is { I_R . $j(X_{LF} - X_c)$ }, which happens to be a negative So, { I_R . $j(X_{LF} - X_c)$ }, so that gives us this part, so J of this, so this become this, but this $X_c > X_{LF}$ so, therefore we can say that this becomes takes a position like that as compared to this.

So, that leads to the corresponding this, now if we suppose you can see that the corresponding X_{LF} , X_C is not there, so (j I_{RF} . X_{LF}), that is +j so 90^0 anti-clockwise to take a (())(22:57) position like around V_s, but now because this $X_c > X_{LF}$. So this will be anti-phase to that Vs close to that and thereby it takes the V_{RF}, the voltage at the relay takes a poison like this and that is the name we call voltage inversion usually, the corresponding fault voltage remains like in this close to this V_s V_{pre}, but now consider that it will remain not Vs the V_{Pre} but now you can say is almost 180^0 out of that.

Generally, we can say that this voltage inversion results in the voltage phase angle more than 90^0 , 90^0 to 180^0 kind of thing during fault for the voltage inversion situation. But note that this circuit diagram we discussed for the 3-phase fault but faults can be phase- to-ground, double phase-to-ground or double-phase fault.

But in other networks, other faults the positive, negative, zero sequence components they add up depending upon the types and thereby they offer larger value of x for the rest of the system and therefore, consider the voltage inversion is not that common in other types of faults as compared to the 3 phase fault perspective and so on. However, whatsoever, the protection schemes cannot ignore such situations.

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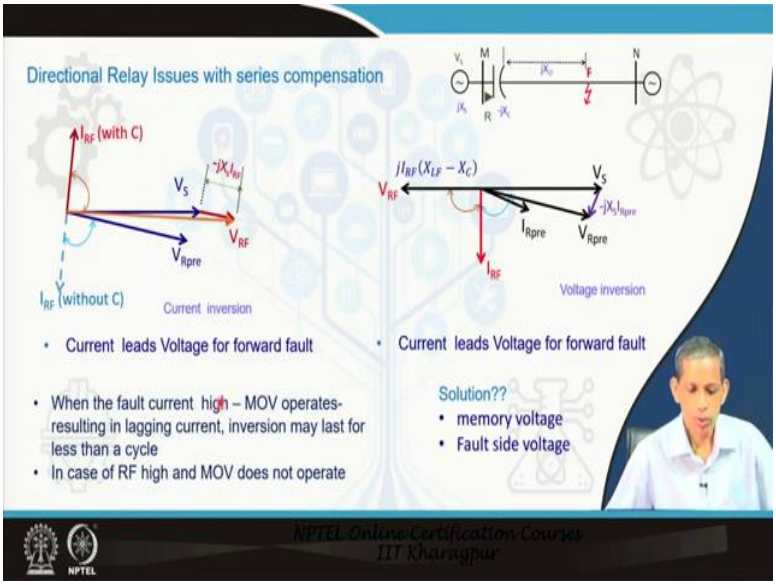

So, we see here, what are the current inversion and the corresponding voltage inversion. These has direct implications to directional relay. So, we will see first what are the issues with directional relay. So, the phasor diagram we have already seen for the current inversion, in case of current inversion the corresponding current becomes upward with respect to this V_{RF}, V_s or the V_{Rpre}, leading current whereas usually it should be lagging current. Now, the corresponding things, as compared to that in case of with capacitor with respect to this relay voltage, the corresponding current becomes leading, but the fault is forward fault.

So, therefore, we say here you can say that this will create problem to the directional relaying based on phase components, based on positive sequence component approach and so. Whereas, normally it should be lagging and because the directional relaying (())(25:37) approach we have discussed is based on the sequence component of current, based on the sequence component or phase approach and so, that is why you see here, we expect this angle up angle based directional relaying is expected to be affected by this issue.

Now, in the voltage inversion case, if you see here the corresponding voltage becomes anti phase to the normal voltage phase position, like that, we see that the corresponding current now leads the corresponding voltage even though the fault is forward this will also create problem in this perspective also.

So, in both cases we see that current leads the voltage and that is the issue, whereas it should lag in normal as in the normal system. There are other points to be noted when the fault current is high MOV operates resulting in lagging current means the capacitor is bypassed resulting in lagging current.

So, this inversion process may last for a few milliseconds to within a cycle in this system, in case the fault resistance is high, the MOV may not operate, in that case the capacitor will be in the circuit and the system may observe the corresponding current inversion and voltage inversion so therefore, the relay algorithm, the protection scheme should be equipped with both the possibilities.

Some of the solutions strategy if we can see the corresponding voltage inversion issue, then instead of taking the voltage at this point, if you measure the voltage at the line side at this point, so fault from this side the corresponding voltage calculation will not be considered inclusive of the capacitor and thereby the system will be behaving like as usual what we have seen earlier.

So, if you can avail the corresponding line side voltage, then the voltage inversion phenomena for this case will not create any problem to the directional line approach. The other you can say that solution is memory voltage, if we see in this case, if we use the corresponding pre-fault voltage not the fault voltage, then our problem is solved.

If we use the pre fault voltage, not the fault voltage then is solved however, pre-fault voltage can be used to a certain period of time because of the issue of frequency drifting with time during the fault and so, therefore you can say that you cannot compare the phasors during fault to the pre-fault value and other issues are also there.

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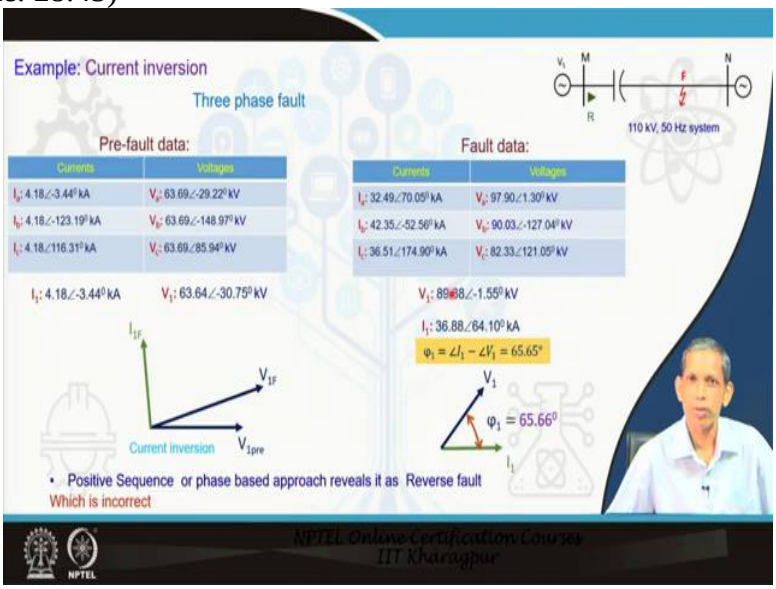

Now, we will see through examples, the corresponding issues and how they affect the directional relaying and then we will see what is the solution strategy also called the directional relaying perspective in the presence of current and voltage inversion issues. 3 phase fault in a

2 bus system 110 kV, 50 Hz system 3-phase fault to create current and voltage inversion issue. We have pre-fault data; we have fault data balanced system.

Now, fault data 3 phase fault current rises significantly, but you see voltage also rises in each phase. So, voltage rise from the pre-fault clearly indicates this is a current inversion phenomenon that we have already analysed. We computed these corresponding I_1 and V_1 for the pre fault and fault. I_1 and V_1 for the fault case also.

In the phase based approach consider in the positive sequence based approach if you see this positive sequence perspective, so positive sequence voltage having -1.55^0 and the corresponding current is 64.10^0. So, $\phi_1 = \angle I_1 - \angle V_1$, which we have already used in the directional relaying principle that becomes 65.65^0. Note that, this positive angle implies reverse fault whereas this is a forward fault. So, that means that the positive sequence based approach fails in the case of we can say that current inversion situation in the circuit.

Note that this is current inversion and if see the corresponding case so, the V_{1F} and this I_1, the I_1 is leading that clearly shows that this is a situation of the current inversion, in the phasor diagram we saw that current inversion has 2 issues, one is at the voltage rises and the other is you can say the current also leads the voltage. So, the current inversion what you mean that, if it had been a normal line then the current should lag the voltage, but now the current may lead a significant amount to the voltage.

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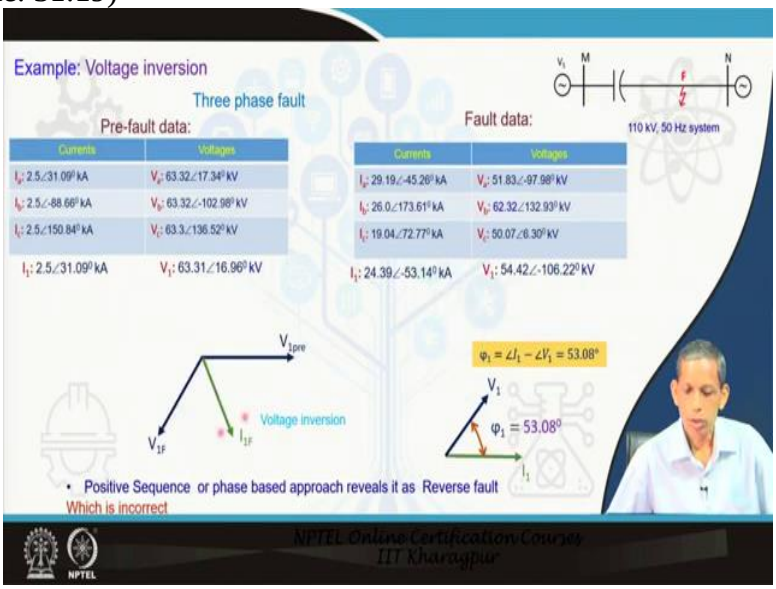

Now, I will go to another example on voltage inversion, same system, 3 phase fault again and we have 3 fault data set of measurements for a voltage and current, the corresponding positive

sequence current and positive sequence voltage calculated and the corresponding fault data Ia, Ib, Ic, significant amount of current Va ,Vb ,Vc and the corresponding positive sequence.

Note here the voltage is smaller than the pre-fault voltage so, this is not the current inversion phenomena. Now see this phasor positions so this you can say that V_{1pre}, I_{1F}, so with respect to V_{1pre} the current is lagging but in case of V_{1F} the corresponding current is again leading. So, this means that this is a voltage inversion situation, voltage is smaller than the pre-fault voltage.

Now, if we compute this $\phi_1 = \angle I_1 - \angle V_1$, that we do call the directional relaying that this clearly shows that this angle is again positive. So, this positive angle means it should be a reverse fault, but this is a forward fault for this relay at this position. Therefore, we can say that this method of positive sequence approach fails.

Note, in case of current and voltage inversion phenomena also if you see the phase based approach also, because the current is leading you see or you can say that this is -97 and -45 with the current leading, so this phase-based approach will also fail in the voltage inversion and so also in the current inversion.

So, the conclusion from these 2 examples is that phase-based approach or positive sequence approach will fail in case of voltage and current inversion situation. So therefore, if a series compensated line is there and this series compensated line has issues of current and voltage inversions, then phase based or the positive sequence-based approach of directional relaying principle cannot be used.

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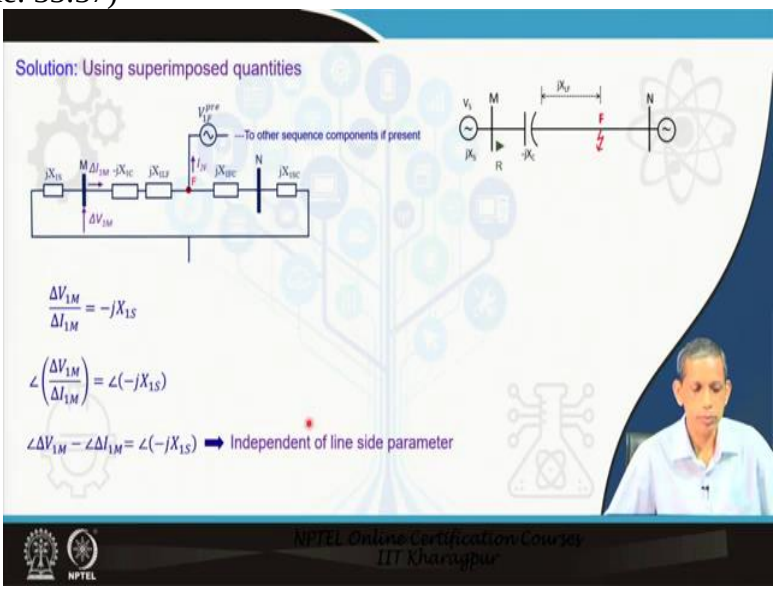

Now come to super-imposed based approach. So, super-imposed based approach, we have considered positive-sequence super-imposed approach, the equivalent circuit diagram, common circuit diagram for other faults and all these things you can add to the other sequence components also depending upon the types of faults, 3 phase fault means you can say it will be having only these positive-sequence component. So, we have already learned that the corresponding relation $\frac{\Delta V_{1M}}{\Delta I_{1M}} = -jX_{1s}$. The current is like this so $-\Delta I_{1M} \cdot jX_{1s} = \Delta V_{1M}$. So, with this we see that the corresponding $\angle \Delta V_{1M} - \angle \Delta I_{1M} = \angle(-jX_{1s})$.

So therefore, this we have already seen in our derivations and analysis for the directional relay part. What you see here, the capacitor part is to the right hand side of the bus relay position whereas this jX_{1s} is to the left hand side. So, the superimposed component as you have already seen earlier also that superimposed components sees the (())(35:01) source side. So therefore, there is no modulation in the source side reactance. So, the super-imposed component we will see the corresponding direction properly unlike that of the positive sequence based approach.

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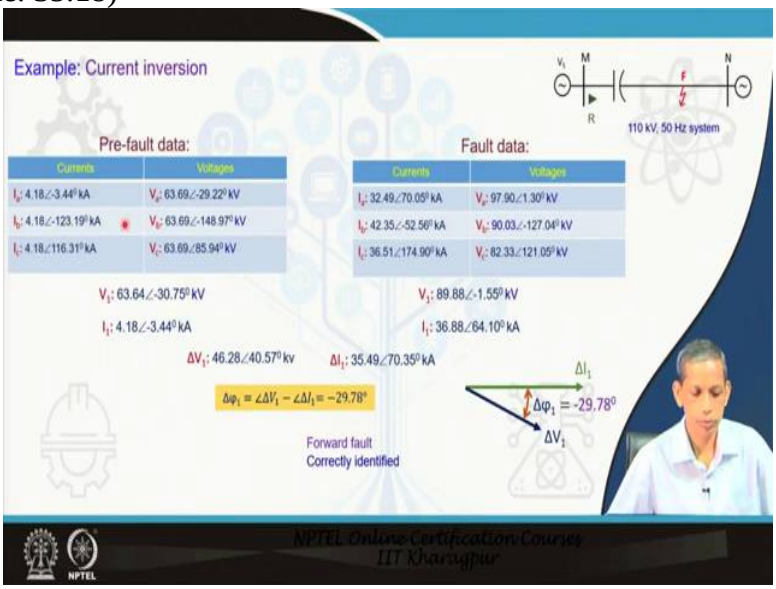

For the current inversion case what you have discussed earlier, we have already computed V_1 , I_1 , and V_1 , I_1 for the same example, so compute the Δv_1 from $\Delta v_1 = v_{1F} - v_{1pre}$ and $\Delta I_1 = I_{1F} - I_{1pre}$. And then $\Delta \varphi_1 = \angle \Delta V_1 - \angle \Delta I_1 = -29.78^\circ$. So, $40.57^\circ - 70.35^\circ = -29.78^\circ$. So this angle is now negative, we say that this is a forward fault. So this what we talk about.

It means that the fault is a forward fault and the approach of positive sequence superimposed component correctly identified the fault and we justified that in earlier slide that because the

corresponding approach sees the source side impedance angle and therefore, it does not have a problem if the corresponding capacitor even in the presence of the capacitor also.

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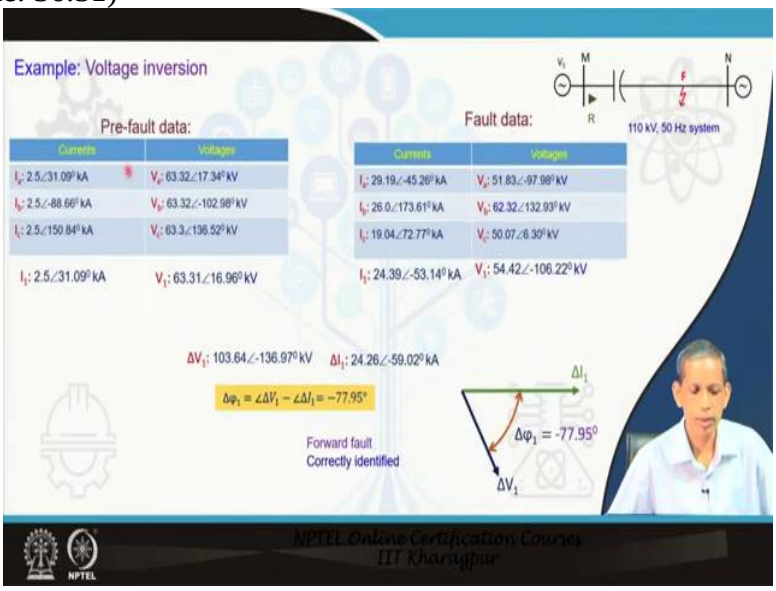

For the voltage inversion case similarly, for the same sets what we have seen earlier the ΔV_1 and ΔI_1 are calculated and when you found that this corresponding ΔV_1 and ΔI_1 are this and we found we can say that these corresponding phasor positions is lagging. So, we can say that because the angle is negative the fault is in forward fault and then the relay algorithm based on the positive sequence superimposed component finds the fault properly.

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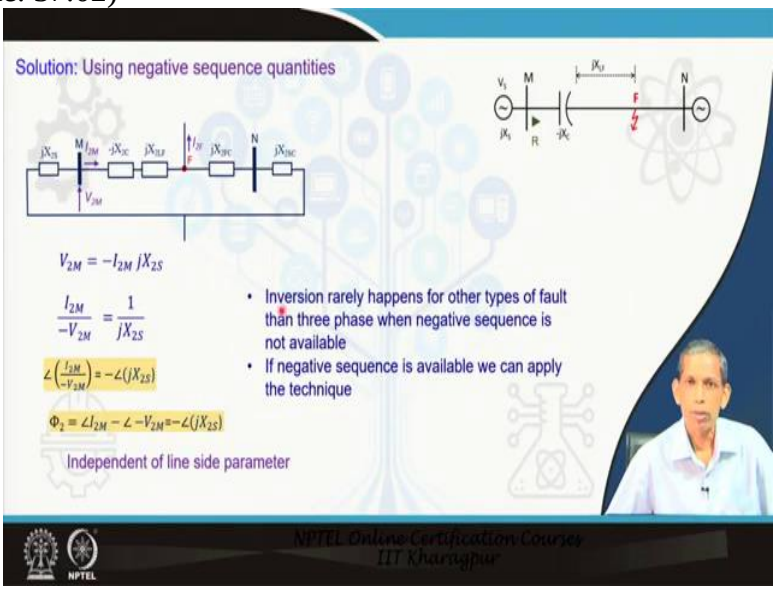

Now, think of now the negative sequence approach which we talked in more details in the directional relaying also. So, this is the negative sequence diagram and we use consider V_{2M} equals to similar to the super-imposed components $V_{2M} = -I_{2M} \cdot jX_{2S}$ and here also the $\Phi_2 = \angle I_{2M} - \angle -V_{2M} = -\angle(jX_{2S})$.

And this is also nothing but depends upon the source side impedance angle only so, therefore this method is also not affected by the presence of the capacitor, which happens to be at the right side of the relay bus in this situation. But, inversion rarely happens, you can say that for other types of faults besides 3 phase as we have already talked about. And however, if the negative sequences is available during certain situations and the inversions are there then the negative sequence can find the direction of fault correctly.

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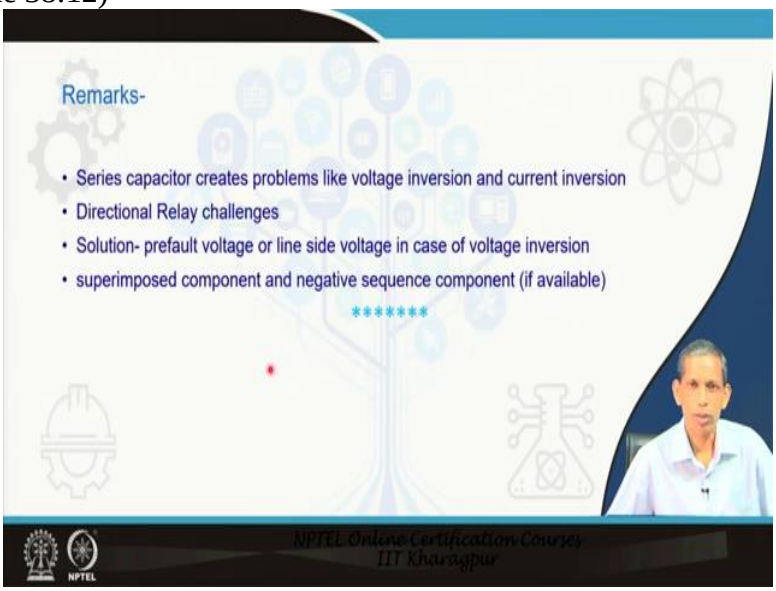

So, in overall, we say that series capacitors create problems to protection issues as it modulates the reactance significantly. Furthermore, the transient associated and the sub-harmonic components may also interfere to the phasor estimation process. We see that directional relays have issues because of the current leading as compared to the current lagging for the forward fault case.

Solutions, a simple solution, use line side voltage or pre-fault voltage for voltage inversion issues or use the super-imposed component or the negative sequence component if available, for any inversion issues. Next lecture we will see how series capacitor affects the distance relay apparent impedance calculation perspective. Thank you.