Power System Protection
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Lecture 05
Numerical Relaying Concept

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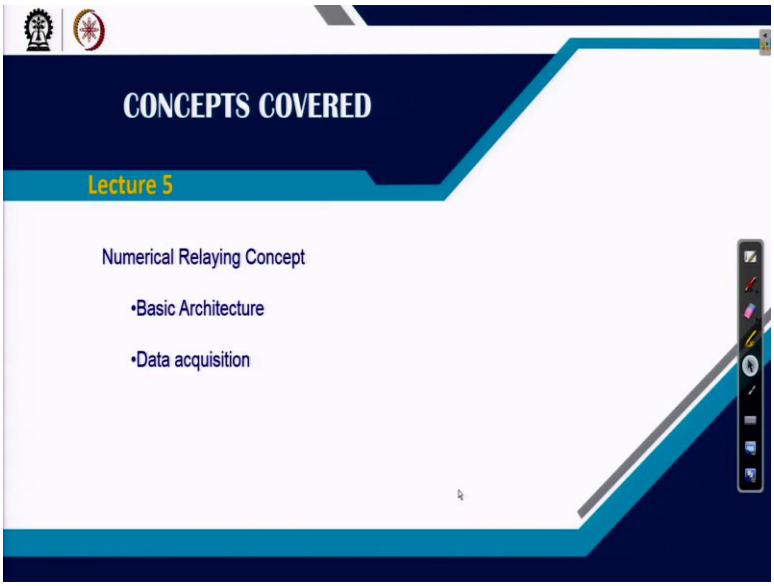

Welcome to the lesson 5 on Module 1; Numerical Relaying Concept. In this lesson, we will discuss on the basic architecture of Numerical Relaying, corresponding data acquisition system, sampling and how the numerical relay is a combination of hardware and software.

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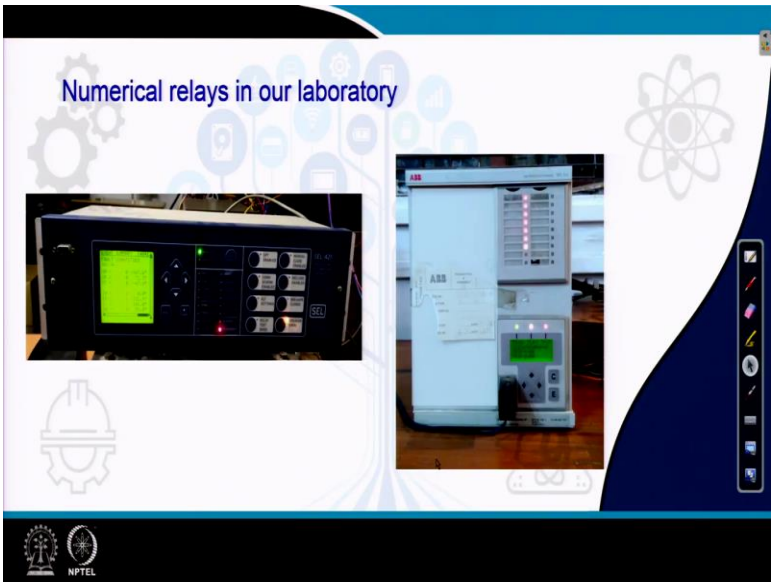

This is a picture of numerical relay available in our laboratory. If we see this picture, then this is the front panel, and where we have LED lights, those are indicators, in case of trip, in case of alarm and so. Here, in this portion you can see the different values of voltage, currents available and the relay provides continuous monitoring of the currents, voltages and the different parameters of the system also. In addition during the fault process.

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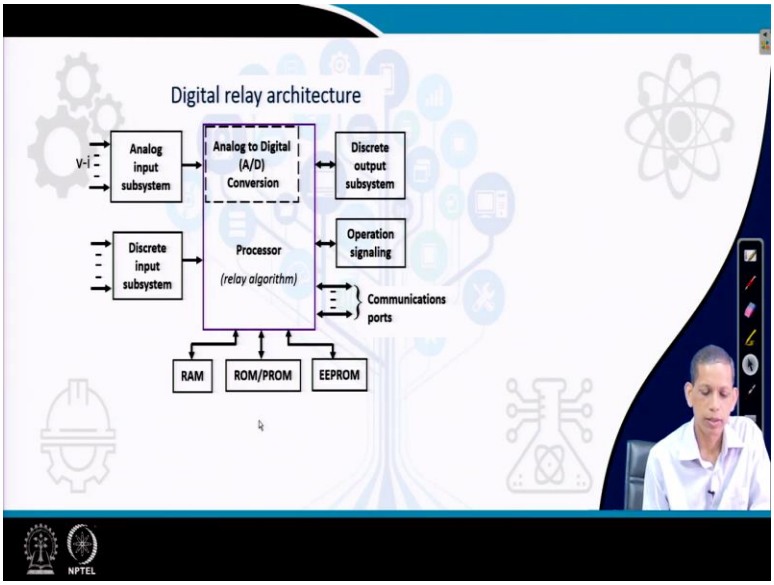

Come to the inside things of a relay; the architecture. So this is the main processor of the relay, where the corresponding relay algorithm or the principle is being executed. This is a numerical platform. It reads the data samples, for that you can say that the relay needs analog to digital conversion, because the signal is analog in nature; currents or voltages. So these currents and voltages are sensed through the CTs and PTs, and they are being input to the relay. So this analog input is converted to a digital platform converted to samples values, and then you can say that the relay processes those samples for a particular decision. Furthermore, the relay can take different signals from other relays also, in the form of discrete inputs. It can makes a decision and communicate to the other relays, or to the subsystem through the different communication ports. Its output can be communicated to the circuit breakers, which it is connected to.

These you can say that the analog input conversions process to the digital form, that is the typical relay processor requires ± 5 V or ± 10 V kind of thing. Therefore, compatibility issue comes into picture due to the corresponding low magnitude signals. Such a processor takes voltage as the input only; therefore, the input signals; currents, voltages must be converted to suitable values; must be scaled down to suitable values compatible to the processor or the hardware architecture of the system.

These processor has different memories, Random Access Memory (RAM), ROM, PROM and EEPROM to take care of the dynamic memory and the permanent memory that in which the corresponding programs and the data are being installed. Note that the relay stores several events. Events means faults or disturbances for further processing of the system.

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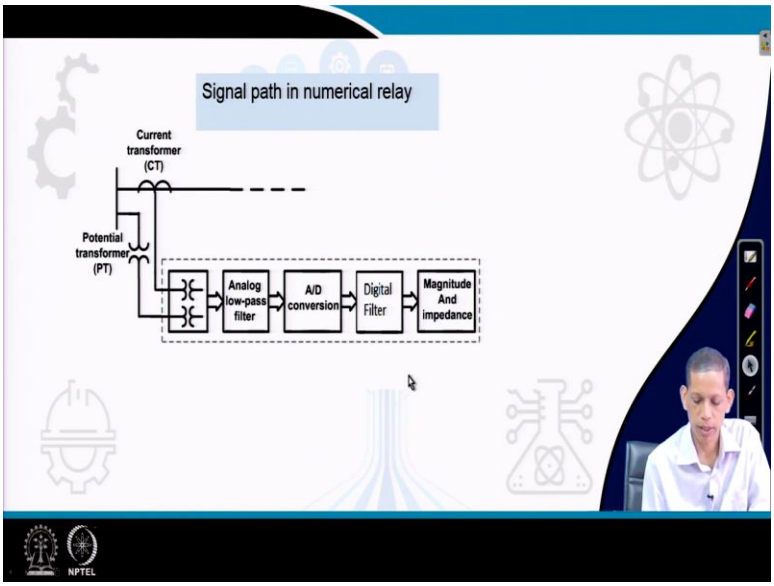

In broad, the signal processing path in a relay becomes like this; we have CTs and PTs, the corresponding sensors or the transducers, those are being used to scaled down the current and voltage signals to the suitable value as compatible to the hardware architecture of the relay, and then you have analog low-pass filter; anti-aliasing filters, we can see that for the efficient processing of the relay that is required; we will address that in later slide. Then we essentially require A to D conversion process, so that the digital signals or the sample values of the signal are being availed by the processor, and then in the processor, you can see that we have these digital filters, where we can extract fundamental, harmonics or any transient or any other components relevant to the relay to decide on the fault. This is the essential in the software part where we program the corresponding principle and embedded it inside. Therefore that algorithm takes the samples value of the current and voltage as required and then it calculates as per the requirement of the relay; like in a distance relay it computes the magnitude of voltage, current and impedance, and makes the corresponding decision process as per the requirement.

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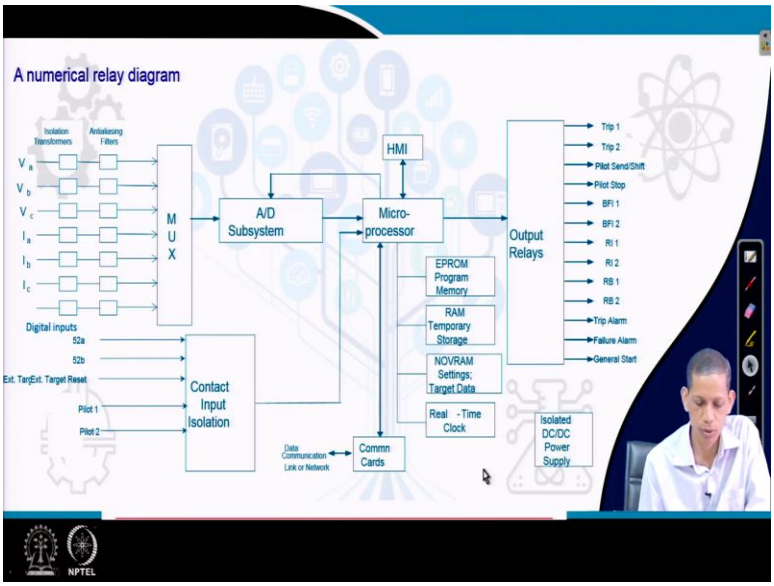

Now if you go into details of the inside things of a relay then here the voltage, currents of three phases, all this six maybe or more currents maybe in a system, or in a differential relay, you can think of all currents from both the primary and secondary side and like that. Signals that are required for the relay are the inputs to the system. We require isolation transformer, because this is a small signal device and in this side much higher voltage appears than the numerical system platform. We require anti-aliasing filters; this is able to pre-filtering in the analog stage of the system. Multiplexer is required, because we have several signals in the analog to digital processing perspective, so that is our requirement. Then this is a processor, which takes the corresponding signal and it requires a different memory, or the storage as per the dynamic processing and permanent storage and so. It has communication cards, to communicate to the outside.

Then as already mentioned, it has different inputs, digital inputs and so to the systems. In the output form, it can communicate to other relays, it can provide informations to the substations and it can provide signals to the LED as in LED information, alarm, and several other things can be integrated to this output module of the relay. Essentially require DC power supply for its operational perspective, or where this DC supply can be taken from an AC source and then converted into DC as per the requirement or can be from a battery source also.

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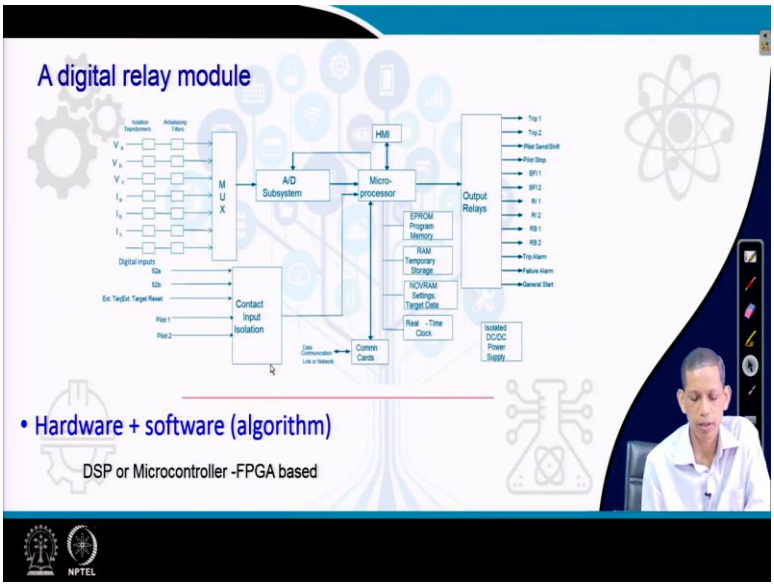

So broadly from this picture, we can say that a digital relay module or a numerical relay module consists of hardware components and also software, but in the software the corresponding algorithm being embedded. This algorithm is nothing but executes the corresponding principle associated with that particular relay. So, if someone is interested, or in the factory the corresponding coding is being done for the particular task. For this the conventional digital signal processor, or microcontroller, or today more and more improved versions are being also available in terms of the FPGA kit and so. This is the evolution of the computer technology. Therefore, with progress in better and better technology available in that perspective, the corresponding numerical relay platform becomes different. Starting from the microprocessor to the FPGA kit, you can see various ones in different older versions to the newer version.

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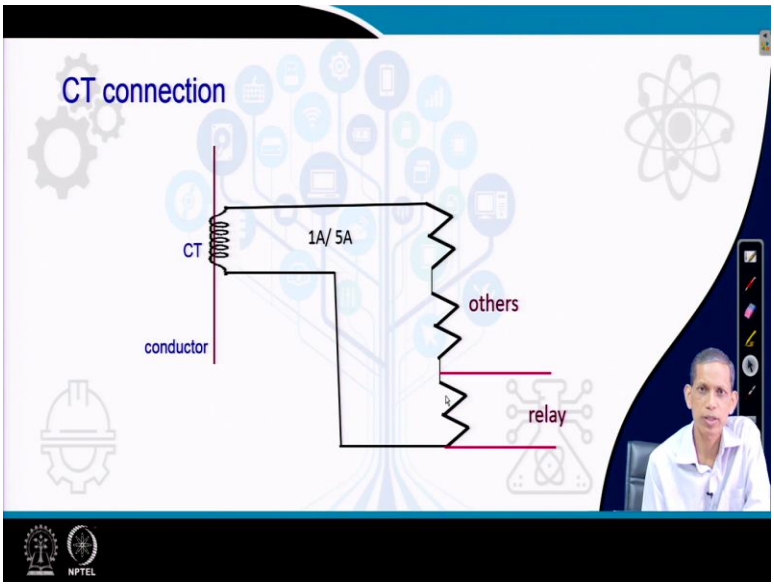

Now come to how the signal is managed in a numerical platform. The current signal has to be converted to voltage signal as input to the kit. So 1 A or 5 A CT is connected to a simple way to different resistances or to the other relays in the series, and then it takes the corresponding output of anyone, that corresponds to the voltage across this part that is proportional to the corresponding current in this path. So to note, CT secondary terminal should be connected suitably to give the corresponding proportionate voltage to the relay.

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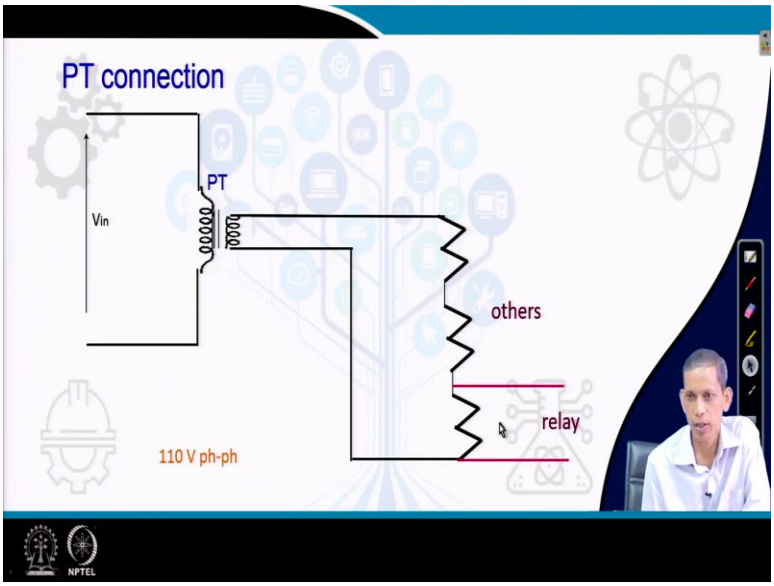

In the PT here, capacitor voltage transducer or transformer in high voltage system, the PT signal is also much higher, typically 110 volt or 120 volt phase to phase. So that has to be down scaled to suitable value compatible to the relay. Therefore a simple way is potential divider connection or any other suitable mechanism should be there. So as far the relay specifications and all these things the corresponding voltage compatible to the relay should be addressed in this perspective.

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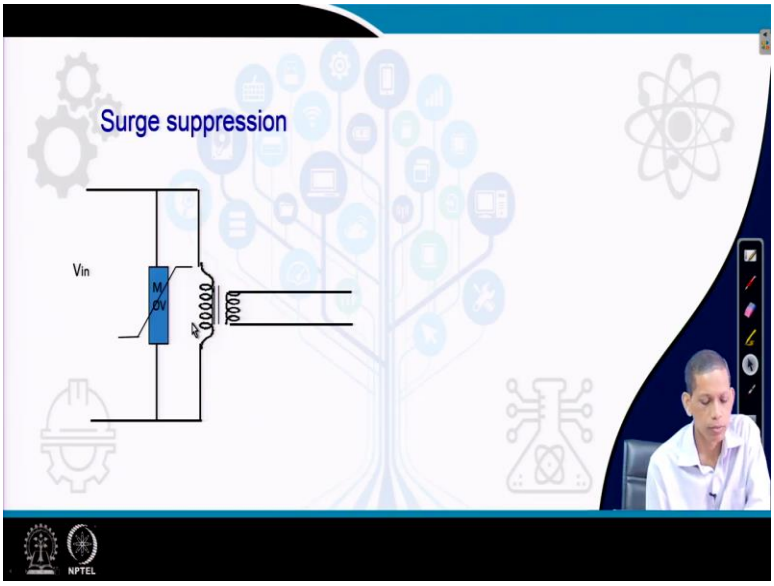

In addition to that, from lightning or surge voltages to protect the system, the Metal Oxide Varistors (MOVs) are being considered, connected in the input side and so also in the output terminals of the analog connectivity to the numerical relay.

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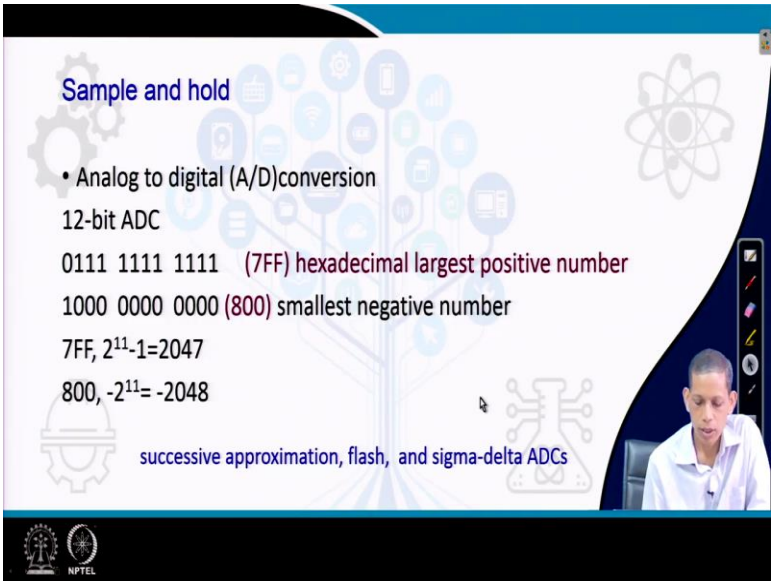

Now come to the analog to digital conversion process, in this case, the simple and whole circuits, what is being done, you can see an example here, the analog to digital conversion process. The relay is having a 12-bit ADC in this case, analog to digital conversion process through this ADC. For this 12-bit, you can express the 12-bit, like this in this format

0111 1111 1111 (7FF) hexadecimal largest positive number

1000 0000 0000 (800) hexadecimal smallest negative number

It means that hexadecimal system the largest positive number can be considered at 2047 and the smallest negative number -2048. So these corresponding whatever voltage input, maximum voltage compatible to that, let us say ±5 V or ±10 V. In case of ±10 V, +10 V can be corresponds to 2047 and the -10 volt corresponds to -2048 in this case. Within that range, the corresponding signal samples are to be manipulated for effective and efficient use of the processor. Different analog to digital conversion (ADCs) principles are there with the evolution of the technology. Earlier versions if you see successive approximations, flash type is a very fast one, and today you can see that many relays use sigma delta ADCs also.

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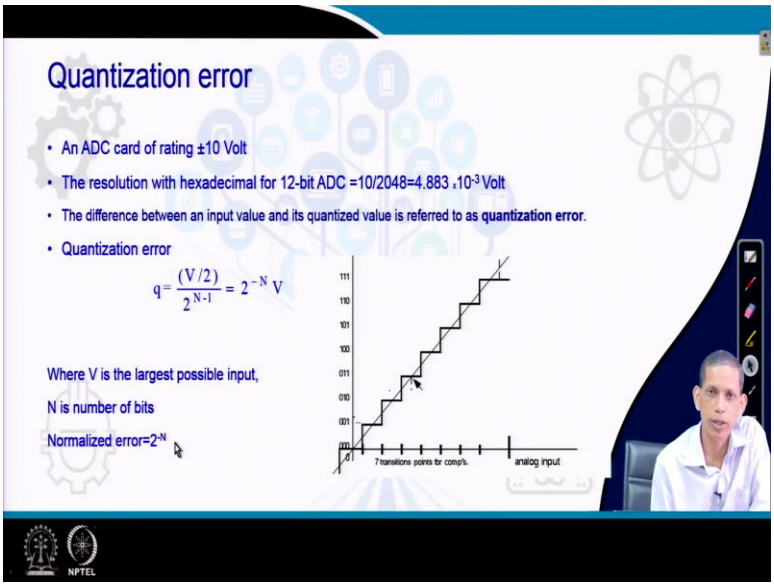

These associated with ADCs there are errors that creep into the digital domain in the further computation and so. Say an ADC rating is ±10 volt range. And suppose we are using a 12-bit ADC, then as already mentioned these (10/2048) gives 4.883×10^{-3} volt resolution. That means between 2 data which will be acquired by such a processor will have an accuracy level of 4.883×10^{-3}. So now this processor is dodged in the former. Let us say we have an analog input signal and this straight line is your analog input signal. Then between the corresponding steps, you can see the perspective, so anywhere analog input signal happens to be there, the corresponding signal value either will be taken at this level or it can be taken into this level. That results in quantization error can be expressed as

$$q = \frac{(V/2)}{2^{N-1}} = 2^{-N}\ \text{V}$$

Where the V is maximum voltage and N is considered the number of bits that is in this case 12. . Therefore V here be +10. If we normalize this, 2^{-N} V divided by V, then the normalized error, quantization error becomes 2^{-N}. Therefore, with increase in value of N, that is number of bits in the ADC becomes more and more, the corresponding normalization error decreases. It means that we will be getting more and more better sample value for the corresponding analog signal.

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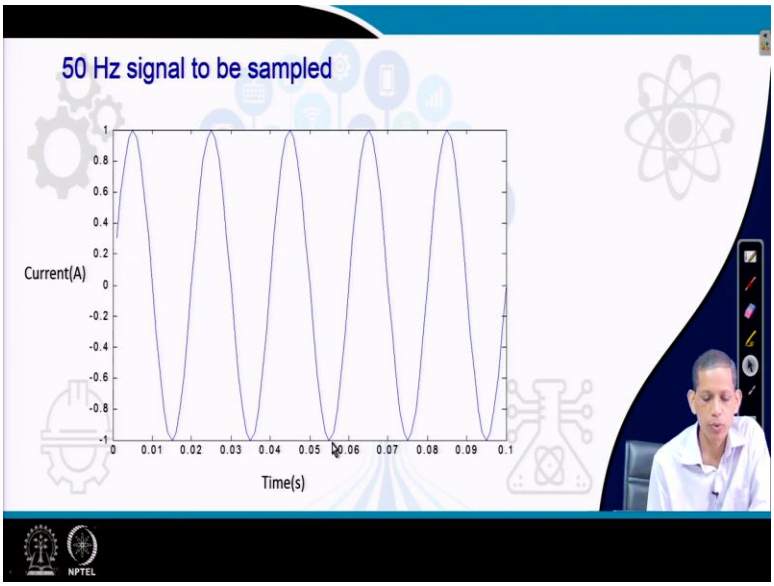

Now next how this sampling is being carried out and what are the corresponding issues, we will see. Let us consider a 50 Hz signal. You can say a sinusoidal signal voltage, current and so. In this case we have shown a current signal. Now these current signal is to be sampled and to be digitized, so that analog to digital conversion process using sample and hold circuits and so.

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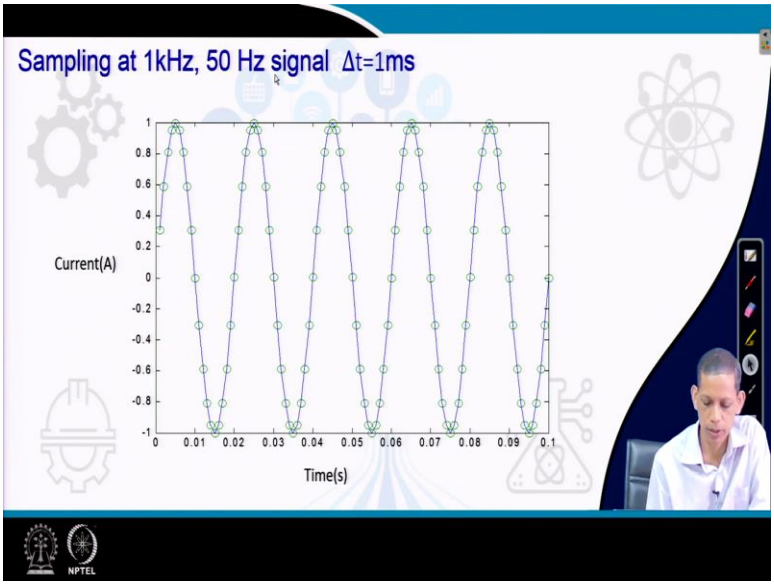

Then at first you can see the example here, now we have a sampling frequency of 1 kHz, it means that 1000 samples per second. So that means for a 50 Hz term which is having a 20 millisecond

(ms) period, the corresponding 1 kHz means the corresponding Δt between two consecutive samples, the time interval becomes 1ms. This 50 Hz corresponds to a time period of 20 ms perspective.

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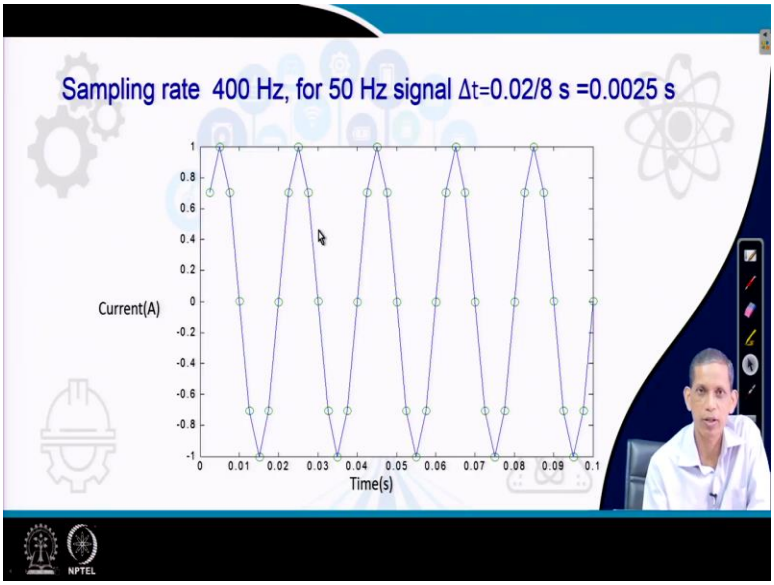

Now let us come to another situation. We have considered only 400 Hz sampling frequency. So that means for the 50 Hz system, we have 20 ms period, so for 0.02 second and these 400 Hz corresponds to

$$\Delta t = \left(\frac{0.02}{8}\right) = 0.0025 \text{ s}$$

It means that it has 8 samples in one cycle and that time corresponds within two consecutive samples 0.0025 s only. So as compared to the earlier case of 1 kHz we have less number of samples in a cycle or in 1 s. So that it is clearly visible from these two pictures.

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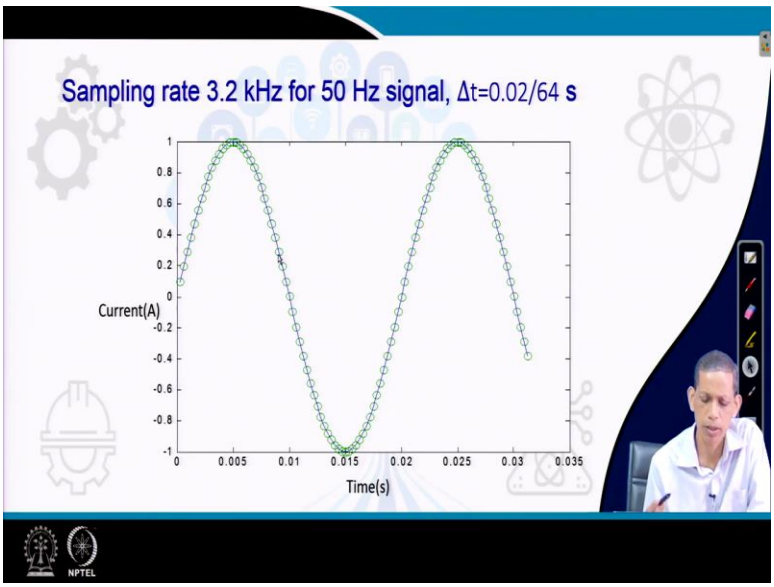

Now comes to the higher sampling 3.2 kHz, much more than that 1 kHz first example. Now for the same 50 Hz signal, and the Δt corresponds to here (0.02 / 64) s. We have 64 samples per cycle that implies the number of samples in one cycle will become much higher, and it is clearly visible that if we like to have more details of the signal we should prefer higher and higher sampling rate for the relay. So this is what we can say that typically today's relay we will see that at a sampling rate at 1 kHz and above, as high as 8 to 10 kHz sampling rate perspective.

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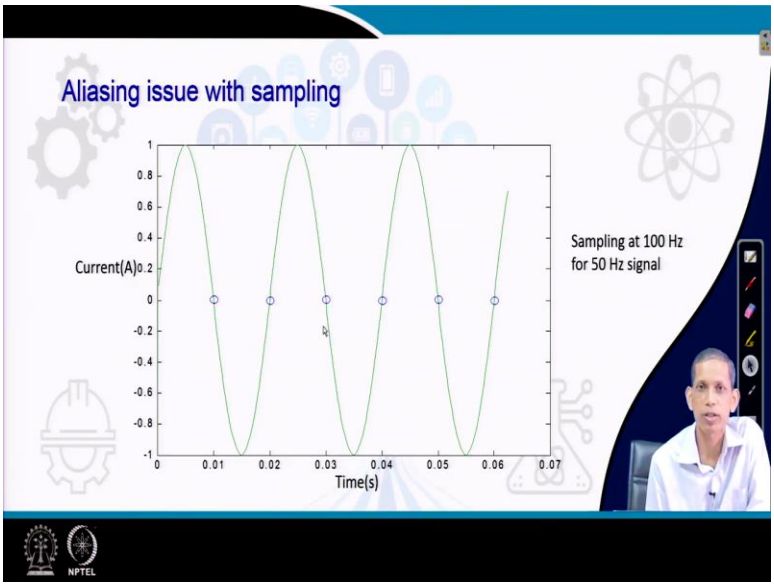

Now the issue with the sampling is, see here, suppose this the same we consider 50 Hz signal and as per the Shannon's sampling, the 50 Hz signal should be at least sampled by twice of the frequency for the fundamental component that is 100 Hz. If you sample at 100 Hz for this one and if you start from this point it will be sampling on 100 Hz, then in every half a cycle will be getting one point and then least situation of only these values will be obtained in the analog to digital process. It means that from these values we cannot interpret the corresponding signal of 50 Hz. So that leads to aliasing issue for the processing systems.

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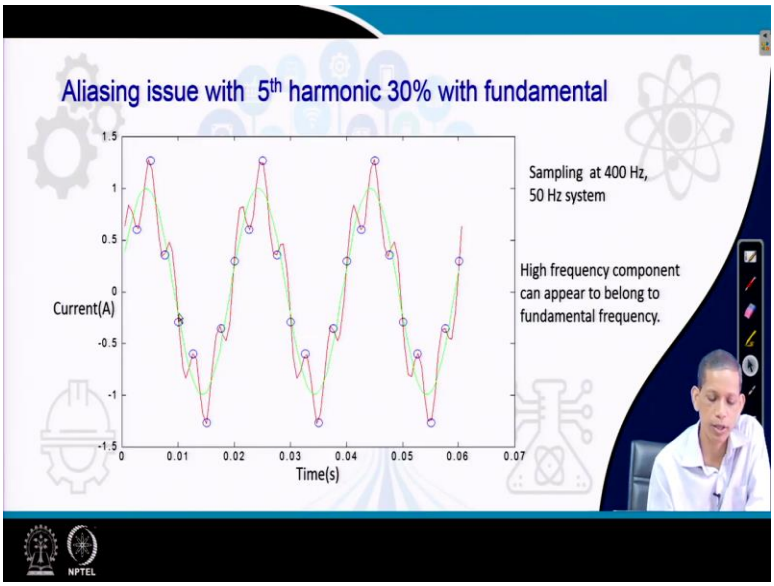

Another issue related to that, let us say that the fundamental signal is the green one and the red one is a contaminated signal of this 50 Hz component, contaminated by fifth harmonic with a 30% 5^{th} harmonic to the fundamental. So let us assume that this is the signal available to the relay in a typical distribution system or so in the current. Now the relay acquires that signals at a sampling rate of 400 Hz, it means that (0.02/ 8) s, then the corresponding samples value which will be acquired will be like this.

From the samples value, if we see, whatever further processing will be accomplished, because these samples values are either lower or higher than the corresponding samples value of the green signal, that is the fundamental signal. So the corresponding computation process will be effected by those erroneous samples in this perceptive and that is what the aliasing issue with the higher sampling frequency components available in the system.

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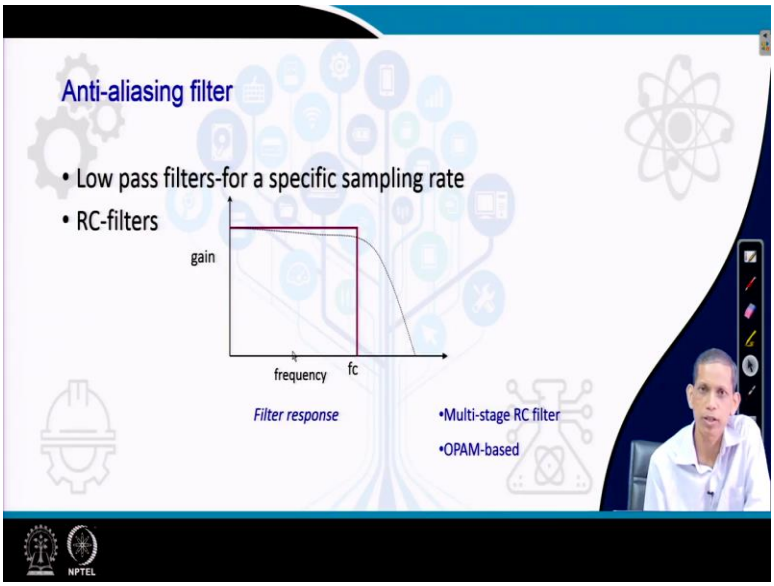

So to overcome this, an anti-aliasing filters are being used and typically what they do is that they filter out the high frequency components from the signal before the analog to digital processing is being carried out. That is what the compatibility, what is the corresponding sampling rate of the DC, and what is the signal frequency of interest to the relay for the further processing perspective; accordingly suitable aliasing filter is being put before the analog to digital processor.

So this is a low pass filter and the low pass filter cutoff frequency is f_c. X-axis is being frequency and Y-axis being the gain of the filter, so an RC filter maybe adequate for this case. In older version of relay uses multiple stages of RC filters are used for effective things. However, more and more stages of RC filters means delay in the acquisition process becomes higher and higher. Today we have OP-AMP-based active filters serving to accomplish this task of anti-aliasing filtering perspective.

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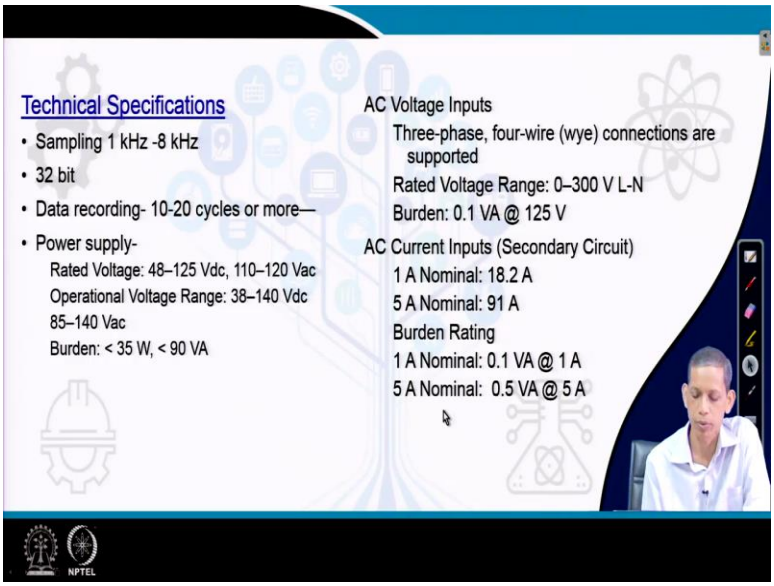

Typically relay specifications have n number of numerous things. For example, we have a typical relay of 1 kHz to 8 kHz sampling rate, a very good relay maybe 8 kHz, very powerful relay sampling perspective, it maybe 32-bit, but older relays consists of 8-bit and so with more and more powerful relays, and cost being lesser and lesser, will find number of bits to be higher and higher in the ADC process and so.

In addition to that, the relay requires data storage; therefore, that is what input and export of a relay. So data recording for each fault event, the relay stores data. It can store several such events in it that also is being specified by the manufacturer. The power supply to the relay can be from the both DC and AC as available, so these are something like a specific relay 48 to 125 volt DC, or 110 to 124 volt AC supply can be good enough for that relay. It is compatible to both.

Then the burden is only 35 Watt from the DC side and less than 90 volt ampere (VA) for the AC voltage perspective. The AC voltage inputs, which the relay can support for this case, for example, three phase, 4 wire input, and the rated voltage can be 0 to 300 volt from line to neutral.

It means that the corresponding voltages are again being considered to scale down to suitable value before the analog to digital process is to be carried out, and the burden is much smaller as compared to the earlier version of analog relays and all these things, only 0. 1 VA for the 125 V input or so.

Similarly the AC currents, the secondary of the CT, can be 1 A, can be 5 A for the same relay, and in case of 1 A, the maximum current matching to that relay is 18.2 A, for a 5 A it becomes 91 A. This is an example for a typical relay. The burden rating for the CT is also pretty low, 0.1 VA for 1 A and 0.5 VA for 5 A. So these shows that some of the technical specifications of a typical relay perspective.

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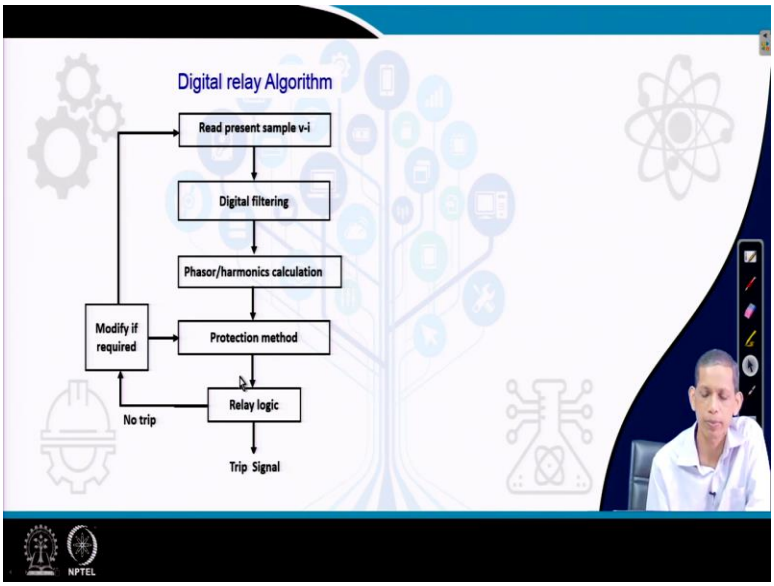

Now come to the software, the domain where the numerical relay executes the corresponding algorithm. So it reads the corresponding voltage and current samples, all three phases, or single phase, or whatever as per the requirement of the relay. Then it accomplish the corresponding digital filtering parts. In the digital filtering, there can be several steps, including the corresponding process of discarding the different unwanted components, and next finding out the component corresponding phasor or component that is fundamental component or require harmonic and so like in a transformer protection. After evaluating all the different components of the signal, the relay goes for applying its principle on the protection method. Like overcurrent principle, differential principle, or distance relay and so.

Then in that protection methods it finds whether the fault is inside the zone or so, and if it is so, it provides the trip signal to the circuit breaker or tripping, or it can communicate to the other relays and substation perspective and so. In case of the corresponding relay, if it is a no case, then it can

go on continuous reading of those samples, or it can also modify the corresponding settings of that prospective depending upon the system condition and so in the firm up and adaptively.

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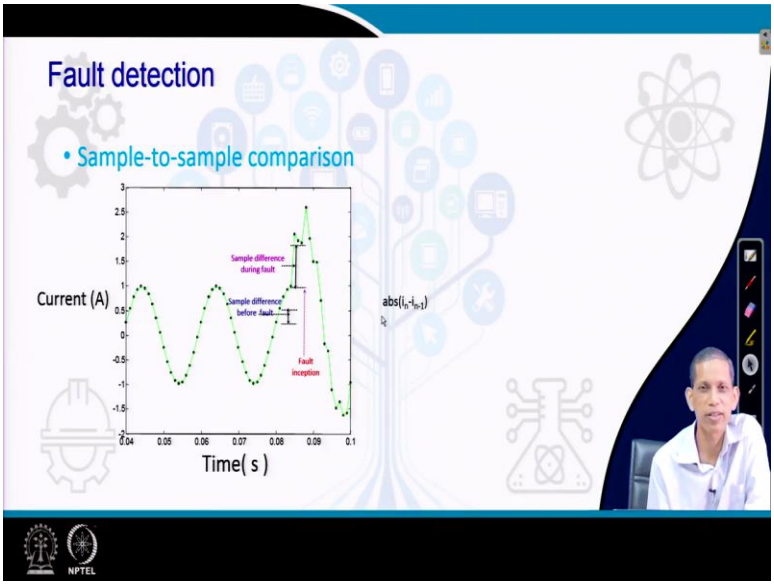

Now coming to how the corresponding sample values are being useful in the relay process and so. Before going to the more details in further in subsequent lectures and so, let us see these, in current signal, at these point, where fault inception has occurred, you can see that, after that, the corresponding current signal jumps to a higher value.

So these sample values are being acquired through an analog to digital processor ADC and once these sample values are there in the relay, in the software; the principle in the relay executes the different algorithms. Therefore, if we see this is a fault detection process only to know whether the fault is there or not. After that the relay can do the sophisticated algorithm for decision, whether the fault is inside the zone or beyond the zone and so. This is a very simple step, and very widely used in many of the relays to trigger the fault event and so. Here the fault is incepted and then you can see the next sample the corresponding jump in current is very large. Whereas, within two consecutive samples in this case before the fault, the corresponding current change is smaller. That going to the principle called a sample-to-sample comparison. If you go, then $| (I_n - I_{n-1}) |$, where n corresponds to the present sample value minus just the earlier sample value. Then you subtract and take the absolute value, you can see that during the fault this change is much significant as compared to the pre-fault case. Therefore, whenever this change is significant, use a suitable

threshold for the purpose. Whenever this corresponding change becomes significant, the relay declares that this is a fault situation and then accordingly further activities can be carried out.

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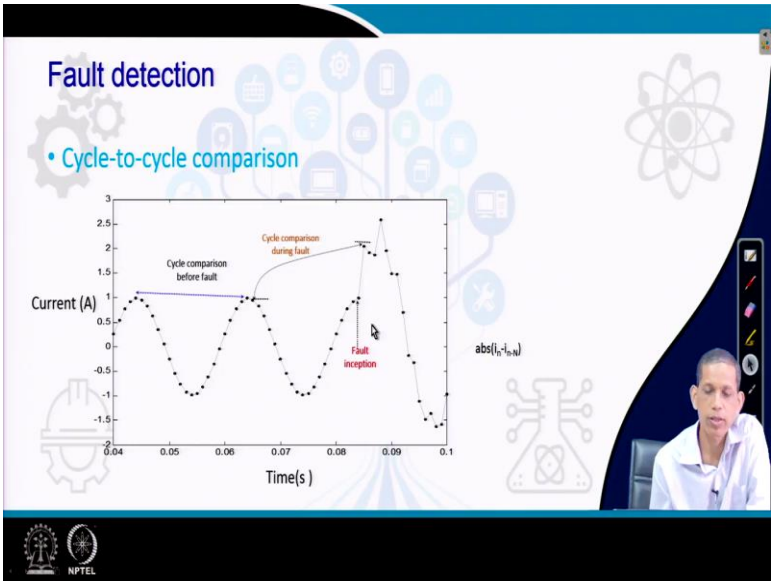

Similarly we know that in a typical power system, let us say 50 Hz signal, this is current. So it maintains its periodicity between a present current sample and one cycle earlier sample, this will be same in general in a normal situation. So that leads to $| (I_n - I_{n-N}) |$ where capital N here corresponds to one cycle, that is period.

So in one cycle period, these difference should be zero or very near to zero. Whereas in case of a fault inception at this point, then these corresponding point and one cycle earlier point, then the corresponding difference between the point in the fault region and the point in the pre-fault region, this difference will be much higher. So if the corresponding detection process uses this cycle-to-cycle comparison of the samples and finds the absolute value and then normally it should be zero or very near to zero, and whenever it enters the fault region, this value will be significantly high. So this also can be used in the fault detection process.

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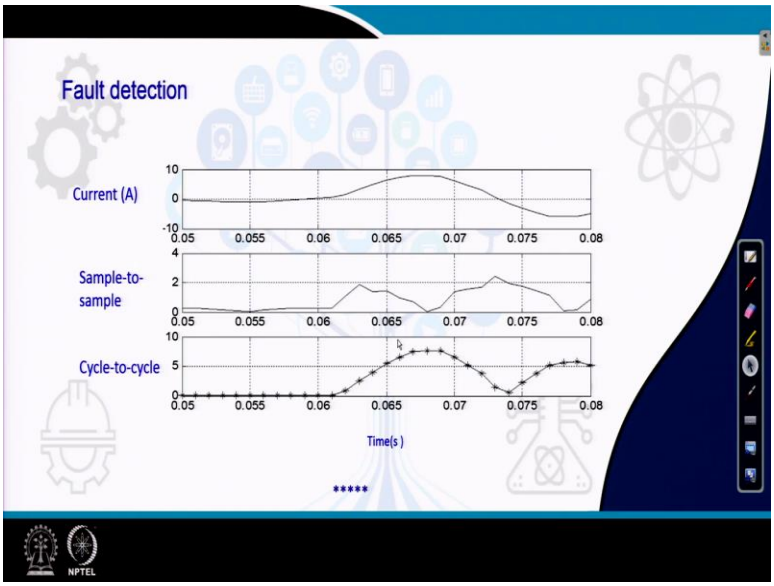

Now if we compare these two fault detection principle, sample-to-sample and the cycle-to-cycle, whenever a fault has happened, these current signal in a fault situation, the corresponding sample-to-sample rises and again like this and so also the cycle-to-cycle process rises. Note that such principle is useful only to trigger the initial following the inception of the fault as fast as possible.

So this kind of simple principles can be used effectively successfully for fault detection process, what we demonstrated here, that how these sample values are being used in the relay. In the subsequent class, in the lectures, we will see how these samples are further processed for different other computations and effectively used.

Note that the relay acquires a new samples and computes such fault detection process, but in between it computes further things and uses its digital filtering, the filtering algorithms and the corresponding principles which it uses and then makes a decision before the fresh samples are being acquired in the process. So in the next lesson, we will discuss about phasor estimation technique. Thank you.