

Digital Control in Switched Mode Power Converters and FPGA-based Prototyping
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Module - 08
Digital Controller Implementation using Fixed-Point Arithmetic and Verilog HDL
Lecture - 74
Digital PID Controller - Hardware Implementation and Experimental Results

Welcome, in this lecture we are going to discuss Digital PID Controller-Hardware Implementation in digital voltage mode control buck converter and some experimental results.

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Concepts Covered

- Digital PID Control using Verilog HDL Programming
- Experimental Case Study of a CCM Buck Converter

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So, in this lecture, we are going to talk about digital PID control using Verilog HDL programming, and this programming part we have already discussed. So, now, we are going to implement this digital PID controller in a voltage mode control continuous conduction buck converter.

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Digital VMC in a Buck Converter – Practical Details

Power Stage Details

Inductance L	1.8μH
Capacitance C	200 μF
Input Voltage V_{in}	3.3V
Output Voltage V_{ref}	ε [1,1.1]
Switching Frequency f_{sw}	200kHz
Load resistance (R_c, R_{sw})	(13.5Ω, 0.33Ω)

So, if we recall our digital voltage mode control this we have discussed multiple times. So, what are the practical details that we have considered? So, in this particular hardware prototype, we have considered a 1.8 microhenry inductor, then 200 microfarad capacitor and it is tested at 3.3 input voltage, and the output voltage is considered between 1 to 1.1 because we will be showing also reference transient where we are changing voltage from 1 to 1.1.

But our nominal voltage is 1 volt and the switching frequency is 200 kilohertz we have considered two discrete load resistance one is a continuous load resistance the other is a switch for example, you know we are talking about the output side of the buck converter. So, here we have a continuous load which we call R_c and there is a switched load which is connected to R_{sw} and this is connected to the Q load that we discussed in the previous lecture.

So, if the Q load is 1 then R_{sw} will come parallel to R_c and the effective resistance will be smaller. So, it will make a load step of transient and if we disconnect R_{sw} then R_c will come into the picture the load resistance will increase overall load resistance will increase. So, it will make a load step-down transient.

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Digital VMC in a Buck Converter – Practical Details

Controller Details

Proportional gain K_p	1.25
Integral gain K_i	0.13
Derivative gain K_d	8
ADC resolution	10 bit / 9 bit
DPWM resolution	9 bit
Controller clock f_{clk}	100MHz
Voltage feedback gain k_f	0.27
Ramp voltage V_m	2V

And in this lecture we also considered I mean what we discussed in the Verilog module when we wanted to write the Verilog module. But before that, we also discussed the ADC converter. So, the proportional gain we have considered inside this controller K_p to be 1.25 K_i this is all discrete-time integral gain 0.13 and discrete time derivative gain K_d that is 8. So, we have 8 bit a d 10 bits of ADC, but we are discarding 1 bit. So, we are representing 9 bits or you can make it 8 bits and the DPWM resolution is 9 bits.

So, typically ADC resolution should be smaller than DPWM, but with 9-bit ADC we are not getting a significant effect of the limit cycle. So, there is slight instability there so, but you know one can choose the 8-bit only thing you will lose is the resolution. So, one way we can increase the DPWM resolution is by increasing the clock, but we have you know limitation of the controller clock which is only a 100 megahertz clock is available.

Then our voltage feedback gain because we are stepping down using a resistive divider and this we have got near about 0.27. So, that is the voltage feedback gain and the RAM voltage that we are considering because inside the digital controller, we are considering this short tooth waveform which is a steer case kind of thing and for the corresponding q format we got the real voltage to be V_m to be roughly I would say not exactly 2 volt. So, this is a RAM voltage.

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Digital PID Controller Gains

$G_c(z)$

Proportional gain K_p	1.25
Integral gain K_i	0.13
Derivative gain K_d	8

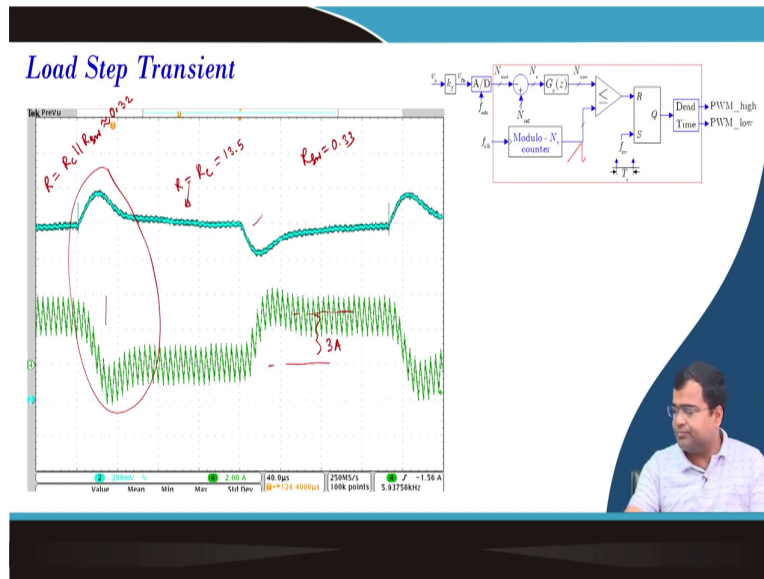
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//PID controller gains
parameter K_p=10'sb0001_010000; //Q4.6 signed format
parameter K_i=10'sb0_001100011; //Q1.9 signed format
parameter K_d=10'sb0111_111111; //Q4.6 signed format
    
```

Now, we have discussed that the digital PID controller is the implementation and we have also implemented MATLAB in week 3. So, this is the proportional gain this is a discrete-time integral gain and discrete time derivative gain in the Verilog, we said these are the parameter and for K_p we have used Q 4.6 and that is why K_p is coming to be 1.25 because if you see the integer bit it is in that 2 to the power 0 location.

So, it is 1 and this is in 2 to the power minus 2 so; that means, 0.25 and integral we are getting roughly this is q 1 dot 9 we are getting 0.13, and the all bits this is Q 4 dot 6 the sign bit all cases are 0 because all positive gain and then rest of the thing this K_d is approximately equal to 8 ok that we have discussed. So, these are the proportional integral and derivative gains. These are all discrete domain digital controllers.

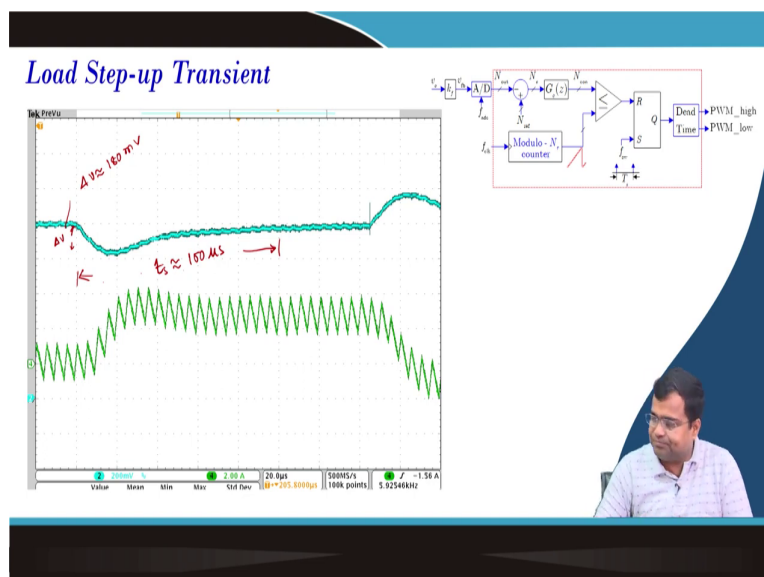
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Now, we have made a load step of the transient. So, we are again in this case we are making a load step down so; that means before this our load resistance was continuous resistance in parallel with R_{sw} and which was approximately coming to zero point sorry 0.32 0.32, and here it is only $R_s R_c$ which is R equal to that is 13.5.

So; that means, we are making a load transient of almost because our R_{sw} is 0.33 and our reference output is 1 volt. So, we are making effectively making a load transient of nearly 3-ampere load step. So, here it is a step-down transient this is a step-up transient.

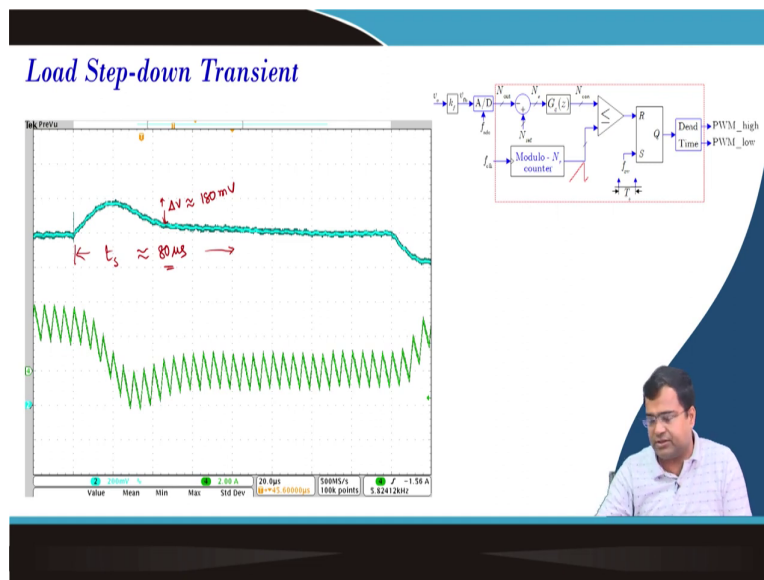
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And for more detail if you consider step-up transient, then we are getting an undershoot of nearly; that means if you consider this undershoot. So, this is coming to be Δv coming to be Δv is approximately equal to 180 milli volt which is large we can always decrease it by setting the suitable controller gain and we will be discussing the design case study in the subsequent week.

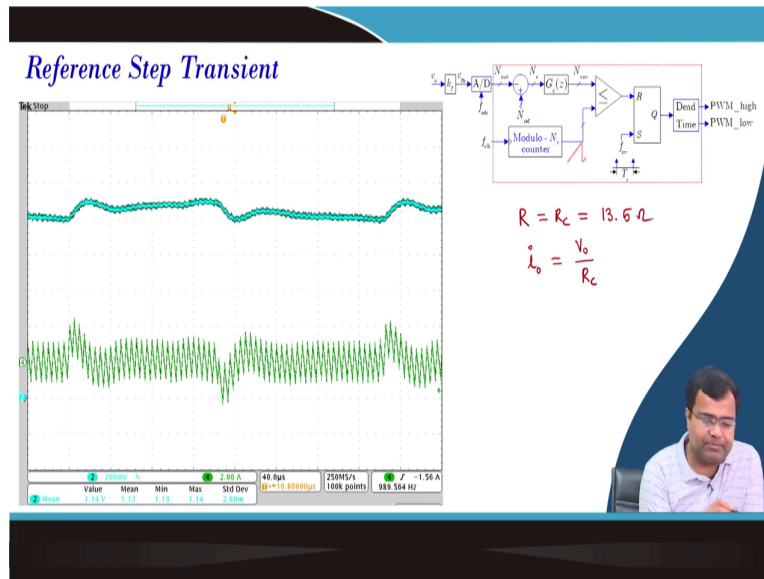
And this settling time is coming to be up to this and each division is 20 microseconds we are getting 1, 2, 3, 4, 5 so; that means, it is settling time is roughly around 100 microsecond and which is like 20 cycles because 5 microsecond is my time period.

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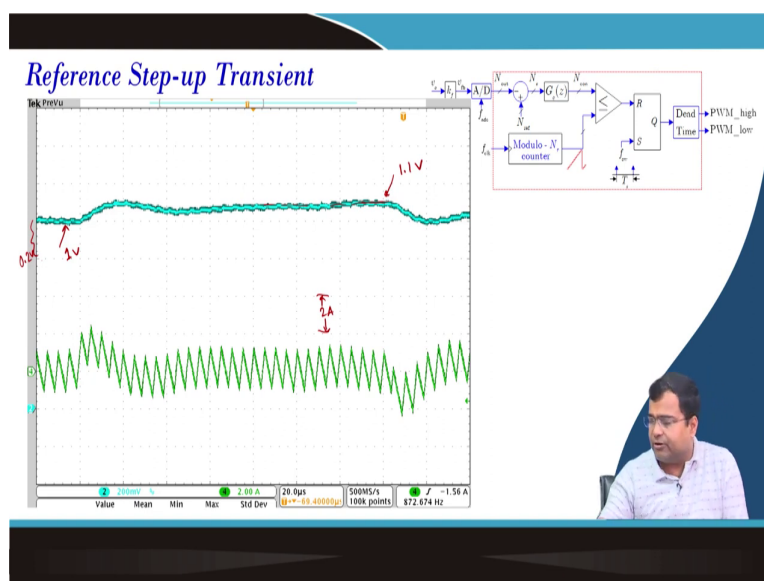
If we zoom the load step-down transient then we will get this overshoot which is also approximately 180 milli volt which is also large we can reduce it and we will show in the subsequent case study how can you make it faster when you go to design. And the settling time that we are getting which is t_s it is up to this point. So, in this case, we are getting equal to 80 microsecond which means 16 switching cycles and we can make it much faster.

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Now, we are considering reference step transient, and in this case, we have set the load resistance at t is R c value which is nothing, but 13.5 ohm. So, our load current depending upon the output voltage will be RR c. So, for a 1-volt nominal voltage. So, the nominal load current for this case; that means, if you set V 0 to be 1 volt then it will come around 70 to 75 you know milliohm milli ampere sorry milli ampere. But you can see we are making a load step-up transient. So, this is step up and step down.

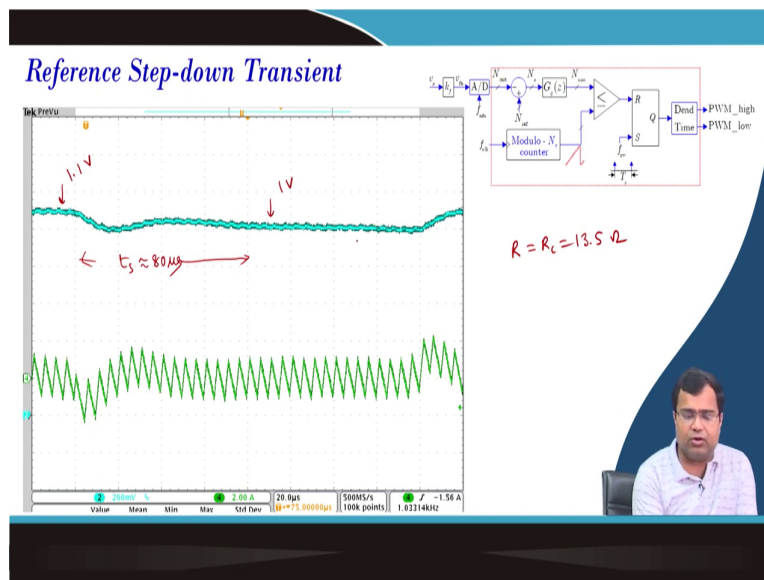
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And if you go to the zoom version of the step-up transient. So, this is roughly around it is not exactly what it is reaching here. So, this voltage is 1.1 volt and this voltage is 1 volt because this axis is 0.2, this is 0.2 volt per this is a 0.2 volt because we are talking about voltage axis in this case and the current axis this to this is our 2 ampere and our ripple is also more or less 2 ampere.

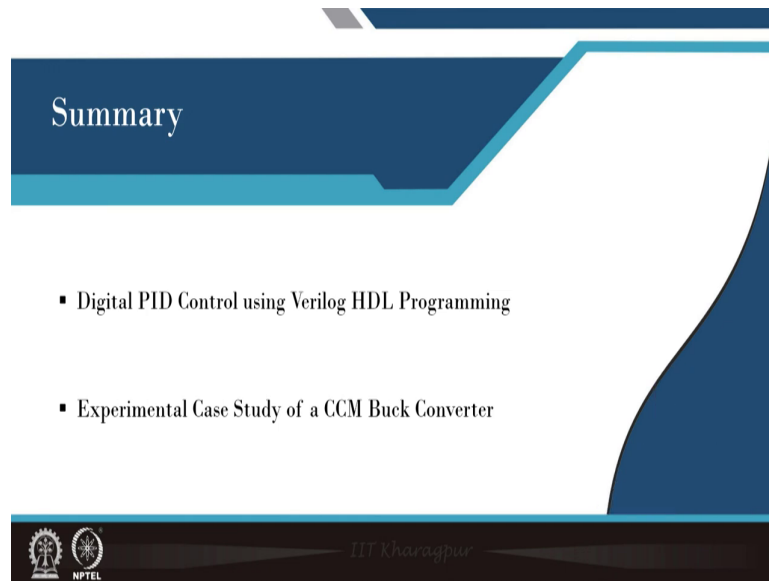
So, it is there is a slight overshoot, but it is taking a somewhat longer time to settle it is going close fast I mean within like a 20 within 20 microsecond, but there is a slight undershoot overshoot with respect to the new reference voltage. So, it is taking somewhat more time to reach the steady state value.

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Similarly, if you take the reference to step down transient, for all these cases we set load resistance to be R_c equal to 13.5 ohms and it can be shown that this is our 1.1 volt and this is our 1 volt. So, it is taking roughly 80 settling times like almost 80 microsecond and there is a very slight and there is no such undershoot and it is coming.

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Summary

- Digital PID Control using Verilog HDL Programming
- Experimental Case Study of a CCM Buck Converter

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So, in summary, we have discussed the digital PID controller and its hardware implementation and we have discussed the PID controller programming in the previous lecture we have shown an experimental case study of a continuous conduction buck converter using a digital voltage mode controller. So, we have discussed the digital PID controller implementation of digital voltage mode control. So, in the next lecture, we will go for mixed-signal current mode control where we will apply digital P I control.

Thank you very much.