

Analog Integrated Circuits
Prof. S. Aniruddhan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture - 11
Differential amplifiers

In this lecture we are going to look at class of amplifiers called the differential amplifiers. So, the motivation for this class of circuits comes from the fact that we are trying to design op amps.

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Differential Amplifiers

$V_o = A(V_A - V_B) = A \cdot \Delta V$ We need a "differential amplifier"

$$V_1 = \frac{V_1 + V_2}{2} + \frac{V_1 - V_2}{2} = V_{CM} + V_{DM}$$
$$V_2 = \frac{V_1 + V_2}{2} - \frac{V_1 - V_2}{2} = V_{CM} - V_{DM}$$

$V_{CM} = \text{avg voltage}$

$V_{DM} = \frac{1}{2} \times \text{diff. voltage}$

So, if you actually look at an op amp. So, it of course, has 2 inputs let us call that V_A and V_B , and let us say the output is V_o the output of the op amp is related to it is input through some very large gain A times V_A minus V_B . So, in other words if the input was some ΔV , the op amp output is related a or is a large gain applied to that ΔV alone.

So, in other words the op amp should not care about what the absolute values of V_A and V_B are, it only cares about the difference between these 2 quantities. And therefore, we want to build a circuit that amplifies only the difference between 2 voltages, and such an amplifier is called differential amplifier. So, we need a circuit called a differential amplifier, this is something that amplifies selectively amplifies the difference between 2 signals, now let us assume we have 2 voltages V_1 and V_2 .

Now, before we go to the circuits portion, we will quickly see how we are going to use these 2 voltages to be applied to the circuit. Now what I am going to do? I am going to write these voltages as a combination of 2 quantities, and I am going to write it in this way I am going to write V_1 as the sum of $V_1 + V_2$ by 2 and $V_1 - V_2$ by 2. So, clearly any voltage or any pair of voltages V_1 and V_2 can be decomposed in this manner. So, V_2 of course, will be $V_1 + V_2$ by 2, minus $V_1 - V_2$ by 2 and any pair of voltages can be decomposed in this manner.

Now, $V_1 + V_2$ by 2 is also called the common mode voltage V_{cm} , and $V_1 - V_2$ by 2 is often called the differential mode voltage V_{DM} . As you can see now V_{cm} of course, is the average voltage, it is $V_1 + V_2$ by 2. So, this is the average of the 2 voltages and of course, V_{DM} is the half the difference between the 2 voltages. And normally during small signal operation that difference between these 2 voltages is expected to be quite small right. So, let us now start looking at a circuit that is going to give us this difference is going to amplify the difference between 2 voltages.

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The slide contains the following handwritten content:

$$V_1 \rightarrow V_{01} = kV_1 +$$

$$V_2 \rightarrow V_{02} = kV_2 -$$

$$V_{01} = V_{0CM} + V_{0DM}$$

$$V_{02} = V_{0CM} - V_{0DM}$$

The circuit diagram shows two identical common-emitter amplifier stages. The first stage has input V_1 , a resistor R , and a MOSFET M_1 with output V_{01} . The second stage has input V_2 , a resistor R , and a MOSFET M_2 with output V_{02} . The gates of M_1 and M_2 are connected to a common-mode input V_{0CM} . The drain nodes of M_1 and M_2 are connected to a differential-mode input V_{0DM} . The slide also features an NPTEL logo and a small video inset of a man in a green shirt.

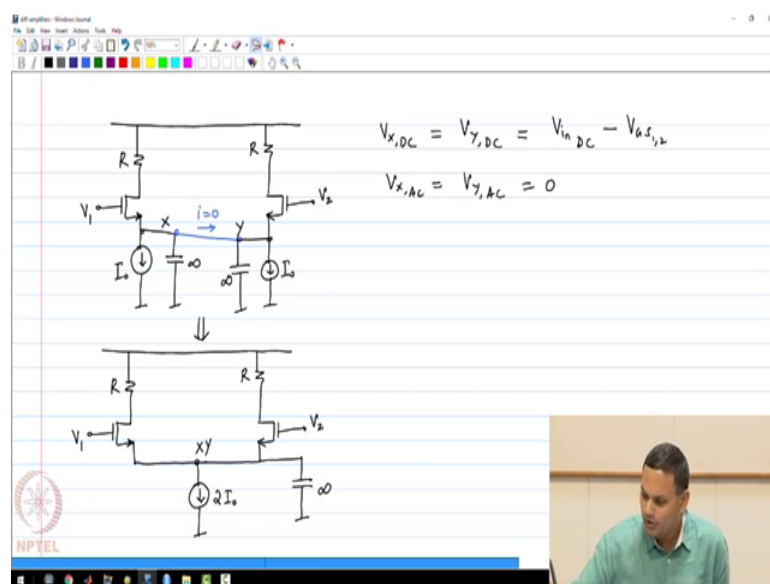
So, so far we know all of you know how to build amplifiers that will amplifier particular voltage. So, let us say I had an input V_1 , the output V_{o1} is sum k times V_1 this is an amplifier of gain k . Now suppose I want to build a differential amplifier, I will first start off in this manner, I will take the second voltage V_2 applied to an identical amplifier of gain k .

So, these 2 amplifiers are identical, the second output V_{o2} is going to be k times V_{o1} . And now I am going to define even though in the op amp I required only a single ended output, for now I will assume it can be it can somehow be in done for now I will assume that I can define the actual output voltage V_o as $V_{o1} - V_{o2}$, I am going to use the voltage as the difference between these 2 voltages ok.

However, please note that in reality I have 2 output voltages V_{o1} and V_{o2} , I can now decompose these 2 output voltages V_{o1} and V_{o2} as the sum and difference between the output common mode and differential mode voltages. It is only when I take the difference that I get this V_{oDM} . So, this is still not where I wanted to be; how will I build this amplifier? Now let us assume you are trying to build an op amp where you need large gain and therefore, the circuit that you are trying to build that will have large gain is probably a common source amplifier.

So, I am going to start with a common source amplifier let us say it has a resistance R , I know that the output voltage is related to the input voltage in a certain way for this amplifier. I am now going to take the second amplifier remember that it is identical. So, M_1 and M_2 are identical the 2 resistors are identical. So, this is my second circuit. Now you also know that these 2 transistors need a bias point which will require stabilization. So, we will make the circuit a little bit more closer to reality.

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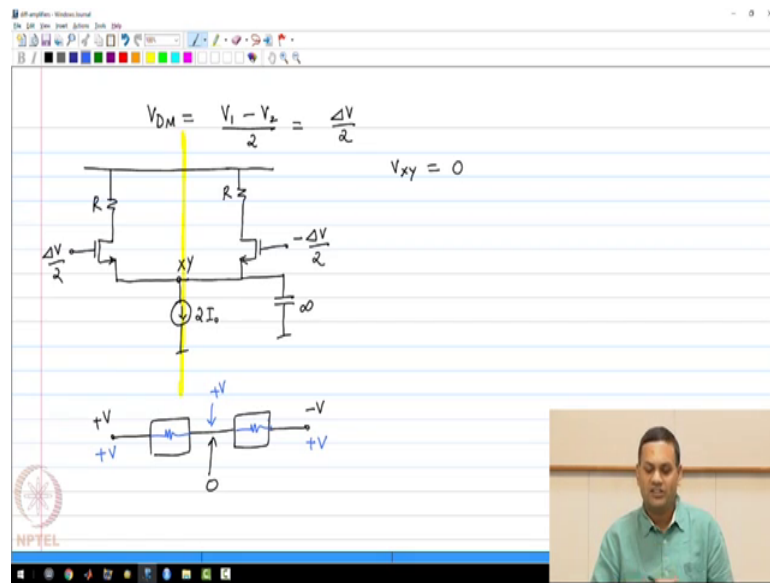
So, one of the most common ways of doing bias stabilization is to add a current source and add an infinite capacitor in parallel with it.

So, that the current source which will call I_{naught} bias is the transistor, but for small signals the sources grounded. On the other side we will need an identical amplifier which I am drawing here. Now I am let me call these nodes x and y , the source nodes of M_1 and M_2 . If you look at the dc voltage at nodes x and y both of these will be equal to the input DC minus. So, this is the DC bias voltage applied to the gates of the 2 transistors, minus the gate source voltage of 1 and 2 which are supposed to be identical. So, the dc voltage at x and y are the same.

Now, what about the AC voltage? Now it turns out that for AC because of the infinite capacitors both of these nodes are at small signal ground. So, therefore, if I actually make a short circuit I take an ideal wire, and connect these 2 voltages this wire will carry 0 current. So, it will not change the circuit in any manner, the voltages will not change and the currents in the circuit will not change. So, now, this circuit can be redrawn in a slightly better manner. So, I will do that here. So, let us look at this new circuit where I am to combine the 2 current sources and show a single current source at the common source node. And let this common source node be x y , and I have 2 current sources in parallel. So, they will become a single current source of value $2 I_{naught}$.

And this circuit I will of course, have an infinite capacitor at that node now let us look at the circuit in a little bit more detail. If I have 2 voltages V_1 and V_2 I can decompose them as the common mode and differential mode components, since we are interested in the differential mode. So, this is the differential mode voltage that is being applied.

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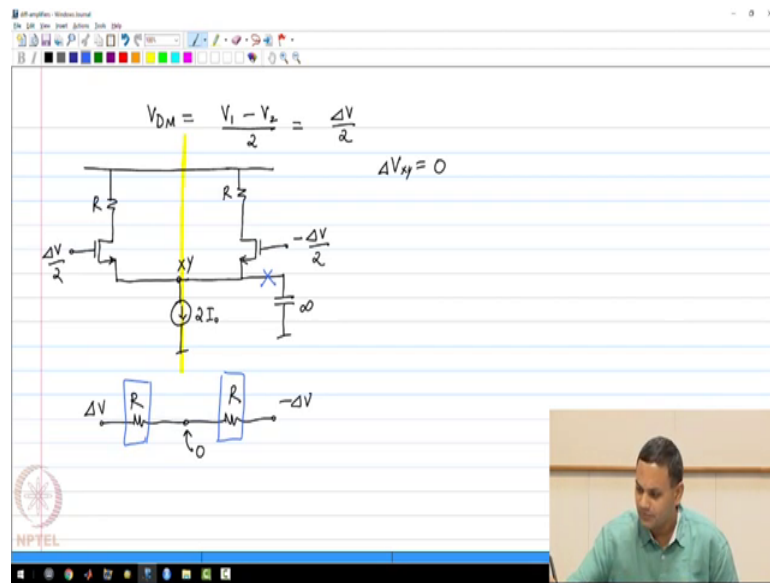


So, this is $V_1 - V_2$ by 2, and I am going to call that some ΔV by 2. So, I take this circuit and I am going to apply ΔV by 2 and minus ΔV by 2 to the circuit.

So, remember V_2 is $V_{cm} - \Delta V$ by 2 I am looking only at the differential mode component what happens to V_{xy} ? So, clearly if I look at the V_{xy} under this condition, you can show that along the line of symmetry all the voltages will be 0. This is this can be shown easily suppose I take 2 equal and opposite networks, and create a line of symmetry and if I have voltages plus V and minus V on either side, I can show that along the line of symmetry I need to get 0 volts.

Similarly, we will be using this result in a few minutes, if I were to apply plus V and plus V on both sides, I can show that I will get plus V on this side also if I have a resistant network. If you have a more complex network, you might have some common voltage at that node. If you look at the voltage at node V_{xy} when you apply ΔV by 2 and minus ΔV by 2, we need to find out what does voltages as of now we do not know what this voltages. So, let us say we are going to look at nodes along the line of symmetry.

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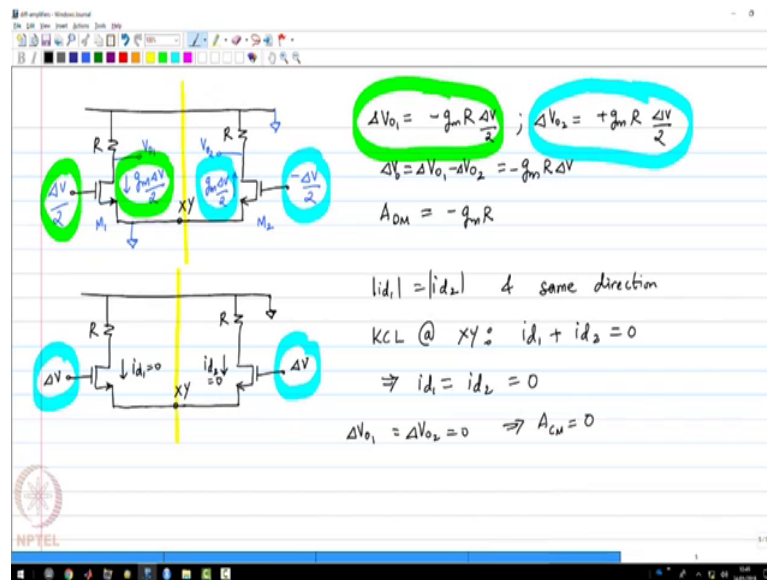


So, let us take an example of the simplest possible resistor network that you can think of; let us say you apply delta well let us say you apply delta V and minus delta V, and let us say the resistor network is identical on both sides.

You will of course, find that the intermediate point is at ground, and this is true even if the network gets fairly complex. So, therefore, purely from symmetry you take a circuit that is symmetric about a particular centre point, and you apply a positive voltage on 1 side and a negative voltage on the other side. You can say that along the line of symmetry you are going to have a voltage that is 0. So, in other words the first result that we will write is that delta V x y is now 0. In other words when you are applying a differential voltage delta V by 2 and minus delta V by 2, x y is going to be at small signal ground.

Once you establish this you no longer have a need for this capacitor. So, the next version of the circuit that we are going to see will not have this capacitor, because we already have a small signal ground at x y purely from the point of view of symmetry.

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Now please note that you can also come up with a same result that V_{xy} has to be 0, by writing down the current and voltage equations, but I am choosing to do it purely from symmetry instead of doing it analytically.

So, this is the version of the circuit that we are now going to see and. So, we are applying ΔV by 2 and minus ΔV by 2 for the circuit, and we know that this circuit is going to have a small signal ground or incremental ground at this node. We know that the current source would be an open circuit. Now this is a fairly simple circuit to solve if you look at the current through M_1 , the current through M_1 is nothing, but $g_m \Delta V$ by 2 in this direction and the current through M_2 is minus $g_m \Delta V$ by 2 in this direction or plus $g_m \Delta V$ by 2 in this direction.

Where do we take the output? We actually take the output at as the difference between the 2 drains. So, this is V_{o1} , this is V_{o2} , and V_{o1} is nothing, but minus $g_m R \Delta V$ by 2 and V_{o2} is plus $g_m R \Delta V$ by 2. So, finally, V_o is taken as the difference between V_{o1} and V_{o2} this is nothing, but minus $g_m R \Delta V$. So, now, you see that this circuit. So, in fact, I am going to write this as ΔV_o because we are dealing with incremental quantities.

Now, this particular circuit has the same gain as the single ended common source amplifier that we saw earlier. So, the gain the what we call the differential mode gain is nothing, but minus $g_m R$. So, it has very large gain in the differential mode, we now

need to see the performance of the circuit with a common mode signal being applied now let us look at the common mode analysis.

Now, for the common mode analysis I am going to apply ΔV voltage to both sides of the circuit. Now if you look at the common mode version of the circuit, if you look at the line of symmetry you can no longer say that the circuit will have a small signal ground at that node.

However what you can say for the circuit, you can say something analogous to what you saw in the differential mode circuit. Now what did we see in the differential mode circuit if you actually look at the differential mode circuit, if you look at the left half of the circuit you have a $\Delta V/2$ being applied to the gate of M_1 that is here, you have a $g_m \Delta V/2$ flowing downwards, and you have a voltage V_{o1} that is $-g_m R \Delta V/2$. If you look at the right hand side of the circuit all the voltages and currents are equal in magnitude, but opposite in direction. So, you can see that $\Delta V/2$ being applied to the gate, the current is $g_m \Delta V/2$ and finally, the output voltage that is developed is $g_m R \Delta V/2$.

So, equal in magnitude and opposite in direction between the 2 halves. Now it turns out that if you look at the common mode circuit you will see something analogous except it's slightly different you apply the same voltage to all components on either side of the line of symmetry, and you will find that all the voltages and currents are equal in magnitude and equal in direction. So, if there were a current developed because of ΔV , this current would be we need to figure out what this current is. So, let us say this current were some I_{d1} and let us say this current was I_{d2} . Now along on either side of the line of symmetry we know that the currents and voltages have to be equal in magnitude and direction. So, so for the common mode half circuit, I know that the magnitude has to be the same and same direction or sign.

What about the current source? In the common mode current source in the common mode picture of course, the current sources are again open circuit, and now if you write KCL at node x , clearly $i_{d1} + i_{d2}$ has to be equal to 0 which means and you know that i_{d1} is equal to $-i_{d2}$. So, therefore, i_{d1} has to be equal to $-i_{d2}$ which has to be equal to 0. Therefore, in the common mode half circuit in the common mode version of the

circuit there is no common mode currents that is generated for this particular circuit, and therefore, equal to 0.

Now, one thing to remember; one final thing to remember please note that as far as signal is concerned the V_{DD} node of course, is going to be a small signal ground. It may not be explicitly stated every time, but since it is a dc voltage it will be a small signal or incremental ground. So, now, one last point we need to make. So, this clearly means that the common mode gain of this circuit is 0, the final point we want to make is that because the differential mode half circuit is antisymmetric, and the common mode circuit is fully symmetric.

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DM \rightarrow anti-symmetric } Simplify analysis through
CM \rightarrow symmetric } "Half Circuit" Analysis

$\Delta V / 2$

ΔV

NPTEL

You can simplify analysis by using only one half of the circuit, and this is often called half circuit analysis. If I were to take one half of the differential mode circuit, that would look like this and once I calculate the currents and voltages for this half, all I have to do is invert the sign and I will have the currents and voltages in the second half of the circuit. Similarly for the common mode half circuit all I have to do is apply some delta V here, and I know what I can figure out what the currents and voltages are, and I use the same values for the other side too.

Now, this become very useful when your circuits get very complex, half circuit analysis very useful in many cases.

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$$CMRR = \left| \frac{A_{DM}}{A_{CM}} \right| = \infty \text{ for the previous circuit}$$

$$R_o = \text{Norton resistance of current source}$$

$$\Delta V_o = \frac{-g_m R}{1 + 2g_m R_o} \cdot \Delta V$$

$$\Delta i_d = \frac{g_m}{1 + 2g_m R_o} \cdot \Delta V$$

The slide includes a circuit diagram of a differential pair with a current source having a parallel resistance $2R_o$. It also shows a half-circuit model for common mode analysis with a current source I_o and a parallel resistance R_o .

Finally, we want to define a quantity called CMRR, this is the ratio of the differential mode gain to the common mode gain and this is the magnitude of that ratio for the circuit that we have seen this is infinity for the previous circuit. Now let us look at the common mode circuit again, but with the case where the current source is not an ideal current source. So, let us say that the current source had some resistance R in parallel with it, this is the incremental output resistance of the current source or rather the Norton resistance of the current source.

How do we handle this? So, clearly we need to find a line of symmetry, in the earlier case it was easy to find a line of symmetry because even though I have not explicitly shown it, I could split the current source into 2 halves which I had not shown explicitly. So, we will do that here for this circuit, because it is much more relevant for us. So, now, if I want to find the line of symmetry I now need to explicitly create this. So, I will take the current source and split it into 2 current sources of value I_o each which are in parallel, and in parallel with each I am going to have a resistance $2R$.

This circuit is exactly equivalent to the previous circuit and of course, now I still have a line of symmetry and along the line of symmetry for differential mode circuits, I will have a small signal ground for common mode analysis I will have I want will not have a small signal ground. So, if I do differential mode analysis for this circuit with a non ideal current source of course, I will still have a small signal ground here, and the analysis will

be exactly the same as before. But now what is different in this case is the common mode analysis. So, let us look at that.

So, for common mode analysis I am going to apply $\Delta V/2$ both sides. If I were to draw the small signal picture of this circuit, that would look like this. Now the current source of course, will be open, but I know have a resistance of value $2R_{naught}$. Now I am going to use only the left half of the circuit at the gate of the transistor I am applying ΔV . So, this is some ΔV_s and this is $g_m \text{ times } V_{gs}$ or $g_m \text{ times } \Delta V_{gs}$. Now if you analyze this circuit you will find that the small signal current Δi_d is equal to $g_m \text{ by } 1 \text{ plus } 2R_{naught}$ in to $g_m \text{ times } \Delta V$ flowing downwards.

Clearly if R_{naught} were infinity this current would be 0, and normally you expect R_{naught} to be very large because you have built and you have try to built an ideal current source. What is the output voltage ΔV now? ΔV_{naught} , ΔV_{naught} clearly is minus $g_m R \text{ by } 1 \text{ plus } 2g_m R_{naught} \text{ times } \Delta V$. So, this portion here is the common mode gain of the circuit. As you can see this of course, tends to as R_{naught} tends to infinity this goes back to the old value that we had written up earlier the common mode gain drops to 0, what is the CMRR of this circuit with a non ideal current source?

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$$\text{Here: CMRR} = \left| \frac{A_{DM}}{A_{CM}} \right| = (1 + 2g_m R_o)$$

For this circuit CMRR is $A_{DM} \text{ by } A_{CM}$. So, this works out to $1 \text{ plus } 2g_m R_{naught}$.

So, CMRR tells you the extent to which the amplifier preferentially amplifies the differential mode. What do I mean by that? Ideally you want an amplifier with a CMRR of infinity, because for the op amp you want and it to respond only to the difference between the 2 voltages, and not to the common mode value not to the average value and; that means, that the differential mode gain of the circuit should be as large as possible, and the common mode gain of the circuit should be as small as possible.

And therefore, this tells you for such a circuit you need it does not depend on the value of the resistance, and g_m changes the small signal gain. So, you there is an extent to which you cannot increase that further you need to have as large and R_{naught} as possible in other words the current source should be as ideal as possible.