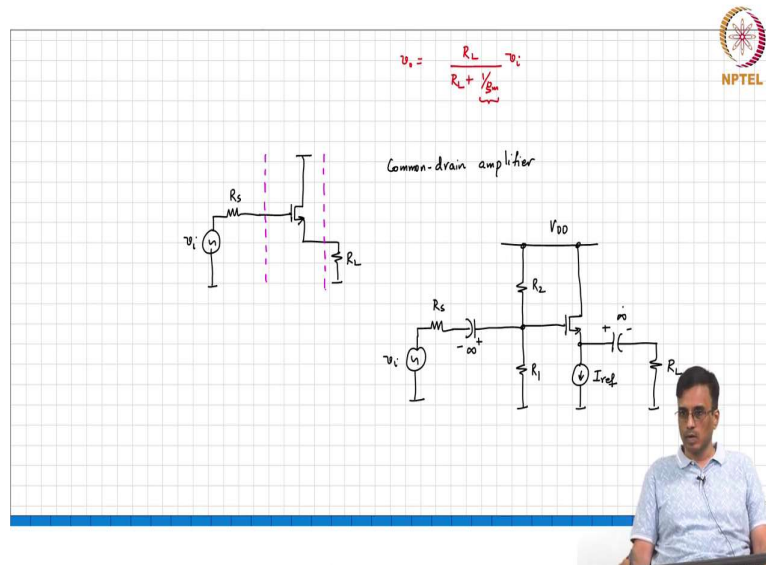


Analog Electronic Circuits
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Lecture - 26
Biassing of the Common-Drain Amplifier and Signal Swings

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Make sense, people? Alright, so this is now the incremental picture. Now, we need to make a real amplifier. So, what should we do?

Student: We should bias it.

We should bias it. We pick our way; you know, we can pick any one of the ways. So, what do you want to pick? Alright ok. So, you know, if you want to do the least amount of acrobatics after you bias the circuit, then there must be as much commonality between the

Student: Bias.

With the bias circuit as well as the, I mean, ideally, if you just simply replace all the voltage sources in the bias network with short circuits, if that leads to this picture, then there is nothing else to be done. So, even though it is possible to pick any of the biased arrangements and make it look like a common drain, What is it? What do you think? Which of the bias techniques that we discussed do you think will be, within your course, the easiest in this particular case?

Yeah, so basically, you know, you might recognise that we already talked about bias circuits where the drain was connected to V_{DD} , which basically means that in the incremental circuit, it is already.

Student: Ground.

Ground, right. So, if the drain is connected to V_{DD} , then we sense the current in the source, correct? Alright, and the feedback—I mean, evidently, we want the incremental voltage to come to the gate of the transistor. So, we do not want the bias to change the gate voltage. So, the only other choice is to sense, so the easiest bias circuit will therefore be one where you sense current in the source.

And let me remind you again: why are we doing this? If we sense current in the source, it means that the drain must be connected to a constant potential, right? So which in the incremental network will automatically be?

Student: Ground.

ground, which is what we want, alright? Now, we can sense at the source and receive feedback either at the gate or the?

Student: Source.

Source, which of them will be easier?

Student: Source.

Source, because the input needs to be coupled to the?

Student: Gate.

To the gate, alright. So, one way of doing it is, therefore, to do this. So, this is my ref, alright. So, this biases the transistor. So, this is V_{DD} , this is R_2 , and this is R_1 . They bias the transistor, alright? So, what do we need to do now? You know, make it look incrementally like the VCVS shown on the left. Yeah, we. I mean, you know, mentally now you should be able to look at the bias network and see the incremental picture, right? The source is, if you take that bias network and convert it into an incremental equivalent, the drain is grounded and the source is open, right? And we see that we are missing the input source as well as the?

Student: Output.

as well as the output load. So, how do we couple the input? Any suggestions? Well, the same old, same old. So, this is v_i , this is R_s , and they are the infinite capacitors. Does that make sense? And what do we do about the load?

Student: through capacitor.

Through a capacitor, R_L , alright, so this is your common drain amplifier, ok?

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$I_{ref} = 1\text{ mA}$
 $\mu_n C_{ox} \frac{W}{L} = 2\text{ mA/V}^2$
 $V_T = 1\text{ V}$
 $V_{DD} = 10\text{ V}$
 $R_1 = R_2 = 2\text{ M}$
 $R_s = 1\text{ k}\Omega$, $R_L = 10\text{ k}\Omega$
 $R_{out} = \frac{1}{g_m}$

$R_{in} = R_1 || R_L \gg R_s$

$Gain = \frac{g_m R_L}{1 + g_m R_L}$

And so, how do we figure out the swings? Oh, by the way, before we go to swings, what comment can you make about the input resistance now? The input resistance of the incremental signals is?

Student: R_1 .

R_1 parallel, R_2 which must be chosen. to be much larger than R_s , ok. So, even though the incremental part of the network, the ideal small signal model that we created had an infinite input resistance, that is the picture on the left, right. The moment you add this biasing circuitry, you can see that unfortunately.

The input resistance which was truly infinite has now become finite after all it is R_1 parallel R_2 ok. And what comment can you make about the output resistance that we have seen already, what is it?

Student: $1 / g_m$.

$1 / g_m$ and must be chosen to be much smaller than $1/R_L$. And what comment can you make about the gain? We have seen this again already; it is nothing but $g_m R_L / (1 + g_m R_L)$. Let us say that finishes the small signal part of the whole story.

Now, the next thing is to figure out the swing limits, okay? And to do that, well, the first thing to do is compute the operating point. So given R_1 and R_2 , we will be able to find the gate voltage V_G , and given the properties of the transistor and I_{ref} , we will be able to find the source potential, right? So, let us take an example. So, let us say I_{ref} is 1 milliampere, and $\mu_n C_{ox} W/L$ is 2 milliamps per volt square. V_T is 1 volt, and V_{DD} is 10 volts. And let us assume that R_1 is R_2 , which is say, 2 Meg, and R_S is 1 K, okay, and R_L is 10 K. Let us use this as an example to figure out what these swing limits are. So, first things first, what are we supposed to do?

Calculate the operating point; let us do that quickly. What is V_G ?

Student: 5 volts.

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NPTEL

Common-drain amplifier

$I_{ref} = 1 \text{ mA}$
 $\mu_n C_{ox} \frac{W}{L} = 2 \text{ mA/V}^2$
 $V_T = 1 \text{ V}$
 $V_{DD} = 10 \text{ V}$

$R_1 = R_2 = 2 \text{ M}$
 $R_S = 1 \text{ k}\Omega$, $R_L = 10 \text{ k}\Omega$

$V_{GS} = 2 \text{ V}$
 $g_m = \frac{2 \text{ mA}}{1 \text{ V}} = \frac{1}{0.5 \text{ k}\Omega}$

$g_m R_L = 20$

$A_{max1} \} \quad 5 + A_{max1} = 10 + V_T \Rightarrow A_{max1} = 6$

The diagram shows a common-drain amplifier circuit with an input signal v_i through a resistor R_S to the gate of an NMOS transistor. The gate is biased by a voltage divider R_1, R_2 connected to V_{DD} . The source is connected to ground through R_S and to a load R_L . The output v_o is taken from the source. The DC biasing is shown with $V_G = 5 \text{ V}$ and $V_S = 3 \text{ V}$. The reference current $I_{ref} = 1 \text{ mA}$ is shown flowing through the load R_L .

5 volts. What is the V_{GS} of the transistor?

Student: V_{GS} 2 volts.

Yeah, $V_{GS} - V_T$ is 1 volt. So, V_{GS} is 2 volts. So, what is the source potential, the quiescent potential? What is the quiescent potential of the source?

Student: 3 volts.

3 volts, ok. Is the transistor in saturation? Yeah, and that is because the drain potential is higher than the gate potential, which there is no risk of. What is it? Now let us start with the incremental voltage. What is the incremental voltage at the gate?

What is the input resistance?

Student: 1 $M\Omega$.

1 $M\Omega$ is that much larger than 1 $k\Omega$ or not?

Student: Yes.

Yes, so the incremental voltage at the gate is?

Student: v_i .

Approximately v_i , ok. What comment can you make about the incremental voltage at the source terminal? What is the g_m of the transistor, therefore?

Student: 2 milliwatt.

2 milliwatt.

Student: Ohms.

Ohms.

Yeah, so g_m is basically $\mu_n C_{ox} W/L$, which is basically 2 milliamps per volt squared times 1 volt.

Student: 1 volt.

Which is 2 milliamps per Volt.

2 milliamps per volt, which is $1 / (K/2)$, correct? So, is $g_m R_L$ being, what is g_m , the value of $g_m R_L$?

Yeah, so $g_m R_L$ is 20. So, what is the incremental voltage at the output at the source or at the load?

$v_i / 21$. So, this voltage at the source is going to be $+ v_i / 21$. So, when the input becomes very large, So, let us say the input is some $A \sin \omega t$. The question is: what is the largest input when the transistor goes up? In other words, in the positive half of the input cycle, what comment can we make about the transistor? Is it going towards, cutting off, or is it going towards the triode region?

Student: Triode region.

Triode region, why? The drain potential is fixed; the gate potential is going up. So, what is the maximum voltage, A_{max1} , that you can use before the transistor gets into the triode region? How will we figure that out? How will you figure that out?

Student: Equate triode boundary.

Yeah Triode boundary, what is that? The gate potential becomes one threshold above the?

Student: Drain.

Drain or the drain goes one threshold below the?

Student: Gate.

Gate. In this case, the drain is not going anywhere, so it is the gate that is going somewhere. So, the gate potential becomes one threshold above the drain. So, basically, the highest potential of the gate is, therefore, $5 + A_{max1}$, and that must be equal to?

Student: $10 + 0.2$.

10.

Student: $+ V_T$.

+ V_T , very good. That is 1 volt + V_T , which implies that A_{max1} is what? 6 volts, is that clear? Now, what about when the input goes negative, in other words, when you are in the negative half of the input cycle? What comment can you make about the transistor?

What is the incremental current to the transistor? Can somebody tell me?

What is the incremental current? I mean, stare at this picture. So, this is v_i ; this is v_o ; what is the incremental current to the drain of the transistor?

It is not $g_m v_i$.

Student: $g_m v_i / (1 + g_m R_L)$

Remember that the transistor current is the difference; it depends on the incremental gate source voltage; the gate is definitely at v_i , but the source is not at ground. So, basically, what comment can you make about the drain current? I mean the 2 ways of doing this, you know that v_o is nothing but $g_m R_L / (1 + g_m R_L) v_i$ and therefore, what comment can you make about $v_i - v_o$?

What is the current in the drain, incremental current in the drain therefore?

$g_m (v_i - v_o)$ that is nothing but $g_m / (1 + g_m R_L) v_i$, which can be written as this by R_L , which is seen to be nothing but v_o / R_L .

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Common-drain amplifier

$I_{ref} = 1\text{mA}$

$\mu_n C_{ox} \frac{W}{L} = 2\text{mA/V}^2$

$V_T = 1\text{V}$

$V_{DD} = 10\text{V}$

$R_1 = R_2 = 2\text{M}$

$R_S = 1\text{k}\Omega, R_L = 10\text{k}\Omega$

$V_{GS} = 2\text{V}$

$g_m = \frac{2\text{mA}}{\text{V}^2} \cdot 1\text{V} = \frac{1}{0.5}$

$g_m R_L = 20$

$A_{max1} = 5 + A_{max1} = 10 + V_T \Rightarrow A_{max1} = 6$

And then somebody will say, oh well this is obvious, why?

Yeah, well whatever current flows out here flows here, that is v_o / R_L must be coming from the?

Student: Drain.

Drain because the gate current is?

Student: 0.

0. Is that clear people? Ok, so, what is the incremental current in the transistor, you know as we in the in our example, what are the Quiescent current?

Student: 1 milliampere.

1 milliampere and the incremental current is plus?

Student: 2 / 21.

v_i , so $A \sin \omega t$ times 20 / 21 that is the output voltage that is divided by?

Student: R_L .

R_L which is 10 k. So, the $1 / k$ becomes a milliampere and this goes away. So, what is the smallest current that can flow through the transistor?

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$r_o = \frac{g_m R_L}{1 + g_m R_L}$
 $I_{ref} = 1 \text{ mA}$
 $\mu_n C_{ox} \frac{W}{L} = 2 \text{ mA/V}^2$
 $V_f = 1 \text{ V}$
 $V_{DD} = 10 \text{ V}$
 $R_1 = R_2 = 2 \text{ M}$
 $R_s = 1 \text{ k}\Omega, R_L = 10 \text{ k}\Omega$
 $V_{GS} = 2 \text{ V}$
 $g_m = \frac{2 \text{ mA}}{1 \text{ V}} = \frac{1}{0.5 \text{ k}\Omega}$
 $g_m R_L = 20$
 $A_{max1} = \min\{A_{max1}, A_{max2}\} = 6 \text{ V}$
 $5 + A_{max1} = 10 + V_f \Rightarrow A_{max1} = 6 \text{ V}$
 $A_{max2} = \left(1 - \frac{2 A_{max1}}{21}\right) \text{ mA} \Rightarrow A_{max2} = 10.5 \text{ V}$

So, what comment can you make about the current situation? In the positive half of the input cycle, is the current increasing or decreasing?

Student: Increasing.

The current is?

Student: Increasing.

Increasing in the negative half of the input cycle the current is?

Student: Decreasing.

Decreasing or going down. So, towards what region is the transistor heading?

Student: Cut off.

cut off, so the minimum current is therefore $1 - 2 \text{ A} / 21$ milliamperes. a max of 2 milliamperes right. Which means A_{max2} is what is the limit for cutoff?

Student: 10.5.

10.5 volts does it make sense. So, which is the largest amplitude you can put in before the transistor gets messed up?

Student: 6 volts.

6 volts, so A_{\max} is the minimum of $A_{\max 1}$ and $A_{\max 2}$, which is 6 volts alright. The next thing is, you know, the infinite capacitors. So, let us assume that we know all the resistors you know already. So, for this capacitance, C_1 is right, assuming that ω is the lowest frequency of interest. How will we choose C_1 ? The capacitive impedance should be less than or equal to the Thevenin resistance looking across the terminals of the capacitor and what is the Thevenin resistance looking across the terminals of the capacitor?

$R_s + (R_1 \text{ parallel } R_2)$, which is about $R_1 \text{ parallel } R_2$, is about R_s . So, it is roughly ω ohm. So, the impedance of the capacitor must be much smaller than $1/\omega$ ohm at the lowest frequency of operation, which if we assume to be ω , then $1/\omega C_1$ must be much smaller than $1/\omega$. What about the output capacitance? So, what is the output resistance?

Student: $1/g_m$.

$1/g_m$. So, one of the reactants of the capacitor that is coupling the load to the transistor must be the reactants at ω must be much smaller than $1/g_m + R_L$, and in any case, if you want a good common drain amplifier, then the R_L is going to be much larger than $1/g_m$. The output resistance is much smaller than the load; that is what it means. So, basically, it pretty much boils down to the fact that the reactants of the capacitance must be much smaller than the load resistor of 10 k. So, which do you think would be the larger capacitor on the input side or the output side?

Student: Output side.

The output side will need a much larger capacitor. Does it make sense, people? Alright. So, this basically completes the incremental voltage-controlled voltage source with a gain of?

Student: 1.

1 ok. So, if you want to try to make a voltage-controlled voltage source with a gain of, say, 5, Do you think it is possible? Why?

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$A_{max} = \min \{ A_{max1}, A_{max2} \}$
 $= 6V$

$A_{max1} \}$
 $A_{max2} \}$

$\sum R_L = 20$
 $5 + A_{max1} = 10 + V_T \Rightarrow A_{max1} = 6V$
 $(1 - \frac{2A_{max2}}{21}) uA \Rightarrow A_{max2} = 10.5V$

$\frac{v_o}{v_i} = 5$

The circuit diagram shows an input voltage v_i connected to a network of resistors. A dependent current source I_x is connected in parallel with a resistor R_1 . The output voltage v_o is taken across a load resistor R_L .

No here, of course. Yeah, I mean that we started off with, you know, our basic idea, which was that I was proportional to v . Now, if you want this gain to be if we want v_o to be if we want v_o to be say $5 v_i$. How would we do this? Let's say you had a variable current source like before. What will we do? What will we compare? We have to compare.

$v_o / 5$ to v_i so and then so therefore, you have a current pumping here. How will you generate $v_i / 5$ or $v_o / 5$?

So, basically some ratio of resistors R_1 and say $4 R_1$ and R_1 and then we have to compare which to?

Student: v_i .

Where will you put the voltmeter? We have to put the voltmeter here. Alright. Now, can you identify the transistor? Think about it; we will discuss it tomorrow.