Analog Electronic Circuits
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Lecture - 36
Finite Output Impedance Effects in Current Mirrors, the Cascode Current Mirror

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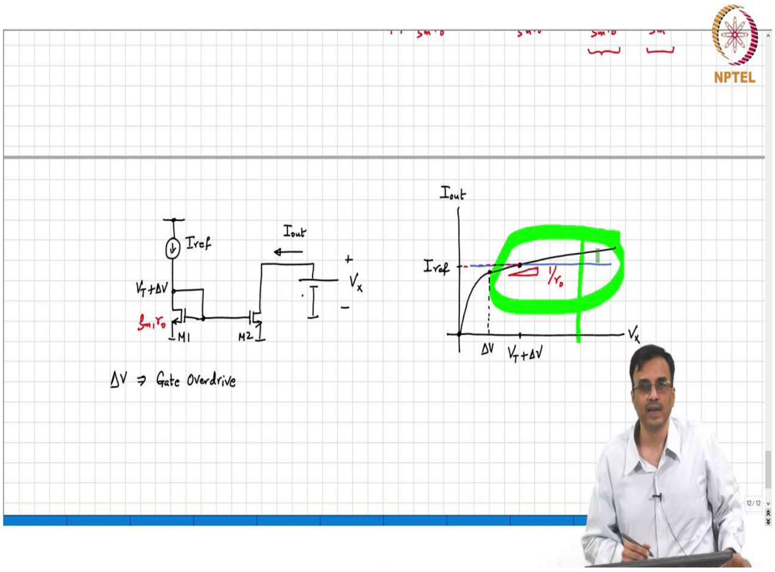

The next thing that I would like to do is, you know, spend a little time again talking about current mirrors because these are very important in practice. So, this is the plain old current mirror, this is M1, this is M2, this is I_{ref} and let us assume that the overdrive of the transistors is ΔV right otherwise, we need to keep carrying this V_{GS}-V_T all over the place.

So, what is the potential of the drain of M1? We did this before please. What is it? Yes, there's a backbench. I understand man, look at it. Do you see something written in the text below?

Student: Yes.

What is it, what is it I say? Yeah, now in terms of known quantities in terms of these quantities can you please tell me what the drain potential of M1 is? By the way, what do you understand about gate overdrive voltage? If I denote the gate overdrive voltage by ΔV, what is the gate potential?

Student: ΔV+ V_T.

$\Delta V+V_T$ is this clear? Alright. So, now, this is the plain old current mirror and we saw this already. So, if I vary V_x and if I plot I_{out} as a function of V_x, how does it look like? For what value of V_x will I_{out} be exactly equal to I_{Ref}? It is going to be exactly V_x identical to I_{ref} if the V_x is exactly equal to $V_T+\Delta v$ so, that point we are going to mark there. Now what is the slope now of this of this characteristic I_{out} versus V_x. If I plot I_{out} versus V_x how will the picture look like? How will it look like? For Vx = 0 what is I_{out}?

Student: 0.

So, what happens as we keep increasing Vx? It will do this and at a certain point it will then do that right. Now let me exaggerate a little bit to show the slope and what is this knee point there? What is the knee point? The point beyond which it sort of attempts to become flat.

Student: Δv.

Δv is this clear? Alright. What is the slope now and what is the slope there? Let us assume that the output resistance is the gm of the transistor is something and r_o is something else. So, what is the slope of that? It is $1/R_o$. So, ideally, we wanted it to be a constant current which is exactly equal to.

Student: I_{ref}.

I_{ref} and we wanted to be exactly equal to I_{ref} for all values of V_x, but unfortunately that is not possible. When V_x becomes sufficiently small the transistor will go into the linear region, the current has to drop right, but beyond a minimum voltage we would like that to behave like an ideal.

Student: Current source.

Current source, correct. So, we see two problems. One is that in this region there is a.

Student: Slope.

There is a slope. So, unless V_x is exactly chosen to be equal to $V_T+\Delta V$, there is not only a slope, but there is also an error in the current that you get out, right.

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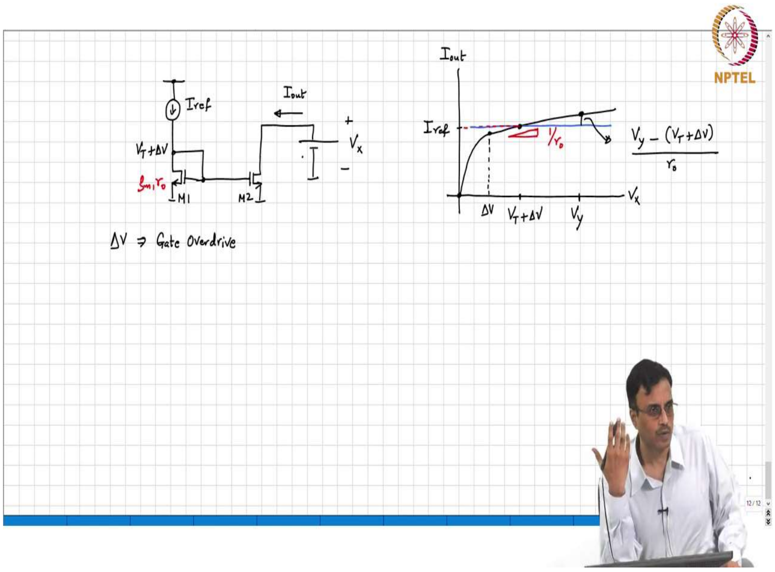

So, for example, if you put a voltage say V_y which is greater than $V_T+\Delta V$ what common can you make about this current here? It is, of course, greater than I_{ref} how much is it greater than I_{ref} by $V_y – (Vt+\Delta V) /r_o$.

So, the change in the drain voltage divided by the output resistance will give you the change in the current alright. Now the question is can we do something to take this bad current source right and make it make it better correct. So, we have already seen how to take a bad I mean when we say bad current source and make it better what does it mean what resistance?

Student: parallel resistance.

Yeah. So, basically, we want to increase the output resistance of that current source.

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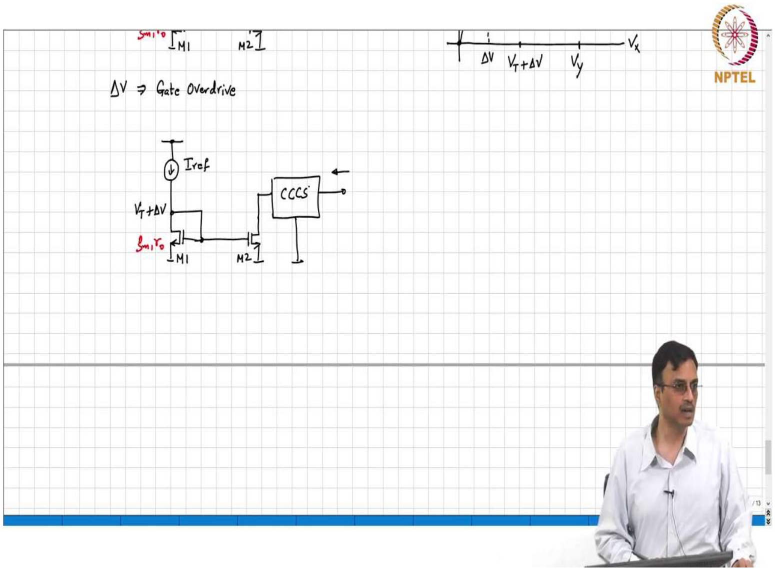

So, the question therefore, is what do we do? So, the question is if we put a box here alright what should we do to make this output resistance?

Student: High.

So, what must be there in this box? What kind of thing must be in that box?

Student: Current controlled current source.

What is the simplest current controlled current source that you know?

Student: Common gate amplifier.

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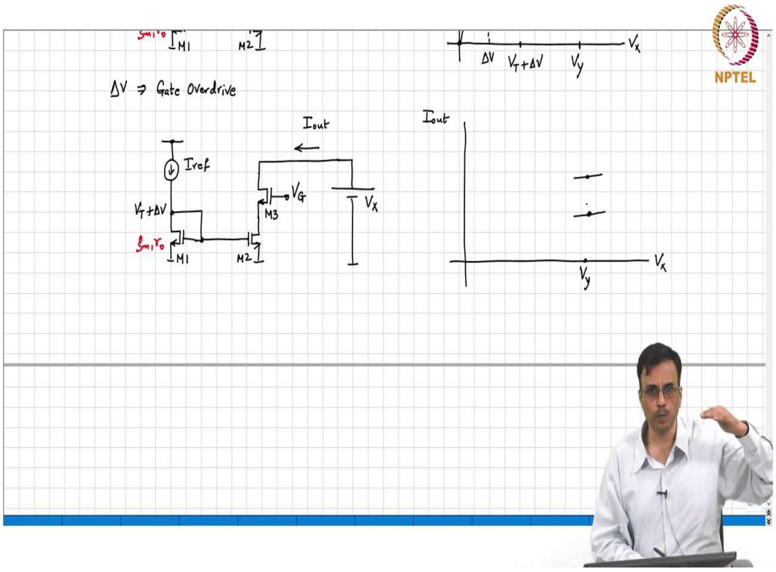

So, basically that is the common gate amplifier and if the common gate amplifier has to work properly the transistor M3 must operate in which region? When will the common gate work like a current controlled current source? When does the transistor operate?

Student: Saturation.

Saturation alright. So, that basically means that this gate voltage V_G must be sufficiently large that M3 operates in?

Student: Saturation.

Saturation, does it make sense? We will figure out what that V_G is a little later, but let us now plot. So, what comment can you make about the output resistance of this is V_x again? This is I_{out} this is I_{out}. So, when V_x is 0 what is the current?

It is still 0 al. So, now what comment can we make about the for a given voltage V_y where all the transistors are operating in saturation. What comment can we make about the slope of the characteristic if I plot I_{out} versus V_x you will get another curve like the previous one right. The question I am asking is what is the slope of that characteristic? The two parts one is a slope one is the actual value at V_y the two different things.

So, both of these have the same slope, but have different output currents when you put in some V_y. So, the first thing that I am going to ask you is what is the slope?

Student: (Refer Time: 10:27).

To find the slope what do we do? What are we exactly looking for when we want to find the slope of that characteristic r_{out}?

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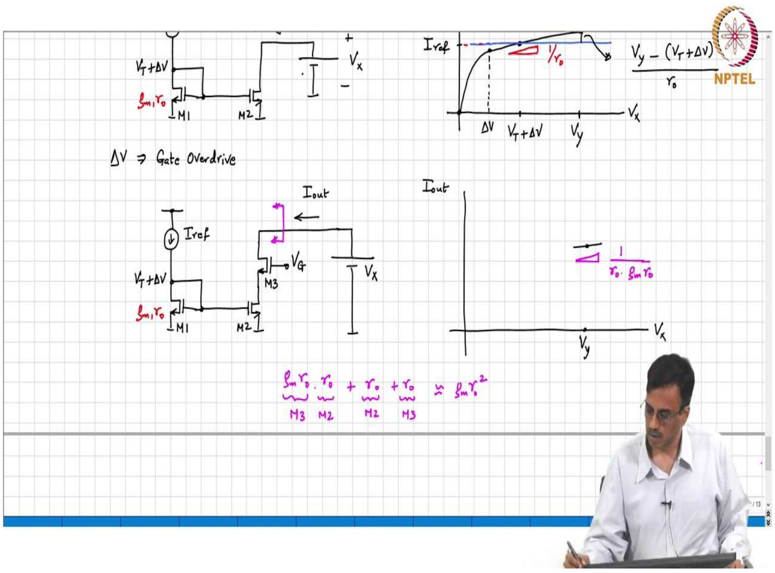

So, basically, we are interested in finding the output resistance there right and we have already seen this until it is blue in the face. So, what is the output resistance? What is the output resistance looking in you know at the point I have drawn in magenta. What is the output resistance? What is the resistance looking down from the source of M3?

Student: r_o.

r_o. So, what is the output resistance looking in now at the drain of M3?

Student: r_{out}.

Very good. So, basically please go back and look into your notes right.

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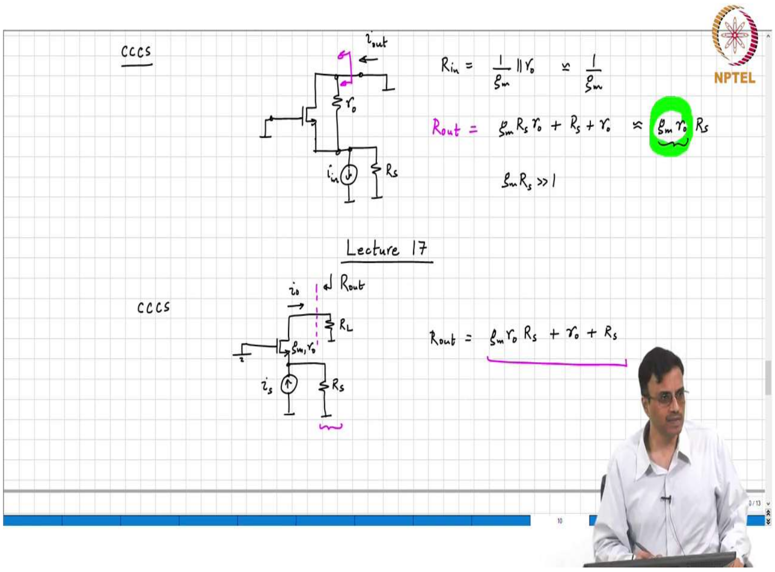

We saw the R_{out} and we discussed this already this morning. The output resistance is nothing, but g_m R_o R_S + r_o + R_S. So, basically the output resistance looking in will therefore, be g_m r_o this this g_m r_o is corresponding to which transistor?

Student: M3.

M3. r_o corresponds to which transistor?

Student: M2.

r_o one corresponds to M2 and one corresponds to M3 and we know that g_m r_o is very large. So, this is all approximately equal to?

Student: g_m r_o^2.

So, the slope of this line therefore, is now 1/ g_m r_o^2

So, when compared to the plane current mirror what comment can we make about the slope?

Slope has reduced by a factor $g_m r_o$.

R r_o and since g_m R_o is maybe I do not know 30 25 30 40 something like that. Basically we see that the output resistance of the current source is increased by an order of magnitude, but another thing we not only want the output resistance to be?

Very high we also want the current to be an accurate mirror correct. So, the question now is what comment can we make about the output resistance if the output voltage is I mean this voltage is V_y we can see that the slope is now much smaller, right. So, for all practical purposes you can therefore say that this line is almost flat when compared to the previous line. So, this is pretty much flat. So, now, the question is what I mean two questions that arise.

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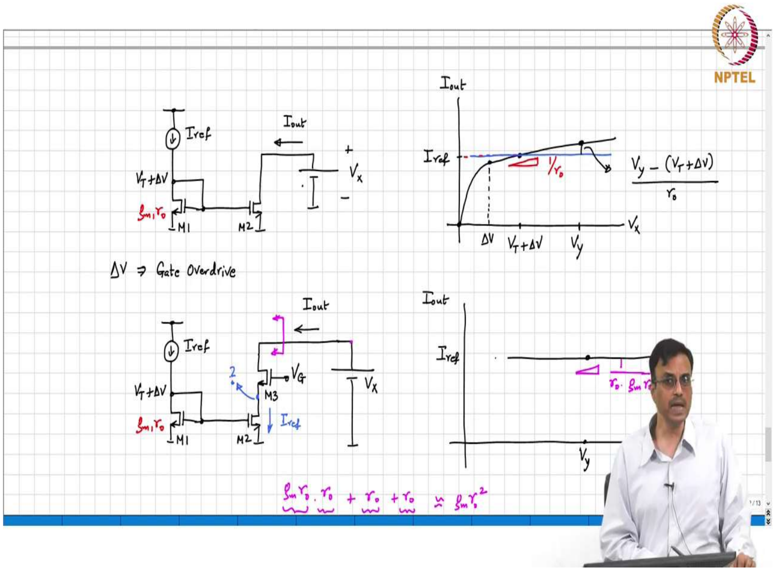

The first is what are the two questions that arise: we know the slope of that line, what else do we need to know about that line? The actual current that is flowing. So, can we get a quick estimate of what the actual current that is flowing is or let me know or let me make this easier what V_G must I use so that the current at the output is exactly equal to I_{ref}. What comment can we make about the current of M2 versus that of M3?

Student: Same.

And that is the same as the output current. Now if we want the current in M2 to be exactly identical to I_{ref} what comment can we make about this potential? If the current in M2 has to be?

Student: Same.

Exactly identical to the current in M2 has to be exactly identical to I_{ref}, what comment can we make about the drain potential of M3? It should be V_T+ΔV.

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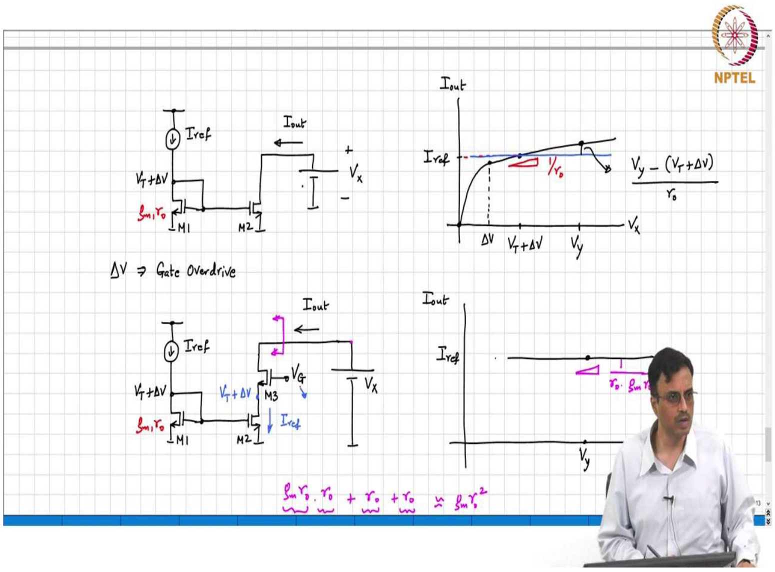

So, this is V_T+ΔV. So, what comment can you make about V_G? What M3 is identical to M2? So, what comment can you make about its gate source voltage? M3 is identical to M2; M3 operates in saturation M2 operates in saturation the gate source voltage of M2 is V_T+ΔV. What comment can we make about the gate source voltage of M3?

Which is V_T+Δv the gate source voltage of M3 and M2 will be.

Student: Same.

You know approximately the same because their drain source voltages need not be need not be the same, but to first order they are approximately the same. So, what comment can we make about V_G therefore, If we want I_{out} to be exactly equal to?

Student: I_{ref}.

I_{ref}. V_G must be 2 V_T +2 Δv alright.

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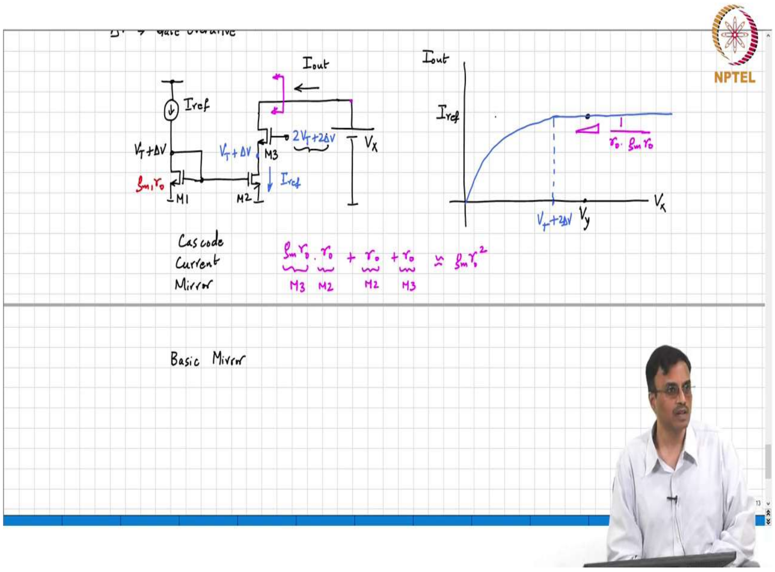

Now what is the minimum voltage that is needed to remember all this nice stuff only works when all the transistors are in?

Student: Saturation.

Saturation. So, what is the minimum V_X needed to make sure that all the transistors operate in saturation? So, basically remember that if you have an NMOS transistor the transistor will be in saturation; the edge of the triode region is defined by when the drain goes one threshold below the gate. So, basically now we have the gate potential is 2 V_T+2 ΔV so the minimum voltage therefore, needed will be?

Student: V_T+2 Δv.

So, after this we have a constant current right, but below this it will do something like this. So, what is the moral of the story? When you compare these two current sources what do we see? So, we can compare the two current sources you know with three parameters right: what are the three points of interest?

Student: Slope.

The slope.

Student: The accuracy.

The accuracy.

Student: Minimum voltage.

And the minimum voltage that you need to be across the current source for it to behave like one. So, basic mirror and this mirror which is where you take a basic mirror and current mirror. Where you basically put a common gate amplifier you know a top M2. This is what is called a cascoded current mirror. Now, of course, the way it is. So, now that we want 2 V_T+2 ΔV I mean can somebody suggest a simple way of generating 2 V_T+2 ΔV. Is a gate source voltage when a transistor has a current that is connected and you pump in I_{ref} through it now I want. So, I have a 1-volt battery. I want to get a 2-volt battery. What should I do? If I had you know an amplifier with which could amplify 1 volt and give you 2 volts its supply voltage must be.

Student: Same.

So, one easy way of doing it is to say basically you know if I want 3 volts I have a 1.5-volt battery I will put 2 in series. Now based on this discussion can you tell me I have V_T+ΔV I want 2 V_T+ 2 Δv.

So, what do you think I can do? You can put it in series. Ok. So, where am I going to put the 2 transistors in series?

Student: On the right side of M3.

On the right side of M3. Well good let us see. So, the suggestion is the following: let us see where this leads us.

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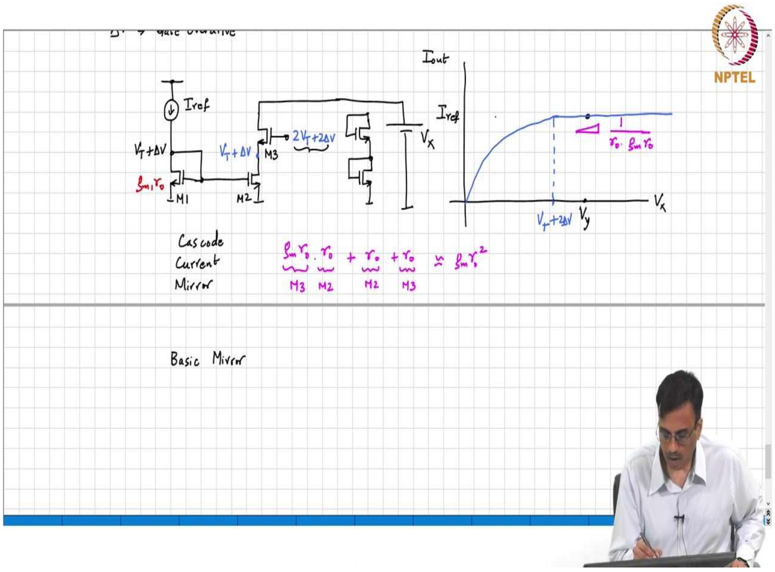

So, we need 2 V_T+2 ΔV. So, the suggestion is two transistors in series and what should I do to the drains and gate of those two transistors? This is M1. This is a transistor then connected to that gate to the gate of M1. M1 is already connected. Add the same mirror?

Student: M1 between I_{ref} and M1 same M1 and gate source.

Both gates mean which one.

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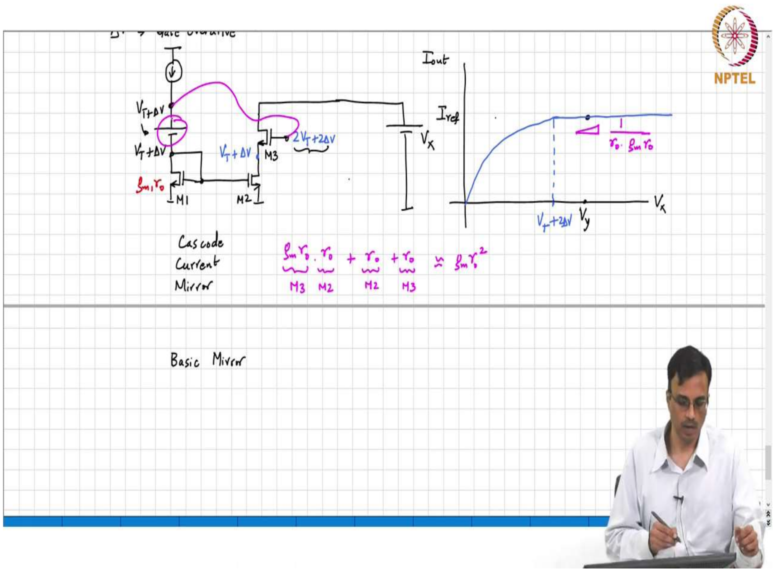

So, basically the idea is the following: we need V_T+2 ΔV there. So, we have V_T+ΔV. So, in principle what will we do? If we had a battery which was VT+ΔV what would we do now?

Student: Connect these.

What is this potential?

Student: 2 V_T+2 Δv.

So, what should we do now?

Student: To connect that point to the gate of M3.

So, can you correct which is equivalent and how do I now realize this battery?

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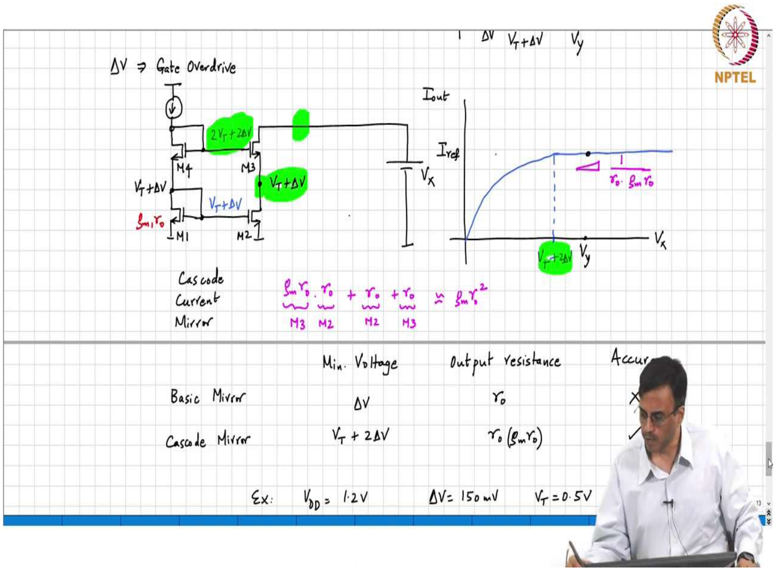

Student: copy M1.

Copy M1 and paste it and I just turn M3 around. So, this is basically 2 V_T+2 ΔV, this is V_T+ ΔV. So, let us. So, this is the cascode mirror. So, the minimum voltage needed output resistance and accuracy. Alright. So, the basic mirror accuracy is not great alright and what is the output resistance? Ok alright what is the minimum voltage?

Now complete the second row.

Student: 2 ΔV+V_T.

Look at the picture again and open your eyes.

Output resistance? It is R_O g_m r_o and is much better provided and that is because the gate remembers that this accuracy will only show up when the gate of M3 is biased properly at 2 V_T + 2 Δv. So, when we move to the basic mirror and the cascode mirror you know what is it that we gain and what is it that we lose?

Student: The accuracy.

The accuracy is improved.

Student: The output resistance is improved.

The output resistance is improved. But the minimum voltage has gone up right. So, for example, let us say V_{DD} is 1.2 volts which is a very common supply to use these days. Let us say ΔV is 150 millivolts and V_T is half a volt right. So, the minimum voltage for the basic mirror is what?

Student: 150.

150 millivolts whereas, for the basic cascode mirror what do we see? V_T+2 ΔV which is basically 800 millivolts. So, you can see that a big fraction of the power supply voltage is lost. So, you can have that current source only operate from 800 millivolts to 1.2 volts only 0.4 volts of head room is left for that current source. So, ideally what would you like to do?

So, what is the problem with the basic mirror? That cascode mirror solved output resistance was very low and the change. But then what is the problem? We fixed those two problems, but now we have inherited a new problem. A new problem is that the minimum voltage needed is?

Student: Higher.

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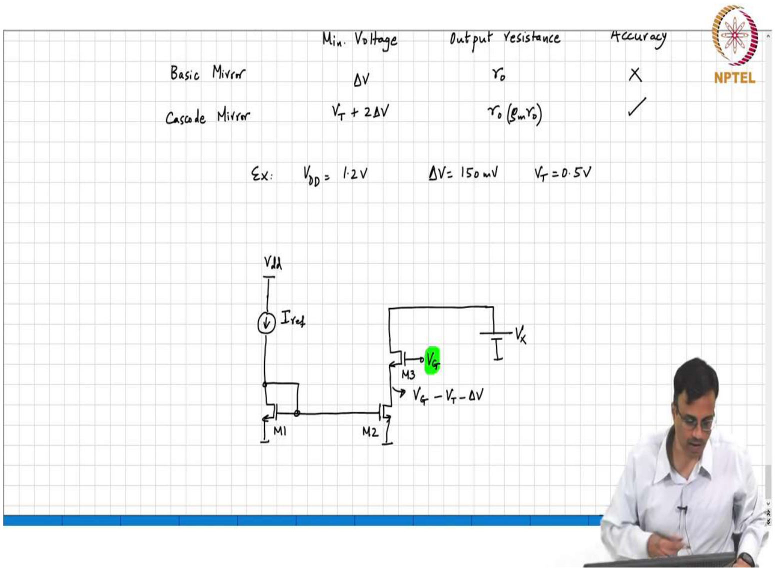

So, what do you think we can do? So, let us now try to see if we can solve the minimum voltage problem. Alright. So, the reason why we had the minimum voltage problem was that both the transistors have to be in?

Student: Saturation.

Now let us see of course, now this ensures that both the transistors are in saturation, but what is the potential at the drain of M2? What is the potential at the drain of M2?

Student: V_T+Δv.

So, is this it is of course, M2 is definitely in saturation, but is it deep in saturation or is it just at the edge of saturation? What do you understand by deep in saturation? So, in other words how much extra headroom does M2 have right with respect to the edge of the saturation region? If M2 had to be, I mean the drain source voltage needed for M2 to be in saturation is just.

Student: Δv.

Δv, but what is the V_{DS} is it actually has? It has V_T + ΔV. So, that V_T is simply you know extra voltage right which serves no purpose as far as.

Student: Saturation.

Which serves no purpose as far as the saturation region is concerned, but because the drain of M2 had to be at V_T+ΔV the gate of M3 has to be at 2 V_T +2 ΔV and consequently the minimum V_x needed becomes V_T + 2 Δv. I mean the reason why the minimum voltage is this large value of V_T+2 ΔV is that the drain voltage of M2 is too high the therefore, the gate voltage of M3 has to be V_T+ΔV higher than that which then basically means that V_x has to be a minimum voltage of V_T+2 ΔV. So, if we want the minimum voltage to drop, what comment can we make? How do we do this?

Now, think with common sense. Why is the root cause? Why is the minimum voltage at the drain of M3 so, high? Because, the gate of M3 is very high. Why is the gate of M3 very high? Because the drain of M2 is very high. So, now, if you want to reduce the minimum voltage what comment can you make about V_G? Should we increase it or should we reduce it?

Student: Reduce it.

You should reduce it right. So, what is the lowest V_G we can use before M2 goes into the triode region or when M2 is adjusted to the edge of saturation now what is this potential? If the gate voltage of M3 is V_G what comment can we make about its source potential? V_G at the gate is known as M3. Let us say it is $V_{G.}$ I am asking you what the drain potential of M2 is simply V_G -the gate source voltage of M3 and what is the gate source voltage of M3? It is-V_T -Δv.

So if you want to ensure that M2 is in saturation what comment can we make? Ok we will stop here I think I am already overshoot we will continue tomorrow.