

Microelectronics: Devices to CiRCuits
Lecture- 51
Op-amp as an Integrator and Differentiator
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Hello and welcome again to the NPTEL Online certification Course on Microelectronics: Devices to CiRCuits. This module will be devoted to an application of an operational amplifier which is primarily an integrator and differentiator. In our previous lecture, we had seen that an operational amplifier is a difference amplifier which actually finds the difference between the 2 voltages applied to 2 nodes, inverting and noninverting node of an op-amp, multiplies that with the gain of the operational amplifier and put it in the output side. This is known as an open-loop gain. So, there is no loop, or is no feedback loop available to me and therefore I typically have my output voltage almost equals to A times V_2 minus V_1 , right.

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The image shows handwritten notes on a whiteboard. At the top, it states: ① $V_0 = A(V_2 - V_1)$ with arrows pointing to 'inverting' and 'non-inverting'. Below this, it lists: ② $Z_{in} \uparrow \infty$ High; $Z_{out} = 0$ Low. ③ Inverting \rightarrow $\left(-\frac{R_2}{R_1} \right)$ with a circuit diagram of an inverting op-amp showing input V_1 , feedback resistor R_2 , and input resistor R_1 . ④ Non-Inverting $\left(1 + \frac{R_F}{R_1} \right)$. The bottom of the slide features the IIT Roorkee and NPTEL Online Certification Course logos, and a page number '2'.

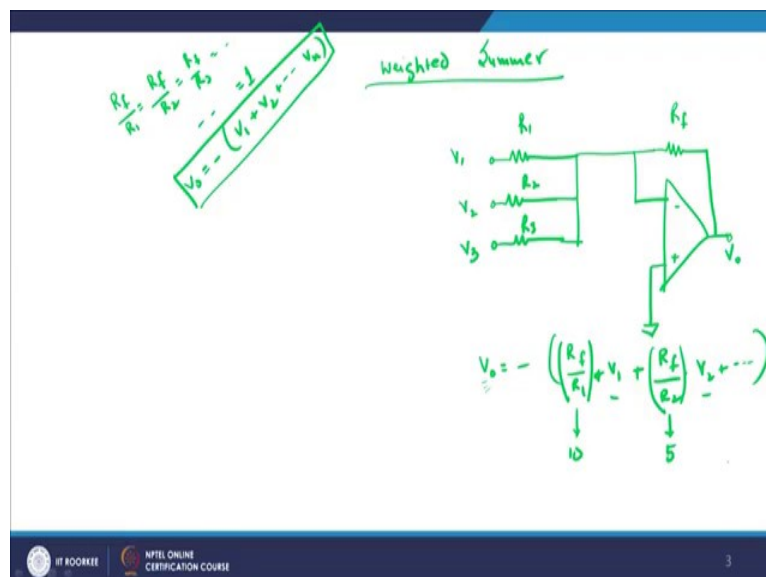
So, in our previous discussions we have seen that the output voltage V_0 right, output voltage V_0 is given as A times V_2 minus V_1 , where V_1 is fed into the inverting terminal inverting terminal and V_2 is fed into a noninverting terminal, inverting terminal right. We also, So, this is the first property, the second property was that input impedance of an operational amplifier ideally is very high. Ideally it should be infinity but really it is very high and my output impedance is ideally equals to zero but in reality it is very low. So, I have got low output impedance and high input impedance.

This is the second important property of the operational amplifier which you saw in the previous discussion. We also saw that I can have an inverter or I can have an operational amplifier which can act as an inverting amplifier, right and we saw that the inverting amplifier can work with the gain of R_2 by R_1 . Which is R_2 is the feedback resistance and R_1 is the input resistance. So, the operational amplifier looks something like this and you had R_f here and you had R_1 here.

Now This was referred to as the closed loop, so this is basically your closed loop gain, closed loop gain, right. I have a closed-loop gain in which I have inverting mode, because it is minus sign. So, it is basically a phase change between input and output by 180 degree and it is minus sign showing it is a phase change and it is a ratio between 2 registers R_2 and R_1 , right. And therefore, this is the inverting. We also studied, I think noninverting consideration non inverting in which we studied that it is basically $1 + R_f$ by R_1 and therefore this was the basically the gain which you which you got in the case of a noninverting case.

Now, we will take care of this one and we will go ahead and see what are the implications of having for example, a noninverting. So, can we have operational amplifier work as a voltage summer. So, if I want to sum n number of analog voltages, what is the best form of doing it and one of the best form is actually using operational amplifier as a summer.

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So, let us just show to you what is known as a weighted summer So, it will be a summing of 3 or 4 analog voltages and it looks something like this. That is your R_1 here, right, and you have got R_2 and your R_3 , all these 3, if you feed here then you get to negative side and then

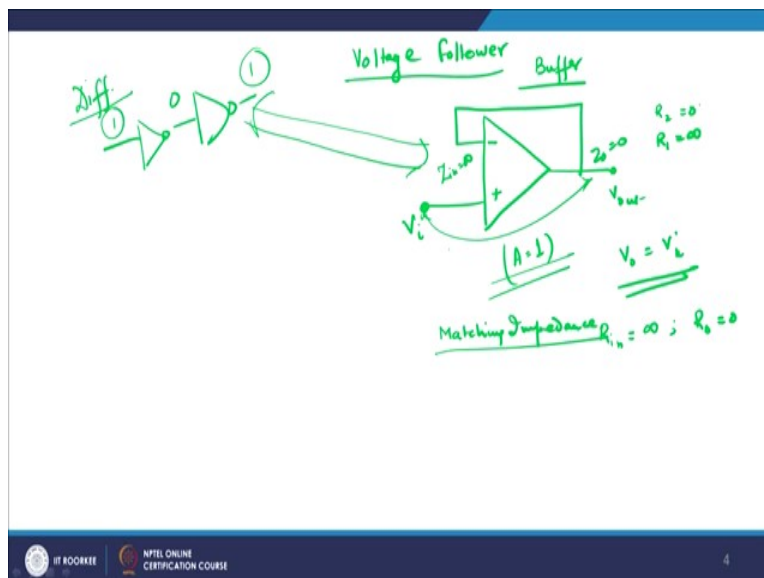
this becomes equals to R_f . This is your R_f , this you ground and this is V_1, V_2, V_3 and you got R_1, R_2, R_3 .

With this knowledge, since this is in inverting mode, I get V_0 to be equals to minus R_f by R_1 plus into V_1 right, plus R_f by R_2 into V_2 plus so on and so forth, which means that the output voltage which is available at this point, right, is basically a sum of input voltage but weight weighted with respect to R_f by R_1, R_f by R_2, R_f by R_3 and so on and so forth. Which, an interesting thing therefore is that if you want to just sum the voltages, you just have to keep R_f by R_1 equals to R_f by R_2 equals to R_f by R_3 so on and so forth, all equals to 1.

If you sustain that I get V_0 equals to minus of V_1 plus V_2 so on and so forth till V_n . So, this is the simple summing of voltages across the board, right. This is a very straight forward way of looking at it. Another methodology or another interesting part of it is that, that is if you want to have this, suppose you want that the output voltage of voltage V_1 should be ten times.

So just keep R_f by R_1 10, you keep this one whatever you want to keep it, 5 and so on and so forth, then voltage V_1 will have a larger influence on the output voltage because you are applying principle of superposition here and all the voltage will be additive in nature. And therefore, you automatically get output voltage which is sum of all the voltages here. This is known as a weighted summer. So, you can you can sum analog voltages in this manner, right. So, if n number of analog voltages you can sum all the voltages in this manner.

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Now, let me come to another one and that is basically a very simple one, that is known as a Voltage follower network and if you look very simplistically it is something like this, that you have got an Op-amp and this is given here, this is applying voltage V_i and what I do is I simply short my input and output. So, the noninverting mode is shorted with respect to output V_{out} .

Under such a scenario, my R_2 obviously is zero and R_1 if you see is infinity because it is input impedance of the operational amplifier as infinity. This is basically, so so what I am trying to tell you is since R_2 equals to zero the closed loop gain A equals to 1. So therefore, this type of configuration gives you a voltage gain of approximate equals to 1. However, in this V_{out} therefore follows V_i , because gain equals to 1, you are not doing any change in the gain therefore V_o equals to V_i and therefore your R_{in} is equals to infinity and we have discussed this point and R_o equals to zero.

R_{in} equals to infinity means input impedance is relatively high or very high, which again means that no current will be flowing through the operational amplifier, only a large change in the voltage will be visible to you. But that will not entertain any current whereas since R_o equals to zero ideally, it primarily means that I can have any current flowing through this but the voltage at output point will be relatively small in dimensions. So, this is a voltage follower.

So, when do you use a voltage follower? Because its gain is 1 and therefore you generally do not use it for high gain applications. But, you use it for, you use it as a buffer circuit, right. So, it is basically sort of an analog buffer which you see. If you remember we had studied digital buffer in our other modules. When we go for digital buffers, we use for example, a static inverter series. So, it is 1 zero 1.

So, whatever input you are giving here, output is also 1. So, so and you remember in a CMOS inverter, static inverter, your input Z_{in} is very high and Z_{out} is very low. And exactly the same thing happens in an Op-amp that here Z_{in} is infinitely large as I discussed with you. And Z_{out} here is very very low. It is almost analog. So CMOS inverter is analogs to a voltage follower in a sense.

And you can use this voltage follower for all your other issues for example, used for the purpose of, for matching the impedances. So, primarily voltage followers are used for matching impedances. And for transfer, so what it implies is that it allows you to transfer

large amount of power from V_{in} to V_{out} , right. Because your impedances are perfectly matched and you have a large power pin transferred from input to output. So, this was important aims of a differential amplifier.

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Difference Amp

$$V_{id} = V_2 - V_1$$

$$V_o = A_d V_{id} + A_{cm} V_{cm}$$

$$\infty \uparrow \text{CMRR} = 20 \log \left| \frac{A_d}{A_{cm}} \right|$$

$$\underline{A_d \gg A_{cm}}$$

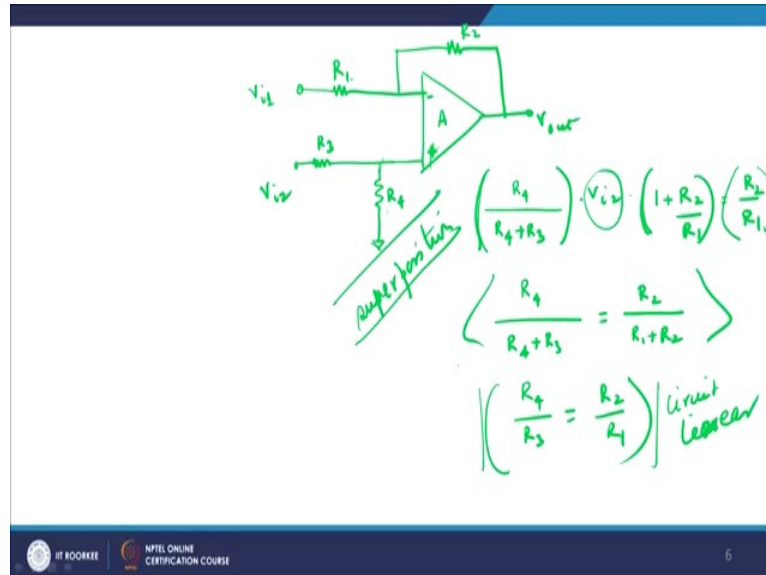
We come to the last part here and the last part of the circuit configuration and that is known as Difference Amplifier. Difference Amplifier, right. What does difference amplifier do? That if you I can write an expression, that output voltage is equals to A_d right into V_{id} plus A_{cm} into V_{cm} . I will explain to you what do I mean by these terms. Well, V_{id} is nothing but the difference of V_2 minus V_1 . This is V_{id} , right. So that if you multiply with A_d , A_d is the differential gain.

Differential gain means that part of the gain which actually tries to amplify the differential signals across the 2 terminals of the operational amplifier. The next part is A_{cm} into V_{cm} , where A_{cm} is basically the voltage gain, right, for the common mode signal. Common mode signals are those signals which are common to both the inputs of your operational amplifier. Now, typically we define, as I discussed with you earlier also, CMRR is equals to 20 log of A_d by A_{cm} , right. Mode value of that, right. That is how you define your CMRR.

And the CMRR ideally is infinitely high or very high, very large value, which primarily means that A_d has to be much much larger as compared to A_{cm} . And makes sense also, because see the differential gain if it is large, then any differential input will be amplified by the operational amplifier. Whereas, any common mode input will be suppressed by the

operational amplifier. And therefore, any Op-amp is a very good selector or a rejecter of noise, right.

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Now, let me come and show to you what is a how does a difference amplifier looks like or what is the configuration of difference amplifier. So, I have got a negative terminal here and this is my noninverting terminal and this is my R_3 , right. So, I have a voltage divided network at this particular point and this is V_{i2} and there I got a V_{i1} and we have got R_1 here, right, and then exactly the same as an inverting terminal R_2 and this is R_1 and this is V_{out} , right.

So, so if you if you if you see here, this is R_1 , R_2 and this is R_3 and R_4 and this is operational amplifier with voltage gain of A . So, I can write down in this case, I can write down R_4 upon R_4 plus R_3 , right. Why R_4 upon R_4 plus R_3 ? Because, if you see very carefully between these 2 points, these 2 are in series and so it is R_4 plus R_3 is the total resistance and the voltage across R_4 appears into the noninverting terminal of A and therefore R_4 upon R_4 plus R_3 into V_{i2} is the voltage at this particular point, right, multiplied by multiplied by 1 plus R_2 by R_1 right, and this this must be equals to R_2 by R_1 .

Why it should be equals to R_2 by R_1 ? Because, you see primarily if I assume that R_4 upon, because you are taking the voltage across R_4 and feeding it into the noninverting terminal of the amplifier. It primarily means that out of some value of voltage V_{i2} only R_4 upon R_4 plus R_3 is available to you at A , right. Similarly, why do you multiply that with 1 plus R_2 by R_1 ? Because, that is nothing but the gain of this stage. So, I multiply these two together and I get

R_2 by R_1 coming into picture here, must be equal to R_2 by R_1 which is the closed loop gain of this system.

So, what I get is that R_4 upon R_4 plus R_3 must be equals to R_2 upon R_1 plus R_2 . You can solve it and get it for all possible reason. Now, this 2 will be equal provided I make R_4 by R_3 equals to R_2 by R_1 , right. R_4 by R_3 is equals to R_2 by R_1 . Once you sustain these 2 inequalities, then the circuit is linear and you automatically get, so this will imply that the circuit is linear and as a result you can apply principle of superposition, right. So, you can apply principle of superposition.

Now, please understand this is the ratio of the registers, right. so it is basically R_4 by R_3 and R_2 by R_1 , which basically means that if this is true, your Op-amp is balanced and your circuit is considered to be linear for all practical reasons. now with this knowledge, let me show to you that what will be the value of a differential gain.

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Handwritten mathematical derivation for the differential gain of an op-amp circuit. The diagram shows an op-amp with feedback resistors R_1 , R_2 , R_3 , and R_4 . The derivation shows the calculation of V_{o1} and V_{o2} using superposition, leading to the final differential gain equation $V_o = \frac{R_2}{R_1} \cdot V_{id}$.

$A_{id} = V_{o2} - V_{o1}$
 $\frac{V_o}{V_{id}} = \frac{R_2}{R_1}$
 $A_{id} = \frac{R_2}{R_1}$
 Next $V_{i1} = 0$
 $V_{o1} = -\frac{R_2}{R_1} \cdot V_{i1}$ $V_{i2} = 0$
 $V_{o2} = V_{22} \left(\frac{R_4}{R_3 + R_4} \right) \left(1 + \frac{R_2}{R_1} \right)$
 $= \frac{R_2}{R_1} \cdot V_{i2}$
 $V_o = \frac{R_2}{R_1} (V_{i2} - V_{i1}) = \frac{R_2}{R_1} \cdot V_{id}$
 $V_o = \frac{R_2}{R_1} \cdot V_{id}$

So, V_{o1} equals to minus R_2 by R_1 into V_{i1} , right, because V_{o1} is the output voltage because of input voltage. Assuming that V_{i2} equals to zero. So, V_{i2} equals to zero that is how you do how do you apply principle of superposition, right. How do you do that? You take If there are n number of signals you take one signal and try to give an input, all other signals are made zero. Similarly, now you take the second signal first and all the other signals are made to zero and then output you go on calculating for each of the signals.

Once the output is available to you, you simply have to add those outputs and for those outputs you will get the input, for these inputs you will get those outputs. Which means that if

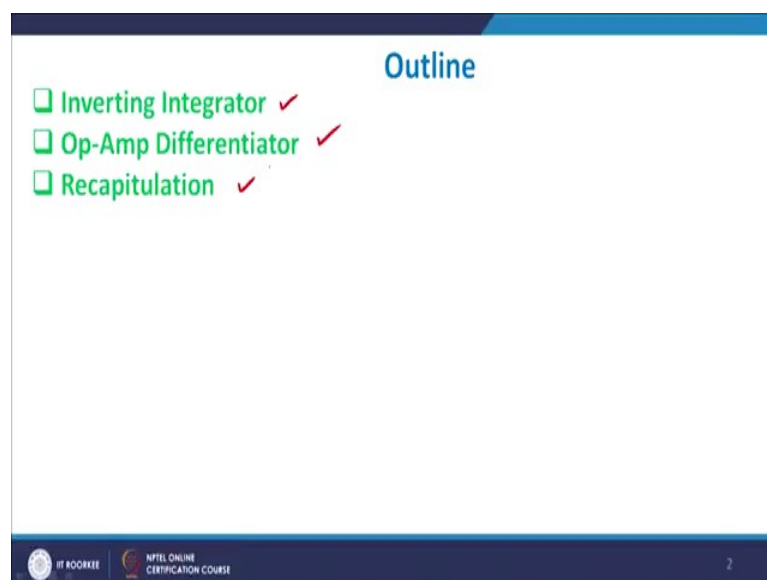
all these n number of inputs work together the output will be the sum of the outputs and this can only happen provided superposition principle is not violated under any circumstances in the circuit which you are using. So, I get V_{o1} equals to R_2 by R_1 into V_{i1} .

Next if I take V_{i1} equals to zero, I get V_{o2} to be equals to V_{i2} into R_4 by R_3 plus R_4 remember. Because V_{i2} is the input voltage multiplied by the voltage divided network into 1 plus R_2 by R_1 which is the gain of the system. This must be equals to R_2 by R_1 multiplied by V_{i2} . V_{i2} is the input voltage multiplied by R_2 by R_1 because that is in the noninverting mode and therefore you get this. Sorry, inverting mode and therefore you get R_2 by R_1 .

So, if you solve it I get V_0 equals to R_2 by R_1 , right, and V_{i2} minus V_{i1} which is also equals to R_2 by R_1 into A_{id} , right. So, V_0 equals to R_2 by R_1 into A_{id} , right. Where A_{id} , What is A_{id} ? A_{id} is nothing but V_{i2} minus V_{i1} , right. And therefore I get, therefore if you look very carefully, I get sorry this is V_{id} , V_0 equals to R_2 by R_1 into V_{id} . This will be R_2 by R_1 into V_{id} . So, I get V_{id} . So I get V_0 by V_{id} equals to R_2 by R_1 .

Now, V_0 by V_{id} is nothing but your V_0 by V_{id} output voltage with input voltage is a gain, closed loop gain and that is equals to R_2 by R_1 , right. Also referred to as differential gain, fine. So, your differential gains are just the ratio of R_2 by R_1 in case of a difference amplifier, right. And that is what you get out of difference amplifier design or issues available to you.

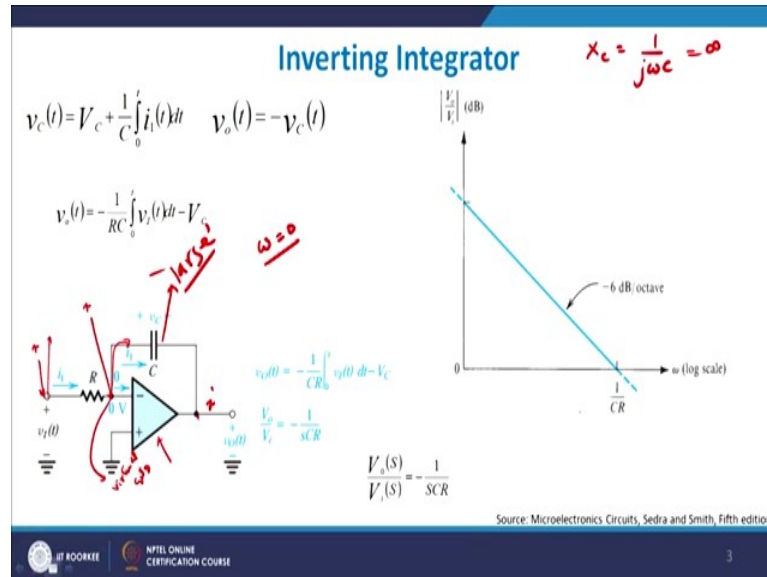
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Now, let me come to, let me explain to you the, the so, let me come to now the topic itself. Inverting Integrator, Differentiator and then we will recapitulate what we have, what has been thought to you. So, we will take up first of all inverting integrator, op-amp differentiator and

so on and so forth. Let me explain it to you, how it works out, if you see the diagram looks something like this as shown in the presentation, that you have an operational amplifier here with again inverting and noninverting terminal.

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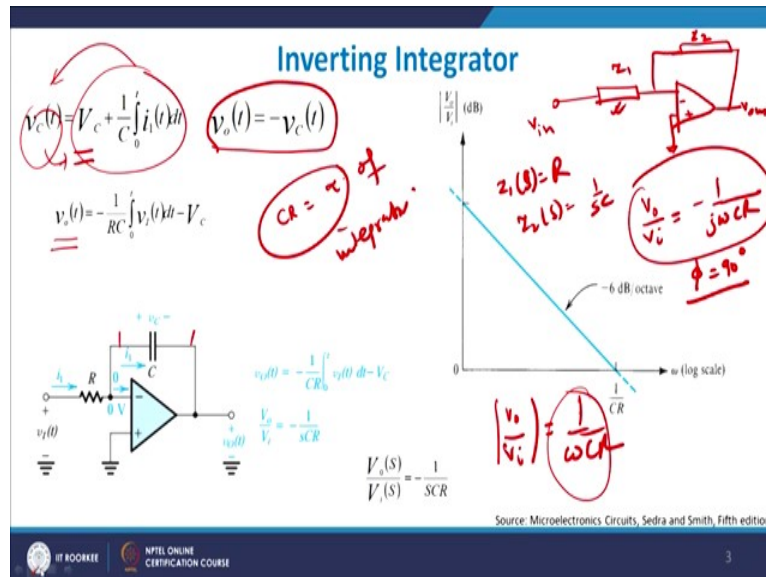
And you feed your input to the inverting terminal and you have a capacitance in the feedback loop, right. Now, quite interestingly at ω equals to zero, this capacitor will be open circuited and there will be no feedback. As the ω increases, the feedback quantity also starts to increase, right. And therefore, with rising gain or rising frequency your gain will start to fall down. This is without even doing any basic mathematics or understanding it.

We can do it by simple methodology that when ω equals to zero, X_C which is basically the capacitive reactance which is given as $j\omega C$, that comes to be infinitely large, right. So, this is infinitely large. Now, when you apply a voltage here, now you apply a voltage here this voltage will appear at this point. Suppose you apply voltage x here and the same voltage will appear across here approximately as x . And the same voltage in reality will also appear here as some value, say x ?

Now, as I discussed with you in our previous module, that this is basically your virtual ground. Virtual ground primarily means that ground where though the voltage is zero but the currents are not zero, right. So, where the current is flowing? Current is coming from here to here. A large amount of current is flowing. So, whatever voltage you are giving at the input here, here write all the, drop that voltage by R is all the current is flowing through this

capacitor C. With this knowledge let me just show to you, how does one how does one formulate a policy for inverting differentiator.

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Now, you see $V_c(t)$ is nothing but the voltage across the capacitor t , with respect to time t . So, the time time dependent voltage across capacitor C must be equals to V_c which is the initial value of the voltage across the capacitor plus 1 by C integral zero to t , zero to t $i_1 dt$ where i_1 is the current flowing in the capacitor. The standard differential equation, the standard equation which we have used based on the physics of the device and we also know that $V_o(t)$ will be minus of $V_c(t)$. Right. And the reason being here connecting a capacitor to the inverting terminal of your op-amp.

And as the result, the output will be a negative part of the input, right. So, if you want to find out the V_o value, right V_o value, so what you do is you will have a negative sign minus RC here integral zero to t $V_1(t) dt$ minus V_c , right. So, minus V_c will come on this side and minus RC by, minus 1 by RC will come here. How did I do that? Well simple, you just take this to the left hand side right, and take this to the right hand side, so I get V_c is equals to minus V_c so I get minus , so I get $V_o(t)$ is equal to 1 by RC $V_1(t)$, right.

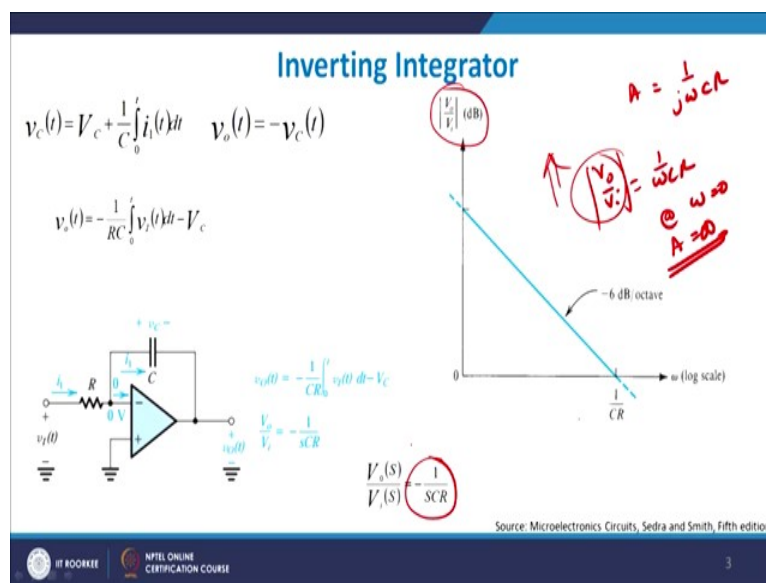
Now, this CR is referred to as τ of integrator, right. V_o is defined as the CR time constant of the integrator. Now, if I do a more generalized formulation then I can safely use it like this. I have got, say this is your Z_2 and this is your Z_1 , right. And this is your output V_{out} . Let us suppose your positive terminal which is the noninverting terminal is grounded. Under such a

direct scenario I can write down my my Z_1 Z_1 S will be equals to R and Z_2 S will be equals to 1 by SC.

So, if you place it in our initial equations, I will get V_0 by V_i to be equals to minus 1 by $j\omega RC$. So, I get the open loop gain to be equals to minus 1 by $j\omega RC$. Now, with the phase ofcourse of 90 degree. I am not interested in phase at this stage. So, if you want to find out the mod value of V_0 by V_i , right, I get this, I will get to be equals to 1 by ωCR . So, j square will be equals to minus 1 and that minus will cancel with minus and I get 1 upon ω square C square R square root over that comes out to be 1 by ωCR , fine. And that is the value of your output the gain that you see in front of you.

Therefore, if you just unable to see this, let me just see how it works out in terms of plotting a Bode Plot, right.

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So, if you look here, this is basically V_0 by V_i in dB with respect to ω which is in log scale. Now, at by my previous discussion or definition we saw that my ω , ω is, so my gain is basically 1 by $j\omega CR$ and if you do all sorts of manipulation I get 1 by ωCR to be equals to V_0 by V_i . So, at ω equals to zero, right, your your gain should be equals to infinity, closed loop gain should be equals to infinity, right, because your ω equals to zero. But, that means the denominator is equals to zero and therefore this shoots upto infinity.

This is not true and there are certain reasons for that because operational amplifier works under DC bias which is given to the operational amplifiers and any voltage larger than that will be clipped right away, right. And therefore you will not get such type of variations in

inverting amplifier. So, you see as I discussed with you I get 1 by SCR with a negative sign as the value of the output voltage with respect to the input voltage.

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$$\frac{V_o(j\omega)}{V_i(j\omega)} = -\frac{1}{j\omega CR} \quad S=j\omega$$

$$\left| \frac{V_o}{V_i} \right| = \frac{1}{\omega RC}$$

$$W_{int} = \frac{1}{RC} \quad \phi = 90^\circ$$

$$\frac{V_o(s)}{V_i(s)} = -\frac{R_f/R}{1+sCR_f}$$

Handwritten notes: $\frac{1}{SRC}$, $W_{int} = \frac{1}{RC}$, $\phi = 90^\circ$

Source: Microelectronics Circuits, Sedra and Smith, Fifth edition

If you see, I told you 1 by $j\omega$ SCR, S can be written as $j\omega$, so I get 1 by ωRC or you can write down this to be as equals to SRC. So, 1 by small SRC as your value V_o by V_i and similarly ω_{int} is equals to 1 by RC. 1 by RC is basically the time constant for the circuitry with phase equals to 90 degree ofcourse.

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$$V_o = V_{os} + \frac{V_{os}}{CR} \cdot t$$

Handwritten notes: $\omega=0$, $\frac{1}{\omega} \frac{Av=\infty}{C}$, $A_{id} \text{ (V}_o\text{)} = \text{(V}_o\text{)}$, $\frac{V_o}{C} \cdot t$, offset

Let us see what happens otherwise, what is the problem otherwise, let me say that you do have a problem that there is a off-set voltage, which means that, so what is the meaning that,

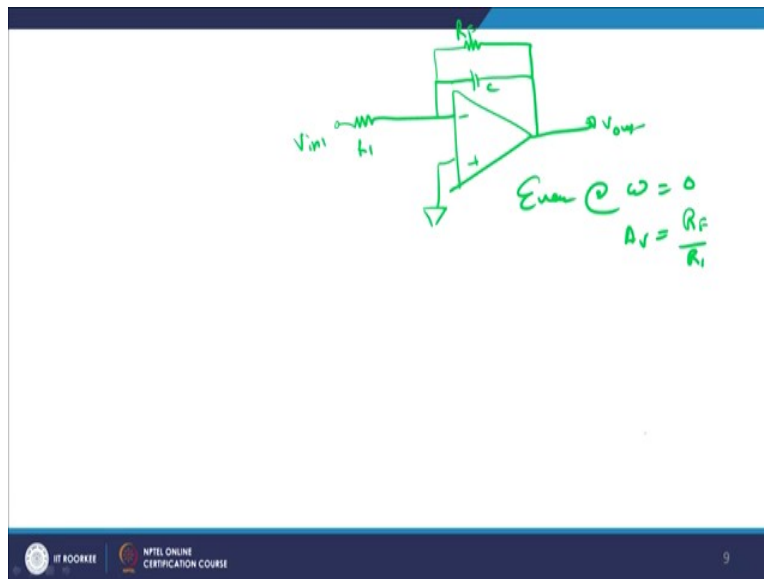
it primarily means that if the differential voltage V_{id} between the 2 terminals of op-amp is zero the output should be exactly equals to zero. Because, A into V_{id} is equals to output is equals to V_{out} . Ofcourse the common mode signal is there but this is the output voltage.

Which means that, when V_{id} is equals to zero, V_o should be equal to zero. In reality, not true, and that is what is known as a op-amp off-set. You have an off-set in op-amp, meaning that howsoever best your op-amp is, there is some finite DC off-set and that results in this chain, first thing. The second thing is, remember my previous discussion I had ω in the denominator, which means that at ω equals to zero my gain should be equals to infinity, right.

But this is not true, we very well know that any gain cannot be equals to infinity. So, how to go about doing it. So, ok, so, we will do something like this, that means if ω equals to zero, X_c opens and your feedback loop closes, there is no feedback available to you. And therefore when there is no feedback your gain will not be stabilized. That was the major reason why we went for a stability principle.

To remove that, I will show you what is the DC off-set therefore, so if I have got a negative and a positive one, right, and I have got a C capacitance here, which is V_0 and this is C and this is R, and this is grounded again, right, and this is grounded and this is C. Now, if you go back to this V_{out} will be equals to V_{os} plus V_{os} by C into R into t, right, which means that V_{os} is nothing but the output off-set voltage. V_{os} is the input off-set voltage. So, so it is something like this that you do not you do not you do not, I will just show it to you, so you what you do is you do not let it apply here and then you have voltage source and then goes to zero and this is what you what you get. So, I get V_0 equals to V_{os} plus V_{os} by CR into t, right. Into t.

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Now, what people did over the years was that, this was quite an interesting addition to the basic amplifier configuration, that if you are able to have capacitance here, right, which is V_{out} and this is positive R_1 and this V_{in1} , then if you are able to sustain or have a feedback resistance here equals to R_f , right, then even at ω equals to zero you will have a finite gain given by R_f by R_1 . So, what people did was that even at ω equals to zero my A_v will be equals to R_f by R_1 , right. And That is quite critical, which means that there is no concept of an infinite gain as such, right, and I have this R_f into consideration.

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$$V_o(t) = -CR \frac{dV_i(t)}{dt} \quad \phi = 90^\circ$$

$$\frac{V_o(j\omega)}{V_i(j\omega)} = -j\omega CR$$

$$\frac{V_o(s)}{V_i(s)} = -sCR$$

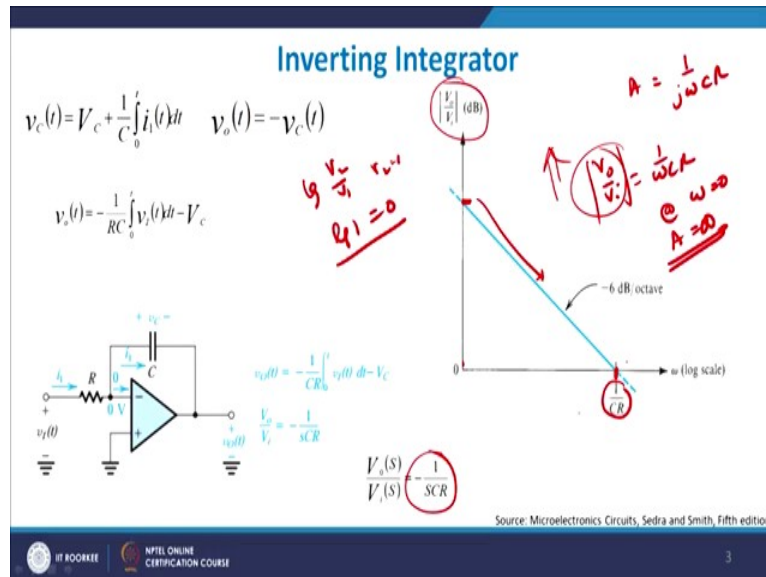
$$\frac{V_o}{V_i} = \omega CR$$

Source: Microelectronics Circuits, Sedra and Smith, Fifth edition

Now, with this knowledge or with this idea, I can I can next come to the, in here that is given by minus SCR and therefore it is ωCR as your output impedance in this case. So, the

integrator starts to behave like a low-pass filter with a corner frequency equals to zero. Why? Because, you see, if you look at. Sorry.

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If you go back, yes, if you look at ω equals to zero, I get this part as the ω starts to increase there is a linear drop with approximately 20 dB per decade or 6dB per octave drop in the gain, right, and where it cuts the ω axis we define that to be as a unity gain point. Because, $\log V_2$ by V_1 , when V_2 equals to V_1 I get $\log 1$ which is equals to zero. And therefore, this is the point where you get unity gain or the gain is unity, right. If you go below this or the negative side of the dB what will have is that the phase margin will change and all these things will happen.

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$$\frac{V_o(j\omega)}{V_i(j\omega)} = -\frac{1}{j\omega RC} \quad S=j\omega$$

$$\left| \frac{V_o}{V_i} \right| = \frac{1}{\omega RC}$$

$$W_{max} = \frac{1}{RC} \quad \phi = 90^\circ$$

$$W_{max} = \frac{1}{RC}$$

$$\frac{V_o(s)}{V_i(s)} = -\frac{R_f/R}{1 + sCR_f}$$

Source: Microelectronics Circuits, Sedra and Smith, Fifth edition

Okay, so that is the reason, with with this feedback resistance, this is the new value of your new value of your of your transfer function or the gain function which is minus R_f by R 1 plus SC , so I get R_f by R into 1 plus S can be written as $j\omega CR_f$, this must be with a negative sign given to V_0 by V_1 , right. And therefore, at ω , now if you see at ω equals to zero only this quantity goes to zero and you still have R_f by R_1 as the output voltage, variation of the output voltage.

(Refer Slide Time: 30:49)

Op-Amp Differentiator

$$i(t) = C \frac{dv_i(t)}{dt}$$

$$v_o(t) = -CR \frac{dv_i(t)}{dt}$$

$$\frac{V_o}{V_i} = -sCR$$

$$\left| \frac{V_o}{V_i} \right| \text{ (dB)}$$

$$\omega \text{ (log scale)}$$

Source: Microelectronics Circuits, Sedra and Smith, Fifth edition

Let me come to the differentiator part, Op-Amp differentiator and if you see differentiator we have just switched to the place of capacitor and register here, so capacitor is here and register is here, so I get i equals to $C(dV_i/dt)$ differential equation. So, if I take differential signal and

we try to evaluate, I get $V_o(t)$ equals to minus $CR(dV_i/dt)$. Now, now therefore V_o by V_i will be equals to minus SRC, right. Minus SRC will be the value of V_o by V_i . Now, this is the gain, so if you see at S it is $j\omega RC$ with a negative sign.

So, with this case ω equals to zero, I get this thing, so in a case of op-amp differentiator even at ω , at gain unity gain you will have your ω equals to 1 by C into R, right. So, you not gaining anything but you are actually trying to imply that at ω at certain ω equals to ω maybe t or ω b which is basically the frequency, 3dB bandwidth frequency or unity gain frequency, sorry. I get this much as amount of my output gain, right, and that is what one needs to find out or why.

(Refer Slide Time: 32:07)

The slide contains the following mathematical expressions:

$$V_o(t) = -CR \frac{dV_i(t)}{dt} \quad \phi = 90^\circ$$

$$\frac{V_o(j\omega)}{V_i(j\omega)} = -j\omega CR$$

$$\frac{V_o(s)}{V_i(s)} = -sCR$$

Handwritten red annotations include a circle around the Laplace transform equation and the text $-1/j\omega CR$.

Source: Microelectronics Circuits, Sedra and Smith, Fifth edition

Exactly, the same thing as I did it in the previous turn, ϕ equals to 90 degree, I get output voltage V_o by V_i equals to minus s times CR, right. So, minus S is minus 1 by $j\omega$ into C into R, right and that what gives you the value of your output voltage.

(Refer Slide Time: 32: 18)

Recapitulation

- ❑ The integrator behaves as a low-pass filter with a corner frequency of zero.
- ❑ The frequency response of the differentiator can be thought of as that of an STC high pass filter with a corner frequency at infinity.

Source: Microelectronics Circuits, Sedra and Smith, Fifth edition

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So, what we have done till now, we have seen that an integrator can actually behave like a low pass filter with a corner frequency equals to zero because that is what it was leading to. And the frequency of the differentiator can be thought of as that of an STC means high-pass filter, right. Your time constants, your unity gain time constants, high-pass filters, with a corner frequency at infinity, right. So, differentiator will have corner frequency equals to infinity whereas integrator will have a corner frequency of zero in ideal conditions.

However, this is not true and we will discuss all these things as we move along. But, this is the primarily 2 major portions of operational amplifier, differentiator and integrator. In the next, I will start with the numerical example and see how it works out in case of differentiator amplifier, right. Thank you very much for your patience hearing.