Microelectronics: Devices to Circuits
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Lecture 07
BJT as an Amplifier, Small Circuit Model-II

Hello everybody and welcome to the online NPTEL online certification course on microelectronics: Devices and Circuits. In our previous discussion on our lecture and the previous module we have understood how your BJT acts as a switch as well as an amplifier and where should we bias our device, so that the device works as an amplifier. In this slide we are continuing with the same thing which we have left in the previous one.

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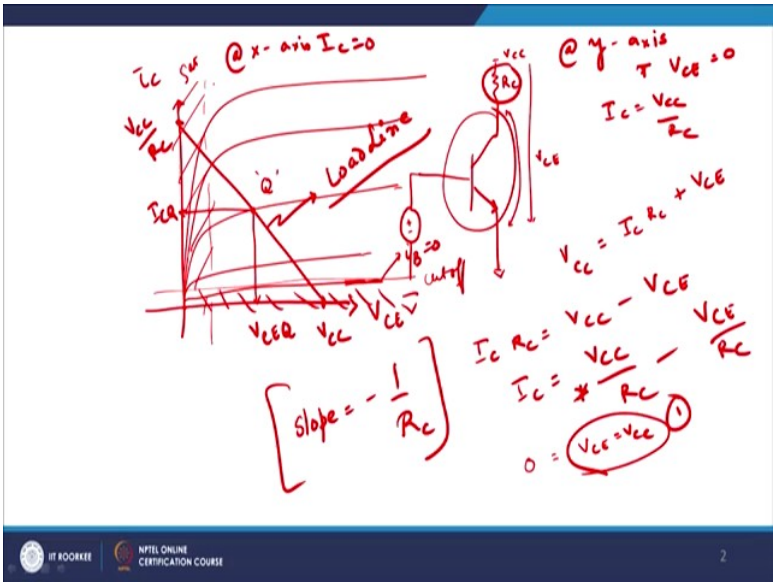

That we see that in a common emitter mode configuration, if you have a common emitter mode configuration BJT, right? Then you have R_C here, right? You have V_{CC} and then you will have, this so for a common emitter mode configuration you will have this and then there will be a bias given here and this bias will bias the device at a particular, appropriate Q-point, let's see how do, I do that. Assuming, so if you go back to this table this is basically your V_{CE}, so I get, $V_{CC} = I_C R_C + V_{CE}$, right?

So you see, $V_{CC} = I_C R_C + V_{CE}$,, therefore if you want to make $I_C R_C$ one side I get $I_C R_C = V_{CC} - V_{CE}$, so as I discussed with you I_C will be there for equals to V_{CC} by R_C minus V_{CE} by R_C. So now if you plot a graph of, let us say on this side you have got I_C, right? And on this side you have got V_{CE}, right? Now putting the same equation in this one if you look at the x-axis your I_C will be equals to zero in that case.

So when I_C equals to zero, I get V_{CE} or V_{CE} to be equals to V_{CC} so what I can point out is, that this is the V_{CC} point, right? And then on the y-axis your V_{CE} will be equal to zero. So, at *x*-axis, right? I_C equals to zero, place it into this equation and you get V_{CE} equals to V_{CC} this is the first thing you get and you place a point here. The second point is at *y*-axis, I get V_{CE} to be equal to zero.

As I get V_{CE} equal to be zero, I safely write down this to be as I_C to be equals to V_{CC} by R_C, so I put a point here which is basically V_{CC} by R_C. Now simply join these two lines and we define this to be as the load line. I will explain to you why it is known as load line. So it's a load line, whose slope is incidentally equals to -1 by *R*, fine, which means that if the resistance 1 by R_C actually this R_C is collector resistance. So depending upon the collector resistance the slope of this line will change, right?

Now wherever it cuts the *I-V* characteristics of the device, we define that to be as the Q-point those are the possible points where you will get the Q-point. So if you have *I vs V* characteristics here that's a good idea to plot it first of all like this and I get something like this then, I get this to be possibly a Q-point because within the active region this Q-point seems to be further away from saturation as well as from cut-off.

So this is my cut-off point, this is my active and this is saturation. So how did you find cut-off? Cut-off is when your I_B is zero. For any point in which I_B is less than zero, it is cut-off. So this is your cut-off region. So your device is cut-off there is no idea, this one is saturation we have already discussed yesterday and this is the active region, so you should bias your device using a DC bias, external DC bias such that the Q-point is somewhere lying here. So the Q-point is this much.

Corresponding to this Q-point you will have V_{CE} in this direction and I_C in this direction, so this V_{CE} and so we write V_{CEQ} and I_{CQ}. So I_{CQ} is the quiescent collector current and we define this to be as the collector to emitter quiescent voltage, right? And once you have found out, now what you do? With this value of a voltage and current, if you give in the input side using a DC bias I superimpose my AC signal over this DC bias, right?

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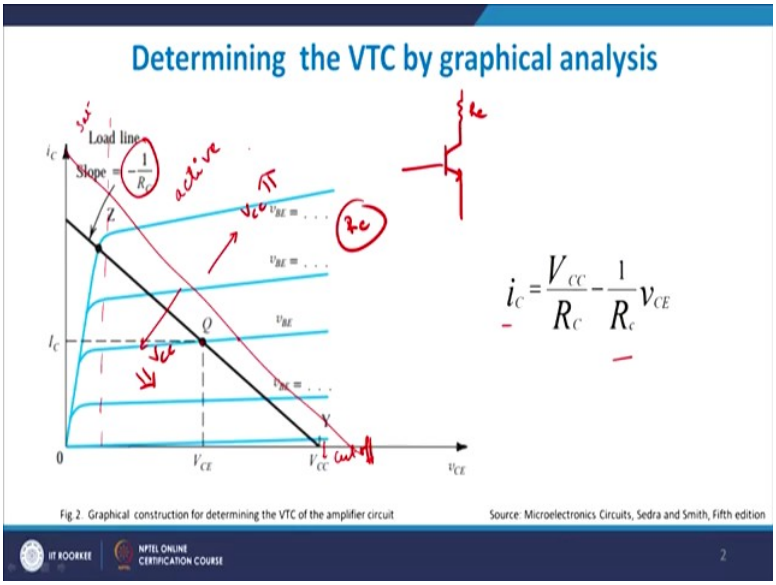

And that is what they're trying to do over the period of time that we are trying to find out our DC signal, so as you can see from here the Q-point is somewhere, well so you see this is your saturation region, this is your active region by the definition we are handling and below this you have got cut-off, right? And this is the Q-point which you see for various values of I_B, right?

It is actually V_{BE} because I_B will depend upon also the value of V_{BE}. Now I_C is by this and therefore the slope is equals to minus 1 by R_C and therefore this is known as load line but you go on changing the load here, right? You go on changing the load here and you automatically get… So if the R_C value is now smaller the slope will change drastically, right? The slope will be something like this now. It might be something like this, right?

So if you make your V_{CC} larger and larger the load line will move to the right. If you make it smaller and smaller it will move to the left. So it will move like this, if V_{CC} is made high, right? And it will move to this side if V_{CC} is made lower, right? And depending on the value of R_C the slope of the load line will go on changing, fine. So we have therefore found out a graphical method by which we can predict what should be the Q-point or the bias point where my device should be sitting, so that in the active region so that a proper amplification is available to me, right? That is very-very important here I wanted to tell you.

Ahh.. This is the, therefore this is the graphical method of determining the VTC the voltage transfer characteristics. And this gives me a quite a nice idea about or a decent idea about where should the bias point or the Q-point should be kept in general.

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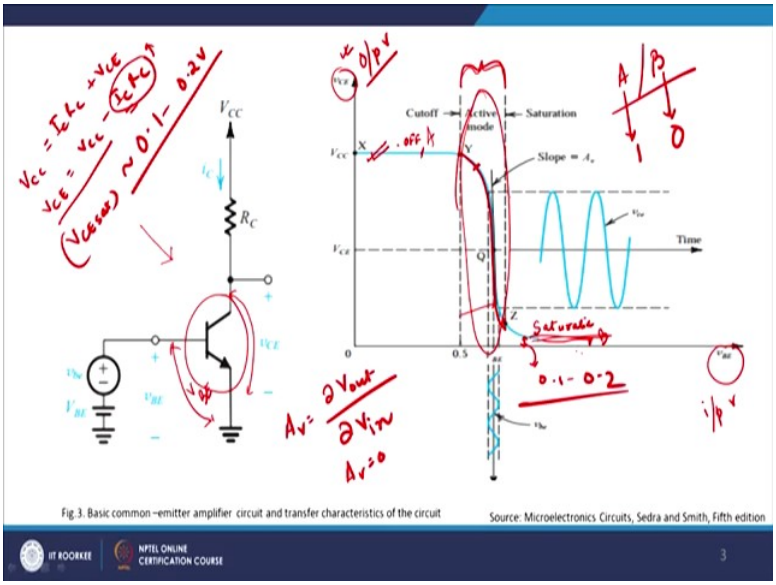

With the same concept we have learned till now, let me show you a proper amplification here. Now as I discussed with you that this is the common emitter mode configuration transistor which you see, this is my NPN transistor. V_{CE} is this voltage is V_{CE}, this is V_{BE} which you see, right? And this is your V_{CE}, right? Now if you, as I discussed with you for low values of V_{BE} typically your, the device will be cut-off because base to emitted junction will not be forward biased for silicon it is 0.7.

So anything below 0.7 cut-off, cut-off means this is zero. Zero means all V_{CC} appears across the output voltage and this is what you see here. So this part is that discussion which you will see. Similarly if your input voltage V_{BE} is very large as compared to the cut-in voltage of the base emitter junction which is 0.7 for silicon, I would expect to see the transistor to get on, so I will get from off-state, so this is cut-off state and I will get on-state, right?

This is the on-state, right? And I get saturation here, right? I get saturation. So saturation is there and the output voltage will certainly fall off. Why it will fall off because if you remember, $V_{CC}=I_C R_C+V_{CE}$, right? So if you take it this side and do sort of try to find out the value of $V_{CE}=V_{CC}-I_C R_C$.So when your I_C is zero, you get V_{CE} equals to V_{CC} and that's what you get here.

When you have large values of I_C this quantity becomes large and what you get is V_{CESat} or the saturating value of V_{CE} which is approximately 0.1 to 0.2 volts typical value, so this value is approximately equals to 0.1 to 0.2 in saturation, fine? Now you see if you bias it here point '*A*' let us suppose or you bias it here let me say here, right?

Point '*A*' and point '*B*' if you bias it obviously point '*A*' and point '*B*' will give you a DC bias, external DC output voltage. Point '*A*' will give you output 1 and point '*B*' will give you output 0 as you can see from the definition of output here but let's concentrate on the part where this active region is there or active mode is there, right active mode? In the active mode if you see the voltage is drastically falling V_{CE} with the small change in the value of V_{BE}.

So this is basically V_{CE} vs V_{BE}, so this is the output voltage and this is the input voltage. So this is my input voltage, right? And this is my output voltage so you see, so I define my voltage gain A_V to be equals to ∂V_{out} to ∂V_{in}, right? This we have already discussed, so if you look at point '*A*' my ∂V_{out} is 0, so my A_V is zero because there is no change in the output voltage is constant, independent of the input voltage.

Similarly at point '*B*' again my output is constant, independent of input voltage. So in both the cases my overall gain (A_V) is zero, voltage gain is zero but the voltage gain in the active mode which is this one is pretty high because you see a very small change in input gives you a large change in the output, right? But the change is what? Negative change. So I get a negative gain sort of concept which means that for an increase in value of input, I get a decrease in the value of output, right?

And the decrease is not equal but it is a very large decrease, so you get a large voltage gain. So higher the slope of this curve from '*Y*' to '*Z*' through '*Q*', more will be the gain or more will be the slope and more will be the gain of the transistor, right? So if you want to operate the device as an active device then please operate within this region which is dotted here and if you don't want to operate and let it work as a digital world you operate in these two positions.

So when you use TTL logic, you use this right transistor-transistor logic. When you want to use it as an amplifier you use this, right? So we have made one thing very clear here that for sure therefore, that if you have a BJT working in the active mode of operation and I am biasing my device in the active mode I am surely getting a large level of amplification to me, right? And is amplification will be linear amplification, right? And I will also find, will show, I would like to convey to you why is it like that also.

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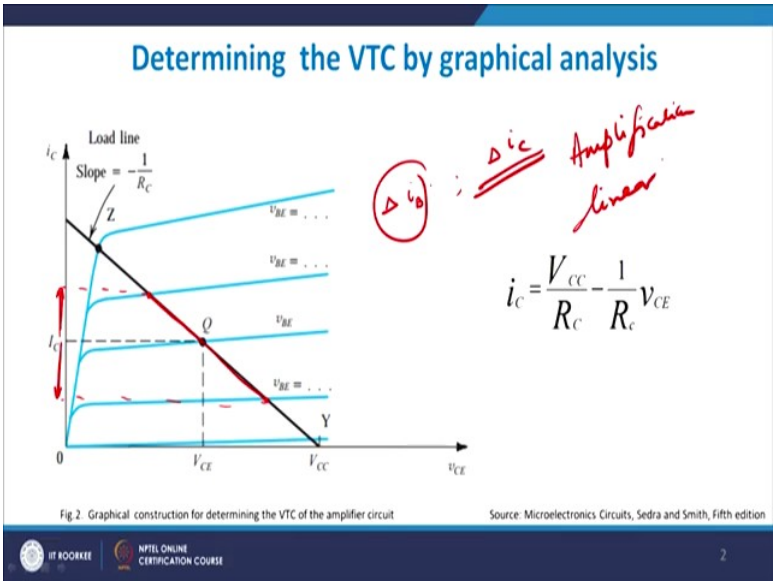

The reason is something like this. The reason is that for equal change in the value of base current, I should get an equal change in the value of a collector current, that is what linearity means. That if I do similar changes in I_B, I should expect to see a similar change in I_C also, right? So you see if you change I_B by this much amount, right?

Such that the Q-point shifts from here to here from this point and then goes from here to here, right? But the change in I_C is linear, so this distance is exactly equals to this distance, right? And therefore we safely say that the amplification is linear in nature, so the amplification which you find out amplification is primarily linear in dimension, sort of linear in nature, right? But the reason being that you are able to, because the rate of change is almost constant for both the cases, fine. And that makes our life easier as far as understanding the graphical analysis is concerned. So you see I gave an input, so my input will be given, so…so… let me therefore recapitulated, so what you do?

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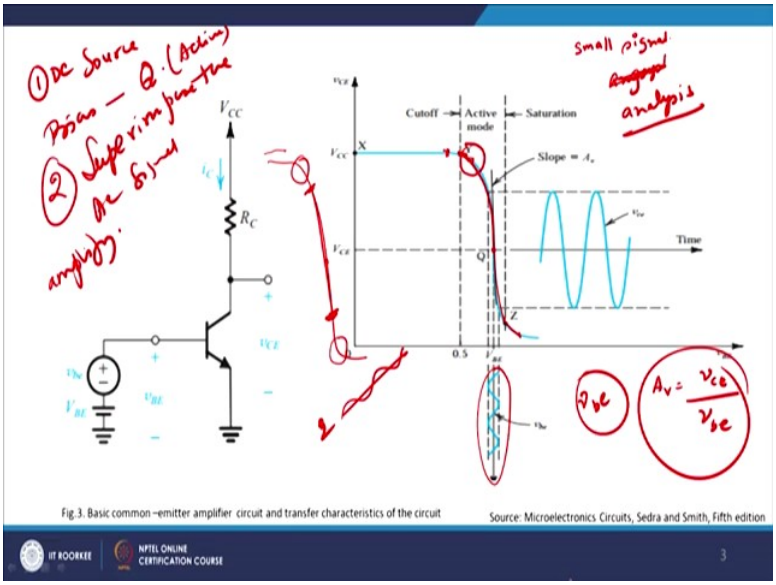

You first insert the DC source, right? You bias the device where, so that it is in the Q-point in the active region for amplification purposes, right? And then superimpose the AC signal, right? Which you want to amplify, right? So you superimpose the AC signal which you want to amplify. So what is the AC signal here?

The blue one if you see here, this is my input AC signal and we are giving it to as V_{BE}, so I am giving as V_{BE} base to emitter voltage change, so I have a DC bias, say 2 volts and 2 volts DC bias is kept superimposed on that I have my AC signal, small signal AC signal, fine. One important point which I should point out here is that there is a limit of the input AC signal.

You just cannot give any AC signal you want and it will work fine for the BJT for example, specially the peak-to-peak value, right? If the peak-to-peak value, suppose you are biasing Q-point here and your peak value is so large that it makes this Q-point go somewhere here in the non-linear region or even here or on the negative side get somewhere on the non-linear region or even here, then you enter into non-linear amplification domain.

Although your amplification fall down, not only that it will depend upon the value of input not a good idea. So you see therefore, we always consider this to be as a small signal analysis, right? What is the meaning of small signal analysis? It means that, that your input signal is so small peak-to-peak that I can sufficiently state that the amplification is linear because if the input signals are too large then the Q-point will move so much away from its basic V_{CE} value which is kept here, right?

That it might even go up to this much point, here. Here if you see it is something like this, it is coming like this and then it fell like this and then it became linear and then it became like this, so if you are somewhere working here or here, it is basically non-linear and as a result you will get a non-linear amplification. So you need to bias the Q-point such that you are just restricting your peak-to-peak between this point and this point, right?

So you should be very careful how you are biasing you device, depending on that will get the output. So depending on that you are getting the output here which is 180 degree phase shifted as well as amplified by a factor which is equal to value known to you. So what will be the small signal gain which you will get? A_v will be equal to V_{CE}, right? Divide by V_{BE} typically that will be the voltage gain which you will see out of the signal, right?

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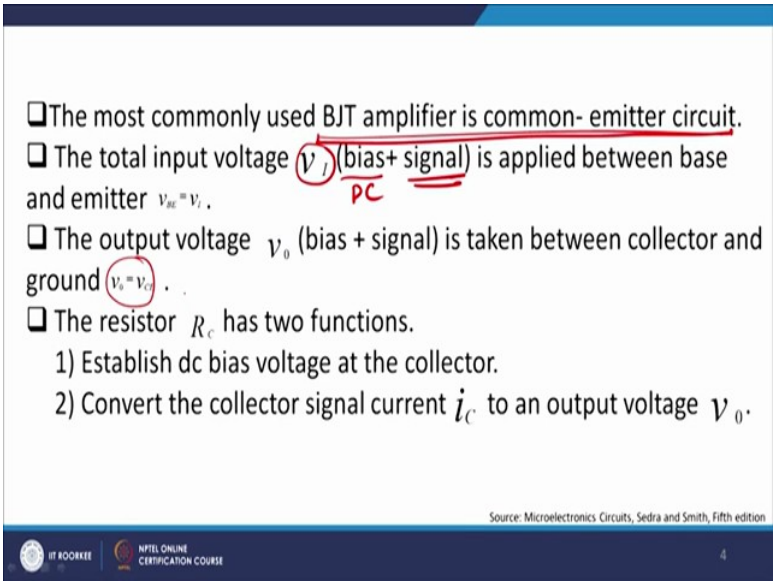

So with this we have understood the basic amplification process of a BJT, so as I discussed with you earlier also, in the earlier module as well as in this module the most commonly used BJT amplifier is the common emitter amplifier, right? So common emitter amplifier or common emitter circuit is the most commonly used amplifier design. Now, my input signal as I discussed with you, will always be a sum of the DC bias plus the signal which you applied, right?

So, V_{in} is the input signal will be a sum of the AC signal plus the DC bias. So DC bias will fix up the Q-point and AC signal will be a signal which will be given, which will shift the Q-point so that you are able to amplify the signal between input and output. Now the output range is V_{CE} as I discussed with you, right? And it cannot go beyond a particular region. V_{CE}

should also be limited by certain things. Just as I should make it a point that V_{CE} cannot be more than of course V_{CC} I will give you an example.

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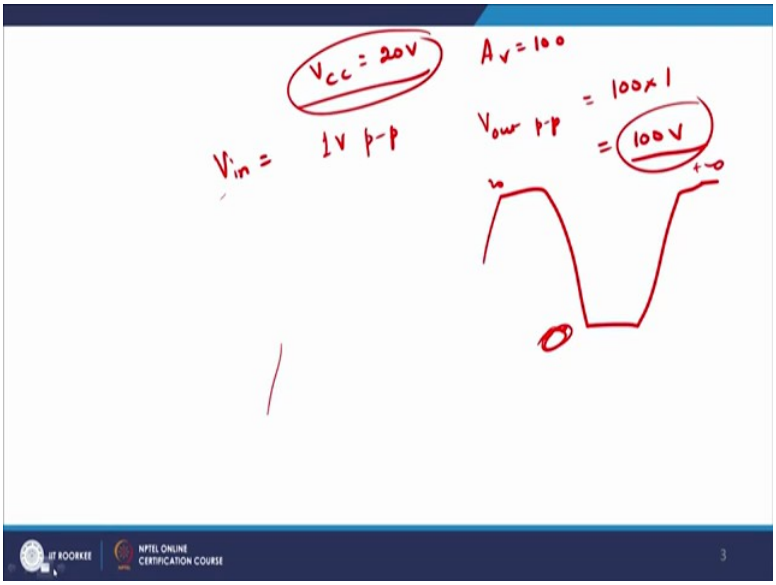

Let us suppose you have an input signal which is 1 volt peak-to-peak, right? You have V_{in} which is 1 whole peak-to-peak your A_v is 100, right? And your V_{CC} is let us say, 20 volts for a BJT, right? So what will be your V_{out} peak-to-peak? It will be 100 multiplied by 1 which is equals to 100 volts, fine. So your output is 100 volts but your V_{CC} is only 20 volts, so you see that in no way we can get 100 volts output.

So what will happen is that it will go up to 20 volts, it will then clip back here, because this is +20 this is -20 whatever +20 and so on and so forth, because zero it will go to zero and not go further down, right? So you see therefore that the output of a BJT will depend not only on the gain, small signal gain of the amplifier but it will also depend upon the V_{CC} which you are using or the amount of bias you are using to get those functions.

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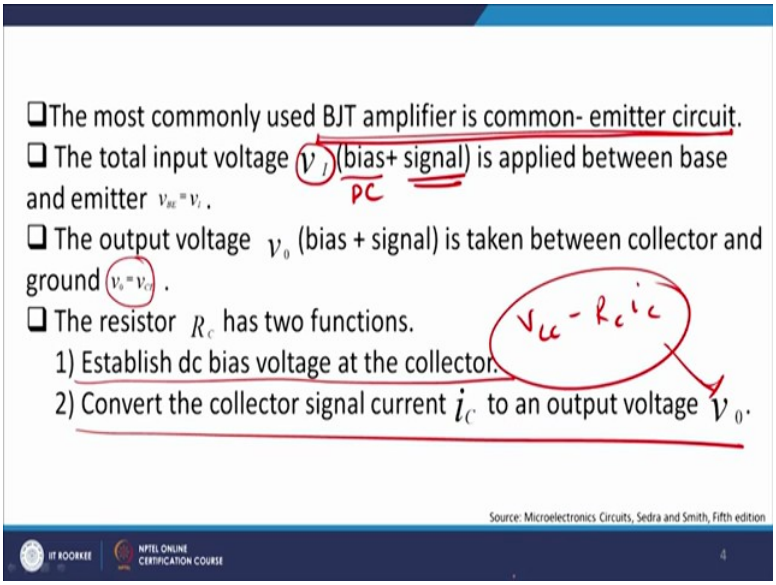

The resistor R_c has two functions. We have already discussed this point R_c will help you to establish a DC bias, so higher is the value of R_c slope will be lower but with a negative sign, right? And lower the value of R_C higher will be the slope with a negative sign. The slope is from the side, it is not like this, it is like this. So you will always understand that the slope is negative in the sense.

And second is that more important point is that, I_C multiplied by R_C is the output voltage, now it is the voltage across the value of, so this is the reason why we convert collector signal current to, so I_CRc, right? So V_{CC} minus i_cR_c, is the output voltage. So R_C has two components or two issues, one is to establish a DC biased and the collector and the second portion is to convert a signal current, collector signal current Ic to its output value voltage V_0.This gives me a basic idea about the basic amplification process of BJT.

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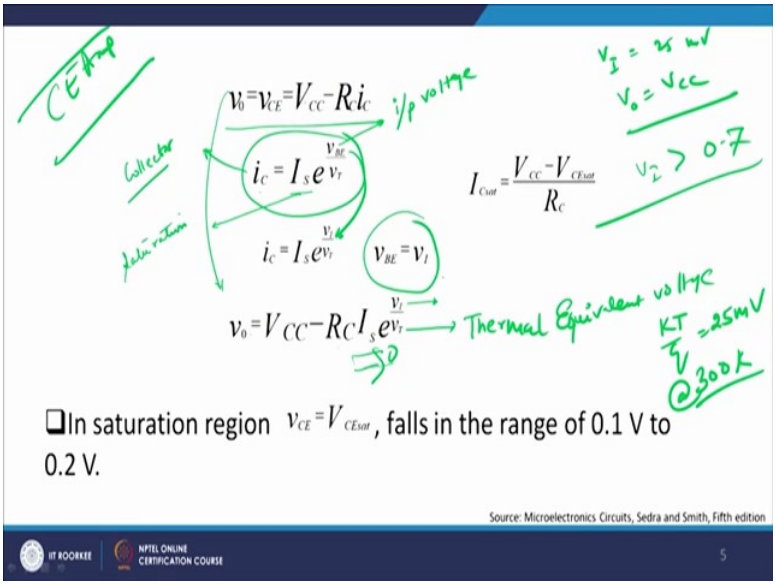

Let me give you the mathematical treatment here. So if you look very carefully V_0 which is in front of you, right? V_0 is there, right? If you look at V_0, this V_0 is the output voltage and is equals to obviously V_{CE} must be equal to V_{CC} minus $I_C R_C$, remember? We have already discussed this point. My yesterday's talk or previous modules talks we have seen that I_C was equal to $I_s e^{\frac{V_{BE}}{V_T}}$. I_S is the saturation current this is the saturation current which you see, this is the saturation current, right? This is the collector current and V_{BE} is the input voltage in the case of common emitter. In case of common emitter amplifier and therefore I get I_{Csat} to be equals to V_{CC} minus V_{CEsat} by $I_C R_C$ and I think this is pretty clear. So V_{CC} minus V_{CEsat} by R_C gives you I_{Csat}.

Now since I_C therefore is equal to I_S, so V_{BE} is now replaced by V_I, we have just discussed this point why? Because I can safely say that the total voltage is a sum of the DC bias which you are giving and the AC bias of the signal which you want to amplify, right? So these are the two important voltage sources which you are trying to do. So I get V_0 therefore this statement it goes to V_{CC} minus R_C times I_C, I_C can be written therefore $I_s e^{\frac{V_I}{V_T}}$. right? Is it okay? Now therefore you see very interestingly that the output voltage V_0 has an exponential dependence on the value of your input voltage V_{in}, right? Which means that if V_{in} increases even by a small amount, I would expect to see a drop in V_0 by a large amount because this is an exponential drop which you see. V_T is the thermal equivalent voltage which is given as KT by q and this equals to 25 mVs at 300 K.

So at 300 K, V_T equals to 25 mVs, right? So if your V_I is let us suppose is, so if my V_I is 25 mVs, right? So e[1] will be equals to 0 and therefore I get V_0 equals to V_{CC}. Remember as long as V_I crosses 0.7, I will expect to see V_0 to be equals to V_{CC} because this will effectively g_o to zero, if not exactly go to zero, right, in the saturation region, which is the saturation region after the active region expands.

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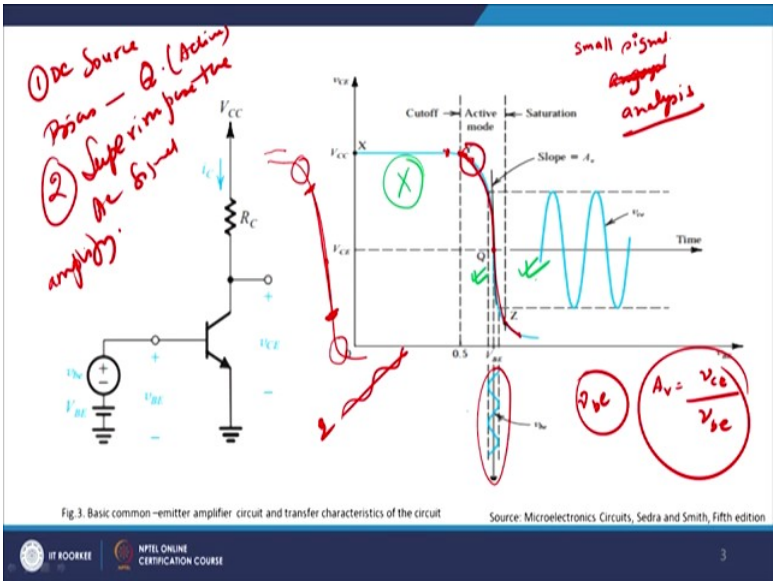

So, I have got if you look carefully I have got this thing that I have got cut-off region which is this one, right? This is the cut-off region then we have the amplification region with the active mode and I have got a saturation region here. So cut-off region, active mode and saturation it will vary depending on the value of V_{BE} which you are choosing. So depending on the value of V_{BE} we can think of active and saturation region, right?

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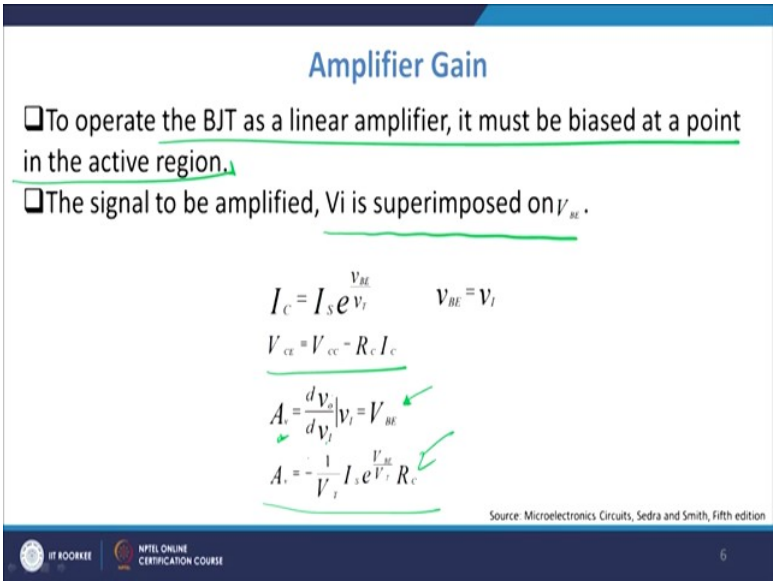

With this knowledge we have gained till now, let me see as what we are looking into. So we are looking into the fact that therefore to operate the BJT as a linear amplifier it must be biased at a point in the active region, we have discussed this point already time and again that we need to bias it, amplifier. And then V_I is therefore superimposed on V_{BE}. We again discussed this point in a much more detail manner.

So I get $V_{CE}=V_{CC}-I_C R_C$, so I get A_v to be equal to $\partial V_0 \, \partial V_I$ which means the rate of change of output voltage with respect to change in the input voltage for a fixed V_I comes out to be V_{BE}, right? So A_v is equals to V_{BE}. A_v also comes out to be equal to -1 by V_T, $Is\ e^{\frac{V_B}{I_{RC}}}\ I_C$. Please do it yourself you'll find this answer very straightforward and simple, right?

And I will therefore get a negative sign expected also because of slope is negative and therefore I should get a negative gain. Negative gain primarily means with increasing voltage, input voltage the output voltage is decreasing and that is the reason we define that to be as a negative voltage.

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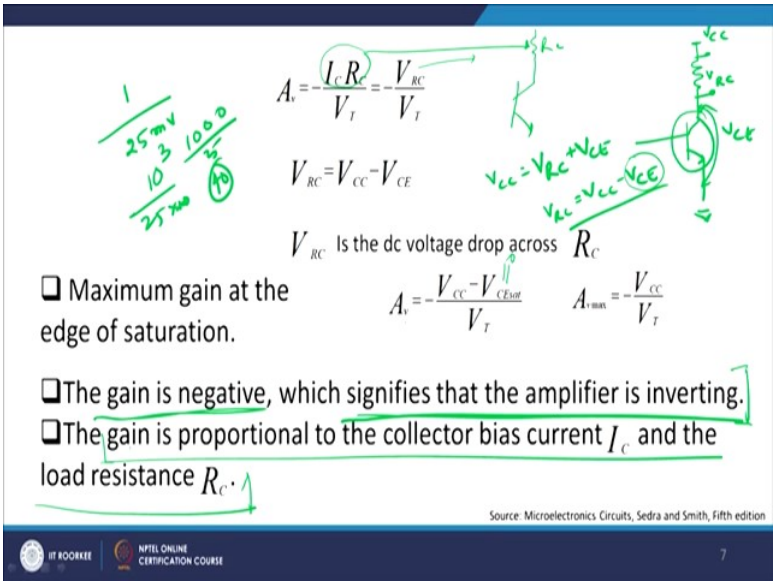

Therefore I get A_v to be equals to minus, why did you get A_v equals to this thing whole quantity. Now this quantity is basically I_C, so I get $I_C R_C$ by V_T. So this is basically the voltage drop across the resistance at the top, right? This is the resistance *Rc*, so this voltage is basically the drop at this resistance *Rc* and that is equals to minus V_{RC} by V_T, right? Now V_{RC} is equal to V_{CC} by minus V_{CE}, remember why?

Because you had a resistance here and you had a, this thing therefore we get V_{CC} is this one, right? And so V_{RC} is this voltage, between these two points and this is V_{CE}, right? So I can write down V_{CC} to be equals to V_{RC} plus V_{CE}, fine. And therefore we can write down V_{RC} to be equals to V_{CC} minus V_{CE}, right? So in saturation this V_{CEsat} will be typically very small and V_{RC} will be approximately equals to V_{CC} and you get a very high gain, right?

So, But then you have to ensure that you don't go into saturation because then V_{CE} sat will be typically very small. So where do you say? You stay within the active region of the operation of the device. So therefore I get A_v to be equals to minus V_{CC} minus V_{CEsat} by V_T and therefore the maximum value of A_{Vmax} is V_{CEsat}, so if I assume this to be equal to 0 approximately I get - V_{CC} by V_T as the A_{Vmax}.

So you see even if I use V_{CC} of 1 volt and if 25 mVs you are getting here, so I will get 1 by 25×10^{-3}, so I get 10^{+3} here, so this is basically thousand by 25 which is basically 40, right? So even if you don't do much manipulation and incidences, what you get is primarily that the voltage gain of a common emitter mode configuration at *T* equals to 300 K happens to be maximum value attainable is basically 40.

But then this is assumption that V_{CEsat} equals to 0 which is never. So actually I will get a drop in the value of V_{CE} in the A_V value. In reality A_V will be much smaller than 40 even, right? And that you have to take care of when you're actually designing a system. As I discuss with you therefore, the gain is negative, right? The gain is negative which signifies that the amplifier is inverting amplifier.

So I have an inverting amplifier available with me and the gain is negative this thing. Further the gain is proportional to the collector bias current I_C and a load resistance R_C. This we have already seen and you know the reason why the gain is like the collector current and basic reason is there. So before we finish this module of lecture let me recapitulate what we did. We had looked into BJT as an amplifier.

We have also understood the various parameters which we need to fix from DC domain in order to bias it in the active region of operation. You cannot bias it in a saturation or in the cut-off region, you have to bias it only in the active region. When you bias it in the active region you automatically get a very large gain. We also saw that theoretically speaking the maximum gain available to us in a common emitter mode configuration is minus 40 times, right?

Provided you are giving a V_{CC} of 1 volt, I get V_{CC} by V_{TS} the maximum theoretical limit which you get in the voltage gain. In reality, obviously we will not get because V_{CEsat} will never be equal to 0 it will have some finite value and therefore your A_{Vmax} will reduce drastically in that case, right? So this takes care of the basic understanding of our design and in the next turn we will be looking into small single models BJT, right? Thank you very much.