VLSI Physical Design with Timing Analysis

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Lecture 11

Timing Analysis in a Sequential Circuit

Welcome to the course on VLSI Physical Design with Timing Analysis. In this lecture, we will discuss about how the timing analysis can be performed in the sequential circuits. The content of this lecture includes timing analysis of sequential circuits. The timing analysis of a sequential circuit is divided into two types: one is called maximum timing analysis or setup check, and the second one is the minimum timing analysis or hold check. And all of you know that there is a variation of process from one chip to the other chip. So, when the chip and when we do the timing analysis, how we can check the different process corner to check the extreme condition of setup and hold violation will also be discussed in this lecture. Let us say if we manufactured a chip and after the manufacturing of the chip, we have a setup violation, then how we can solve the issue. And if you have a hold violation in a manufactured chip, how we can solve the issue, those also will be discussed in detail. So, in the last lecture, we discussed about the setup time and hold time. The setup time is basically the time before the rising edge of the clock, the data should be stable such that it can be captured by the flip-flop properly.

Then, the hold time is the amount of time after the rising edge of the clock; the data should be stable such that it can be sampled by the flip-flop properly. So basically if you can see here, so there are some parameters which is related to flip-flop. So one of them is called the setup time, t setup. Then the second one is called the t hold, the hold time. Then you have the third parameter, which is called tccq or minimum; I can also write this term t clock to q minimum; this is called the contamination delay, contamination delay between clock and the q, between the clock and the q. Then fourth one is tpcq. So, I can t clock to q maximum, I will use this term, the propagation delay between clock and q. So, this is the contamination delay, the minimum delay, this is the minimum delay, and this is the maximum delay between the clock to q. So tccq is a clock to q minimum, tpcq is clock to q maximum. Then you have the tcd is also I will denote by t combinational

minimum; this is the contamination delay of the combinational path, combinational circuit.

Then the fifth one, the sixth one is tpd, which is t comb maximum, which is called the propagation delay of the combinational circuit. So here, the delay of the combinational circuit is the minimum delay of the combinational circuit, and this is the maximum delay of the combinational circuit. These four are the parameters of the flip-flop and these two are the parameters of the combinational circuits. So, whenever we will do the maximum timing analysis, we will have to have both together. So, I will give some examples of where the sequential circuits are used. For example, it is used in finite state machine, state machines efficient. In this case you have inputs, you have some combinational logic, then you have basically flip-flops are used, I have discussed flip-flops. Then output of that one will store the state and will go back go as input to the combinational logic. So, this is input and it will create some output. So, basically, this is a schematic of a finite state machine.

Similarly, it is also used in second example is pipeline design. So, what is this pipeline design? In case of pipeline design, let us say I have a bigger combinational delay, I will divide into smaller delay and I can place the flip-flop between the combinational delay. For example, this is a flip-flop, this is combinational one, then this is another flip-flop comb 2 like this. So, all are clocked with the same clock. These are some examples of sequential circuits. It is used in other places like shift registers, counters, many more places. Wherever you need some kind of sequencing, in that case, you need sequential circuits. Now we will discuss about the maximum timing delay constraint, max timing analysis of flip. So, earlier case we discussed one flip-flop. In one flip-flop, we have set up time, hold time, clock to q delay. So, one flip-flop has 3 parameters: one set up time, second one is hold time, and third one is clock to q delay. Now, I am considering 2 flip-flops, and I am putting some logic in between. So, how it looks like? I have a flip-flop here, I have another flip-flop here. So, in between there is some logic is there. So, this is clock, this is clock, they are connected, same clock is going to both of them.

Then you have a D pin, this is the IN and this is a combinational delay. Then this is the D pin, this is the Q, this is the Q. Now what we are doing? We have 2 flip-flops, flip-flop 1, flip-flop 2. So, this is called launch flip-flop and this is called capture flip-flop. So, because it is launching the data that is why it is launch flip-flop and the flip-flop 2 is capturing the data that is why it is called the capture flip-flop. Now we will see that how the maximum timing analysis can be done in this case. So, basically here if I do any data, I will draw the waveforms then I will do the analysis. So, basically, if I have a time t equal to 0, I am starting here. So now first one is the clock, I have a clock signal. I have a clock signal.

I am making it bigger to make it more clear, but you can draw smaller also. This is a clock. So, this is a clock then you have a D input. So the D input before the setup time. It is captured properly by the flip-flop like this. So now my Q will take some time to appear at the Q. This is the Q. So, the Q will appear after the rising edge of the clock. So, this is the rising edge; this is the rising edge. The clock will change in this rising edge. So, if you can see here, basically, your Q is initially 0, and it will change after a certain delay. So, this delay is called, this delay is called t clock to Q delay. t clock to Q whatever the symbol I have used here, t clock to Q maximum. t clock to Q maximum because I am doing max timing analysis. So, it will take some delay and it will appear at the output. Now it will like this. See again it is basically getting 0. If you can see here, it will go delay of same clock to Q delay and after that will go to 0. So, this is also t clock to Q maximum. Now my data is there. Now I will do the combinational delay.

So, this delay whatever I have included is t clock to Q maximum. After that from here to here is t combinational maximum. So, now if I have D2 or the D of flip-flop 2, so, how it will look like? It will come here. This t comb max is little, bigger. So, it is going like this. It should be settled somewhere here. So, it should come before the setup time of flip-flop 2. Otherwise, it will not captured by the flip-flop 2. So, the flip-flop 2 should the delays from here to here is basically t comb maximum. Now your data should be stable before the setup time from here to here.

This distance should be greater than setup time, or minimum, it should be equal to setup time. So, this is my total time period from here to here. Now I can write my max timing delay equation where

$$T_{clk} \geq t_{cq}^{\max} + t_{comb}^{\max} + t_{setup}$$

So now this same thing we can use the other notation t clock to Q, this would be

$$T_{clk} \geq t_{pcq} + t_{pd} + t_{setup}$$

So, both the equations are same. I have used t clock to Q maximum. In books, it is written as tpcq. I have used t comb maximum. In the book, it is tpd, and t setup is same as t setup. So, this is my max timing constraint. So, we start with one clock edge or the first clock edge, this is the first clock edge and end with the second clock edge. Whenever we are doing max timing analysis, we have start with one clock edge end with the second clock edge to find the clock period. This is your clock period t clock actually. This is your t clock. This distance from here to here is your t clock.

So, now basically, if you can see, we have find out the t clock. So then we can find out my maximum frequency of operation. So whenever I am finding maximum frequency of operation, I have to check what is the worst case t clock that satisfy all my flip flops in

the design. Not only two flip flops, let us say variety of many flip flops are there inside the design. All the combination delay, all the path I need to find out which is giving me the maximum delay t clock max, I have to take that one to find the frequency of operation. My frequency of operation, maximum frequency of operation I can write it here max frequency is basically

$$Max \;\; freq = \frac{1}{T_{clk}}$$

So, you have to remember this. So we have to find the worst case t clock which satisfy my constraint, then from that I can find out the max frequency f max. And second point here is important is that we have several corners are there. What is this corner? Whenever you have do chip design, we have NMOS and PMOS transistors are used.

We have NMOS transistor and we have PMOS transistor. These two transistors are used. So in some process NMOS has three flavors. One is it is slow, then typical, then fast, then PMOS is also slow, then typical, then fast. The types of corners are one is SS slow slow, your NMOS is slow, PMOS is slow. Slow slow means SS means slow slow. I will not write for other thing. Now I have TT typical; then the third one is FF, then the fourth one is FF means fast fast both NMOS is fast, PMOS is fast, then I have FS, NMOS is fast, PMOS is slow, then the fifth one is SF, NMOS is slow, and PMOS is fast. So these are the corners related to your basically transistors. There is also we have temperature, we have voltages is also there, but I am not we can include the temperature and voltage also. Let us say if you include the temperature, there will be another parameter, then the fourth one is the voltage. So, I am looking only into the process now basically this SS TT and FF. So if I do the max timing analysis, which corner I will do the analysis. So, whenever my worst case condition should come, whenever which case my worst case condition will come basically I have to consider the worst case delay, when the delay is maximum, when both NMOS and PMOS are slow. So for max timing analysis, max timing analysis we have to use SS corner. So now we will go into the minimum timing analysis.

So, in case of minimum timing analysis, we need to consider the basically hold time. So here, basically, we need to consider the hold time. So let us say I have flip flop, one flip flop, I have another flip flop, this flip flop 1, flip flop 2, I have clock, the clock is same for both of them. This is called launch; the flip flop 1 is called the launch flip flop, flip flop 2 is called the capture flip flop. Now you have a D pin, then you have a Q pin, and you have a short delay. In the case of minimum, I have to consider the minimum delay between the minimum combinational delay all the things should be minimum. So this is the D pin, this is the Q pin. So now what are the parameters important in case of basically minimum timing analysis, one is hold time, then the second one is basically TCCQ or this is called the contamination delay or minimum delay. Whenever your clock

changes, what is the minimum time the Q will appear that is your clock CCQ. So, I can also denote this by T clock to Q minimum, this is a contamination delay.

Then the third parameter will be responsible for this is called TCD, basically, TCD is basically the combinational minimum combinational delay, or I can denote this by TCOM minimum. These three parameters are responsible for minimum timing analysis. So, let us take the clock. So basically, I will draw the timing diagram and explain this whole time, whole check, or this is also called the whole check, in detail. So now I have a clock signal, I have a clock signal, this is my clock. Let us say my D is here, this is my D. Now I have a Q, the Q of the flip-flop one. So, in this case, it will take after the rising edge of the clock, so this D is also the flip-flop one. Now, after the rising edge of the clock, then your Q will come out after some delay; what is the minimum delay it will come out so that delay I need to consider. This is my basically the T clock to Q minimum. So, then this delay similarly here also the same case, it will take what is the minimum time it will come out that needs to be taken.

Now what will happen is that now I have D pin of the flip-flop two. Now I have the D pin of the flip-flop two before D pin of the flip-flop two. So, it will take some time, but let us say this delay is after that I have to calculate, after this edge, I have to calculate. So, this is my basically minimum delay. This t come minimum. This from here, I will now use a different color. From here, this clock is to this edge, this delay is my, what will be my delay, this delay. That delay is basically

$$t_{clk}^{\min} + t_{comb}^{\min} \geq t_{hold}\ (FF2)$$

So, why it is needed? What is the problem if we do not meet this constraint? So, if you do not meet this constraint, the data, the previous data stored at this node will be overwrite by the new data what is coming to the flip-flop one. Basically, if you can see here, your data arrival time at the flip-flop two and basically and the clock arrival time at the flip-flop two must be larger than the whole time of the flip-flop two. Otherwise, what will happen the previous data what is stored at this node will be overwrite by the flip-flop. And second thing, if you can see, unlike the setup time, I will write the difference in case of setup time; we are using two clock edges for verification. But in case of setup time check or the minimum, then the whole time check we are using one clock edge, the same clock edge we are checking for. And there is one important point here is that whatever I discussed about corners, whatever I discussed about the corner, here we have basically we need to check for the basically your fast corner because we are looking for the minimum delay in the path. So, whenever you are doing hold check or the minimum hold check, then we need to check it the FF corner, we do the simulation in the fast corner. Then the fourth point is that let us say if you have how to fix the hold violation,

how to fix the hold violation, fixing the hold violation. So, for fixing the hold violation, what you have to do? We have to increase the delay of the combinational path, increase the delay of combinational path between the flip-flop. How can I increase the delay of the combinational path? Basically, I will do buffer insertion.

Whenever you are doing max timing analysis, let us say you designed a chip, and after you manufacture the chip, your chip has a setup violation because, for some reason, we missed a path and there is a setup violation. How can you solve that manufactured chip? So, after the manufacturing, so let us say this is a special point, so I am writing in a different color. So manufactured chip has setup violation. So, how can I solve that point? Solve the setup violation. Basically, if you can see here, the clock is provided from outside the chip. So, what we can do? We can slow down the clock speed to fix the setup violation. But now I will go to the second here. This is a special case I am writing manufactured chip has hold violation. So how can I fix this chip? So I cannot insert a buffer inside a chip after the chip is fabricated. So, it is not easy to fix hold violation after the chip is manufactured because this short path or the minimum path cannot be modified after chip is fabricated.

But there are some techniques is there to what people do is that usually the hold violation happens even if you do a lot of analysis in the different paths because of some reason we will discuss in the future lectures, but there is a fix is there for hold violation. What the people do is that so people insert some buffer which is not connected to different paths. Let us say I have a chip, this is a part of a chip and this is a I have this flip flops are there and I have a short path created between the flip flops because of some reason. So what people do these days they put some kind of isolated buffer in the design. Those isolated buffer I am writing B here because I cannot write because of B are inserted inside the chip.

So what they do after the chip is manufactured if there is a short path is there they can cut this path and this cut this path they can connect to this buffer and if hold violation is bigger they can connect two buffer or one buffer depending upon the requirement. So then they can connect it. Why? How it is possible? Because all these are happening in the metal layers not in the basically transistors level. So this metal modification requires less cost compared to manufacturing the chip two times. So compared to manufacturing the chip two times this cost it cost less.

So people use to insert the buffer if there is a hold violation is there after the chip is fabricated what they do is that they change the some metal connections and one of the layers of the metal will be created while by the fab and the chip will be redesigned and the cost of the chip will not be the 2x of the actual cost of the chip. It will be slightly increased by some amount because only one metal layer will be changed, but the chip will be functional by after making that metal connections. In this lecture we discussed

about basically the timing parameters of the flip-flop, like set of time hold time clock to q delay and t-combinational delay. We discussed two timing analysis one is called maximum timing analysis one is called the minimum timing analysis and we discussed about the maximum timing analysis which is also called as a setup check. We also discussed about the minimum timing analysis, which is also called the hold check, in detail.

Thank you for your attention.