VLSI Physical Design with Timing Analysis

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Week - 02

Lecture 12

STA in Sequential Circuit with Clock Skew – I

Welcome to the course on VLSI Physical Design with Timing Analysis. In this lecture, we will discuss about Timing constraint in Sequential circuit considering clock skew. So, timing is one of the most important parameter in case of any kind of digital design and clock skew is one of the important parameter need to be considered while doing the timing analysis. In this lecture, we will cover how the clock skew will impact your timing constraints in a sequential circuit in a digital design. So, the content of this lecture includes what is clock skew. There are different types of clock skew like positive skew, negative skew, those things we will discuss in detail. Then we will discuss the max timing constraint or the setup check with clock skew. Then we will discuss about the minimum timing constraint hold check with clock skew. So, first of all, we will start with what is clock skew. So, we will discuss what is clock skew. So, this is the difference, the clock skew is the difference of the arrival time of the clock signal at the input of two consecutive flip flops in a design. So this is called your clock skew. Then what is that mean actually? Basically, let us say I have two flip flops; whatever you discussed in the last lecture, we have two flip flops: one is called your launch flip flop, one is called the capture flip-flop. Ideally, we consider in the last lecture, there is nothing, the clock is basically a same line and all the clock is arriving to the two flip flops at the same time. So, this clock is arriving at the same time.

However, in reality, it is not the same. So, what extra things are there, why it is not arriving at the same time. So here, so ideally it is the same, but in reality it is not the same, because if you can see here, we have buffers in between. So, this buffer will introduce some delay in your clock path and also there is what are the reasons of the clock skew. One is interconnect delay. This is the first parameter, and the second parameter is your buffer delay. So, that will create a delay in the arrival time between the clock in the launch flip-flop and the capture flip-flop. So, this is the reason. The second point is that the clock skew occurs due to spatial variation. What is the spatial variation? Basically, location of the flip flop in a design. So, the location of the flip flop, basically,

if you can see the spatial variation, is that let us say I have a chip is there, this is a chip, I have, let us say two flip flops are there. Ideally, they are, they should get the clock at the same time, but the location is different. So, let us say I have a clock source there; even if I want to route both to the same delay, there might be some delay, there might be some variations are there because of the location of the chip. Spatial means space or space at which your registers are located. So, this will create your clock skew.

So, we discussed about the definition of clock skew, the regions of the clock skew and the clock skew, basically what is the spatial variation, why it is lead to basically variation in the arrival time of the clock at the two consecutive flip flops. Let us say if I have a buffer here in this point and I have a buffer here, both the buffer will not offer same amount of delay after it is manufactured. Let us say I have a buffer here; let us say I have another buffer here; this buffer direction will be opposite. So, both the buffer will not give you the same delay after it is manufactured. So, that will lead to variation in the clock skew.

It is basically a static variation; there is one called this fourth point: it is a static variation. The clock skew or clock skew is basically a static variation in the path length. What is the static variation is that once the chip is manufactured, you can estimate that amount of variation and that amount of variation will remain constant throughout the, it will be estimated, it will not dynamically change. Once the chip is fabricated, you know that between the two points what is the variation in the clock skew, if you have a technique to measure it, but it will once you measure it and you know that, that will remain the constant, more or less constant, not very much. Then what is the here we are doing is that let us say I have here I have a combinational path is there, T combinational. Now this is your D pin, this is Q pin, this is D pin, this is Q pin. So now, this is your launch flip flop, flip flop 1, flip flop 2. Now, here at this point, I have basically what I am telling is that the arrival time of this one is, let us say, T1, and this is T2. So, the clock skew is basically T2 minus T1. So, we can define, so the clock skew we can define as basically capture clock arrival time minus launch clock arrival time.

So, I have a capture clock arrival time at T2, launch clock arrival time is T1. So, this is my definition of my clock skew. Now I have one more point I have to write for the clock skew which is very crucial. So, the clock skew basically does not change the clock period. But it will shift the phase of the clock. So, what is this meaning is very important point, this is very important point. Let us say I have this is clock 1 and this is clock 2. So now if I plot the clock 1 and clock 2, I have some space here. So, the clock 1 is let us say this one. The clock 2 will be shifted by some amount delta. It will be shifted by some amount delta. What it says that this time period T clock, this is T clock, let us say, and this is also T clock. And this one is also a T clock, and this is also a T clock. So that is why this point is that the sixth point comes. The skew is constant, the clock skew is constant from cycle to cycle. The clock skew is constant irrespective of the number of the

cycle. So this is the most important point and which is used for timing analysis. Now we will go into the all the definitions are clear. Now types of clock skew. There are two types of clock skew. So, there are two types of clock skew, one is called positive skew. Let us discuss the positive skew first. Then we will discuss the negative skew. So, if you can see here in case of positive skew, I have a flip-flop.

This is my flip-flop. This is another flip-flop. Some combinational delay. There is some combinational delay. So, I have basically clock. This is clock. So, if this is a clock, this is a clock, this is a clock. This is d pin, d pin, d pin, q pin, q pin, q. So, here if you can see your clock and the data is moving in the same direction. And the clock signal, the clock in the data signals are moving in the same direction. So, if you can see here a clock at this point and at this point, let us say this is point A and point B is shifted. So, if you can plot only point A and B, and B will be shifted by some amount. Like this. So, which is your capture clock? Your B clock is your capture clock. So, your basically skew definition is capture clock arrival time minus launch clock arrival time. So here this is t 1 and this is t 2.

So t 1, t 2 minus t 1 because t 2 is larger, so this skew is positive. That is why it is called it is positive skew. If your data and clock is moving in the same direction, then your skew is positive. Now we will discuss the negative skew. Second point, second type is a negative skew. So here if you can see, if I have two flip-flops and your clock is moving in this direction, I have a buffer sitting in between. This is your clock. This is your D pin, this is your Q pin. I have some combinational delay. This is D pin, this is Q pin. Like this. So let us say if your data is moving in left to right, your clock is moving from right to left. Your data and clock is moving in the opposite data signal, data and clock signal is moving in opposite direction. So, in this case how my skew will look like. So now if I draw, let us say this is A pin and B pin. So let us say this A will come, which will come early, B will come early. I will plot the B first. Related to that one I will plot the A. So here, if you can see, this is, let us say, the clock signal. This is my clock signal, and my A is coming after the rising edge because there is a buffer delay is there and some interconnect delay is also there.

So, it will come after some time. It will come like this. So here if you can see, your skew definition, same skew definition you apply here. Capture clock arrival time minus launch clock arrival time. So here capture clock arrival time which is coming first, let us say this is T1 or whatever you take this time is let us say T1, and this time is T2. So, the capture is T1 and launch is T2 and this skew is negative. So now we will discuss how to do max timing analysis considering skew. So first of all we will see that delta is positive, that skew is positive. Skew is basically denoted by delta here. So, we discussed earlier I will first write the waveforms then we will derive the equations. So first of all, I will draw the waveforms then we will derive the equations. Let us say I have basically one flip-flop, which is called a launch flip-flop, which is launching the data. I have a capture

which is capturing the data. So, this is clock. I am drawing multiple times but this combinational delay, this is your D pin, this is your Q, this is D, this is Q.

So, now this is clock, this is clock. This is clock 1, this is clock 1, this is clock 2. Now I will do the analysis. So, I have two clock, clock 1 and clock 2. How they are positioned and how they are going to the flip-flops we will discuss. The flip-flop 1 and flip-flop 2. Now I have basically let us say I will draw the clock 1. Now I have a positive skew, the clock 2 will come after this clock 1 because of delay of the buffer and the interconnect. So this is let us say the skew. Now and as I told you the time period will not be modified, it will just shifted by some amount that is the amount of phase shift in the clock. So now this is your delta, this is your delta, basically that is your clock skew which is positive. Now how many edges I have? I have edge 1, this is edge 2, this is edge 3, now this is edge 4. Now your flip-flop 1 will sample at edge 1, the flip-flop 1 will sample at edge 1, and flip-flop 2 will sample at edge 4. The flip-flop 1 samples the data at edge 1, flip-flop 2 samples the data at edge 4. So, I can write here in different colour, this is for sampling the data flip-flop 1 and this is basically the point it will sample by the flip-flop 2. So, now earlier my time period was this much, earlier my time period was t clock, okay, my time period is t clock. Now my available time is increased by t clock plus delta, okay. So available time is basically t clock plus delta. So, when there is no skew, the constraint is that there are two cases, okay. I will write down two cases. So I have basically I can write it here itself, I have some space here, case 1 without skew, okay. What is the constraint equation? Basically, t clock, so I have two cases I will write here, without skew basically is one case, then I have case 2 with skew, okay. So now, basically without skew constraint is basically your

$$t_{cq}^{\max} + t_{comb}^{\max} + t_{setup} \leq T_{clk}$$

So, when there is no skew, when there is skew is there how my equation will change? My equation will change instead of t clock, now t clock plus delta, okay. Now I have a equation

$$t_{cq}^{\max} + t_{comb}^{\max} + t_{setup} \leq (T_{clk} + \delta)$$

So, we can write the same equation in other form by t clock to q, it is better to write it here,

$$(t_{cq}^{\max} + t_{comb}^{\max} + t_{setup} - \delta) \leq T_{clk}$$

So, what is, this is my equation after considering the clock skew. My total time period is now basically is means what will happen is that my total time period earlier is reduced by delta, okay. If your time period will reduce what will happen to your speed? So here, if your time period t clock is reduced, what will happen to the speed? Your speed of the

clock, f clock will increase. So what is the final conclusion out of it? So what will happen is that your clock period is reduced, so the clock period will be reduced by how much amount? By delta which is your amount of the clock skew, basically your total time period available to evaluate considering the clock skew will be less. How much it will be less? It will be less by delta because if you see here it is a negative factor is there in the left hand side.

Earlier it is t clock, okay, now it is reduced by delta. So if it is reduced by delta my clock period is reduced, okay, clock period is reduced means your clock frequency will increase. So what is the summary of this discussion? Your summary of the discussion is that the positive skew improves the speed of the design. So this is the one of the advantages of this positive skew. So this is the equation basically for considering clock skew. So, if your positive skew improves the speed of the design it is good for us, but nothing comes free. There will be some penalty on this one which we will discuss in the next slide. So now we will discuss about the minimum timing analysis. Now we will discuss the minimum timing analysis considering positive skew. So, we are considering that minimum timing analysis basically considering positive skew.

So, what is the scenario here is that I have two flip flops again I am drawing the same two flip flops because without drawing it will be not very clear. So, the same two flip-flops, okay, so they have two clocks. I am just considering the clocks only and you have some minimum delays there, okay. Here you have t com minimum, okay. This is d, this is q, this is d, this is q, okay. So now basically what is happening is that here you have a if you do not have clock skew, okay if you do not have clock skew case 1, okay your without clock skew, okay your basically in this case your hold time the hold time is basically t hold, okay. So t hold of the flip flop 2, flip flop 1 and this is flip flop 2. But in case 2 is basically the case 2 when I have with clock skew, with clock skew so what happens I have two edges this is clock 1, this is clock 2. So, if you can see here my clock 1 is like this, okay.

So, this is clock 1. My clock 2 will come after the rising edge of the clock 1 because there is a delay of the buffer and the interconnect, okay. Now this is my clock 2, okay. So, if you can see here, this is my skew, this is my skew delta, okay. Whenever I am considering the hold t hold, I am considering the hold of the flip flop 2. Now I have a hold around flip-flop 2. This clock 2 is going to flip flop 2. How much it is basically? It is the t hold. This is your t hold. So now, with clock skew, my hold will be how much? Now from here-to-here total thing will be t hold. The hold time now, the hold time of the flip flop 2, basically flip flop 2 here also, flip flop 2 is now earlier it is t hold, now it is increased by delta.

That is the amount of skew. That is increased by delta, okay. So, it is clear because we are checking the same clock edge for the hold, but in the case of setup, we are checking

the two clock edges. But if you are seeing here, we are checking the; basically, if I can draw the edges, this is the first edge, this is the second edge, this one is the second edge, this is the third edge, then this is the fourth edge. But for basically hold violation I need to check the same edge. Same edge here is the first edge of the clock 1 and the second edge of the clock 2. For hold check, we need to consider clock 1 is 1, clock 2 is 2 in this timing diagram. So now my hold time is flip flop 2 is t hold plus delta. Now if I have a hold constraint, what is the hold constraint without skew? I can write it here itself. My t hold, so here I can write your

$$t_{hold} \leq t_{cq}^{\min} + t_{comb}^{\min}$$

This is small, I am putting it in a box to isolate that from the rest of the text. This is my t hold condition without skew. Now, I have to do t hold condition with skew. So now my t hold is increased by delta.

$$(t_{hold} + \delta) \leq t_{cq}^{\min} + t_{comb}^{\min}$$

What is the problem is that my hold constraint is increased by delta. My hold constraint is increased by delta. I will put it into a box. This is a very important conclusion that positive skew degrades your hold constraint. What is this conclusion out of this equation is that conclusion positive skew degrades your hold constraint, hold requirement. So, this is the conclusion. So, nothing comes free in this world. So positive skew improves the speed of your design, that is a positive point, and the negative point is that positive skew basically degrades the hold requirement and hold requirement is very dangerous.

If your chip has a hold requirement it is very difficult to fix because you cannot insert a buffer without a connection. If it is not there in the design time you cannot insert a buffer after the chip is manufactured. But if your setup is violated you can reduce the clock speed. So, this is the minimum timing constraint considering the positive skew. So, in this lecture, we discussed about what is skew, what are the different types of skew, then we discussed about maximum and minimum timing analysis considering positive skew.

Thank you for your attention. Thank you.