VLSI Physical Design with Timing Analysis

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Week 03

Lecture 17

STA for Combinational Circuits – I

Welcome to the course on VLSI Physical Design with Timing Analysis. In this lecture, we will discuss about static timing analysis for combinational circuits. So, the content of this lecture includes different types of path we have in a combinational circuit. Then we discuss about arrival time and required time. Then we will discuss about how basically output arrival time we can find it for a inverting gate and a non-inverting gate and we will take some example to find out how the things are happening, how output arrival time we can find it out. Similarly, also we can also discuss about how to find the input required time for non-inverting and inverting gates. So, there are basically for a combinational circuit, we have different, it is a lots of components are there. We can have different types of paths, so types of path in a combinational circuits. One is basically called your critical path, or which is also called the longest path in a design or in this combinational circuit, so which is used for your setup check actually. What we discussed already.

Then the second type of paths are called short path or minimum path in the minimum data path in the circuit or design in a design or circuit same thing. So, which is used for hold check, this is used for hold check. We have discussed with several examples in earlier lectures. Then the third type of path is called the false path. The false path is a path which will not be activated in any condition, but if you consider that in a timing analysis, it will look like a critical path. So, in certain input condition that path will never be activated or never be excited or activated during any of the input condition, but if you do not ignore that path, it will act as a critical path and what it will do? It will falsely basically tell that my critical path delays so long, but it is never be activated in any time. So, these three types of paths are there in combinational paths. There are several other paths are there which is non-critical. Non-critical means that it is not a critical path, or it is not a short path. So, those are called non-critical paths. So, basically then we discuss about the arrival time. So, what is arrival time? Arrival time is actual rise and fall time at different nodes due to the rise and fall delay of the logic gates. So, basically this arrival time is the actual

rise and fall time at different nodes due to the rise and fall delay of the logic gates and the required time, what is this required time? So, basically this rise and fall arrival time, the rise and fall arrival time required or needed due to the time constraint specified by the circuit design. So, this is two things we will consider in today's class actually arrival time and required time. So, now first we will discuss about the inverting type of gates.

We will discuss about the inverting type of gate. So, let us say first we will discuss about one input gates like inverter. This is easy to understand for one input, then you can go to the multiple input gates. So, let us say we discuss about the inverter. I have a inverter, this is input, this is output. So, if this is the input and this is the output, now I will plot their time. Let us say this t equals to 0. So, now I am this is input, this is input. If this is the input and I have a output, output will look like it will be delay by some amount, it will be delay by some amount. Correct. So, now let us say this is my arrival time or the input. Let us say this is t1 and what is the delay from here to here? This delay is your fall delay, t fall. This is your t fall. Similarly, let us say this is your time t2. So, this is t2 is your fall arrival time, input fall arrival time and what is this delay from 50 percent to this point? It is your, this one is your t rise. So then if I have this much of information, then what I want to find out output arrival time. So, I have to find out what is the output arrival time rise I want to do. Output rise arrival time or output arrival time rise. So, in that case, so I should take t2 plus t rise. What is t2 actually? It is the input fall arrival time plus t rise. So, output arrival time fall is basically t1 plus t fall. What is my t1? Basically, if you can see t1, it is rising. So, basically, this is my input rise arrival time plus t fall. So, this is the actual summary of what we can say. So, these are the output arrival time. If I know input arrival time and t rise and t fall, I can find the output arrival time at the output. So, this is for one input gate. Let us say I have multiple input gate. Let us say I have multiple input gate. So, what will happen? I have let us say 2 input NAND gate is there.

So, I have A, B, then C. So let us say I will use ta 1 rise, ta 2 fall, ta, ta, tb rise, tb fall. So, this is the input arrival time. Now I have t rise and t fall. So, at the input, I have 2 arrival time for rise. So let us say I have just I am considering for the rise. Let us say my input is changing. Let us say this is my a signal. So, this is my ta rise, this is b signal, this is my ta, tb rise. So, I have 2 arrival times. Which one I should take for calculating the output arrival time at this point? So, we have to consider the worst case. Worst case means out of both which is giving you the maximum delay. Which will give you the maximum delay? tb rise will give you the maximum delay. So basically, your output arrival time, your output arrival time rise or fall whatever you can say that will be the max of. So, in this case what I have to take? This is the max of ta rise, tb rise. And if this is the case then we have to take if you can say ta, tb rise will be taken here. So that one will be taken as the reference for the input side. So max of input fall arrival time plus t rise, t rise your rise delay, rise delay of the gate. So similarly, I have output arrival time fall is basically max of input rise arrival time plus t fall. So, this is my actual equations.

So, I will put this equation in the box. So, this is for the multiple input gates. So, if I know the input arrival time and t rise and t fall how can I find the output arrival time rise, output arrival time fall? So, this is for basically a single gate like inverter. So, these three formulas are useful for inverting type of gates. So now take an example here for inverting type of gates. Let us say this is a inverting. So, it is two inputs. So let us say a and b. So, the inputs are 3 by 4, and your B is 5 by 3 and rise delay is 2 by 3. Then I have to find out the output arrival time at this point. Let us say your O. So how can I find the output arrival time? So, I need to do the output arrival time rise. Output arrival time rise equals to the input max of the input fall arrival time. What is the fall arrival time here? Output 4, 3 these two. So out of which is max that should be taken. Then you have to add the rise time. What is the rise time? 2. So this is 4 plus 2 it is 6. So, output arrival time rise is 6. Output arrival time fall is max of so max of rise arrival time. Rise is 3, 5. So actually this 3 corresponds to this 3 and this 3 corresponds to this 3 and this 5 corresponds to this 5. Correct. Now I have to add the fall delay. Fall delay is 3 here. So now this is 5 plus 3 is 8. So, your output arrival time will be 6 by 8. So, this is an example of inverting type of gates. Now I will go for the non-inverting type of gates. So, in this case I have two types of gates are there single input. So there also I should write not one input this is should be single input actually. So, if I have single input gate let us say buffer, I have single input single output. How I can find the output arrival time? So let us say this time axis I have input I have output. So let us say my this is the input this is input this is my output. So now I have let us say this is my t1. This is your t1, and this will be your t rise. Basically, this is if I consider this one is my t2 and this delay is basically t4. So now if I write my output arrival time rise output arrival time rise so that will depend upon my t1 plus t rise. What is this t1 actually? t1 is basically input rise arrival time plus rise delay. So, input rise arrival time so output rise arrival time output same thing output rise arrival time is same as this in words. So, this is a very important conclusion. Similarly, I can derive the output arrival time fall is basically t2 you look into the t2 here this t2.

So t2 plus t fall. So, this is my output arrival time. So, this is my output arrival time rise. This is my output arrival time fall. So now if you have this so basically if I have output fall arrival time equal to input fall arrival time plus fall delay. So, this is for single input gates. So, the second one is the multiple input gate. So multiple input gates what will be the conditions? It is same as the way I did the for the inverting type of gate. So, I am writing the formula directly. So, I have output arrival time rise equals to max of input rise arrival time max of input rise arrival time plus rise delay. Only thing I have added if I have multiple input take the max of the all the input arrival time max. So here it was only one input that is why I am taking that input rise arrival time but here I have multiple arrival time. So, I have to take the max of that because I am doing for the worst-case delay calculation. I am doing it for the critical path calculation. So, all these analysis whatever I am trying to do is for the critical path analysis, the longest path in the design. Input arrival time fall is basically max of input fall arrival time plus fall delay.

So, this is basically this is my equations. So, I am putting this one in a box because this is very important conclusion what will be used for my critical path finding. So, this is for multiple input this is single input. Now if I take an example for the multiple input. So let us say I have a multiple input non-inverting type of gate multiple input non-inverting type of gate. So let us say the a b is the input and the arrival time is 3 by 4 here this is a 5 by 3 and rise delay is 2 fall delay is 4 then I need to find the arrival time at the output node. So the output arrival time output rise arrival time is equals to max of input rise arrival time. What is the input rise arrival times are there? So basically, if you can say 3 and 5. So this 3 5 I have to take 3, 5 plus rise delay rise delay is 2. So here it will be 5 plus 2 is 7. So, output arise rise fall arrival time at node O actually this is output node is basically max of 4, 3 the 4 corresponds to basically this 4 and this 4 corresponds to this 4 and this 3 corresponds to this 3. So, this is your fall arrival time then I have to take the fall delay. So, this is basically 4 plus 4 is 8. So, the output arrival time is 7 by 8. So now I will discuss about the input arrival time. So, input arrival time I will discuss about the input how to find the input arrival time what is given to me input arrival time.

So, whenever I am finding the input arrival time what are the things are given to me. So, we will discuss about the input arrival time. So, whenever you are finding the input arrival time so what is given to us is that the given parameters are output arrival time both rise and fall. So, whenever I am finding input arrival time, I have to do for both rise and fall. Similarly, what are the things I have given I have given with output arrival time rise and fall this is one parameter and second parameter is given to me rise delay and fall delay of the gate rise delay and fall delay of the gate that is given to me.

Here we have two types of gates one is inverting first I will do it for the inverting type type gate inverting type gates. So, for inverting type gates I have basically single input one case is single input first it is easy to explain with the single input then I can go for multiple input. So let us say I am taking the inverter. This is my input this is my output. If I know let us draw the waveform then I can find it out let us say this t equals to zero here this is input waveform and this is output waveform.

Let us say I have a pulse giving to the same inverter. Now output will come out after some delay let us say this is a delay. So, I have this is my input arrival time and this is my output arrival time, and this is my t fall. So, this is my basically input fall arrival time this is my output rise arrival time and this delay is your t rise. So now what is given to me this let us say the t1 is given to me and t2 is given to me because this is corresponds to my output t1 and t2 and I know the rise and fall delay. So, from this I can find it out, so the input rise arrival time is basically rise arrival time is basically t1 minus t fall. So, this is same as output fall arrival time minus fall delay. So, this is my equation input rise arrival time. If I know this output fall arrival time and fall delay, I can find out the input rise arrival time. Similarly, so this t1 basically this t1 is corresponds to this t1 and this t fall is corresponds to this t fall and this is my input rise arrival time. So this is one of the equations. Similarly,

I can do it for input fall arrival time. So, the input fall arrival time is basically t2 minus t rise. So, this is output rise arrival time minus rise delay. So now this is basically your second equation input fall arrival time. So, I will put these two equation in the box because this is useful for critical path finding and here if you can see your t2 here this t2 corresponds to this t2 and the t rise here okay this t rise corresponds to this t rise correct.

So, this is the for the inverting type of gates. So here we are discussing whatever the single input and single output. But here we are discussing the second case when you we have multiple fan out gates okay multiple fanout connected to the output node output pin, pin of the gates okay. So, if a multiple signal is connected to the output how can I find the input arrival time. So, in that case what will happen I have to take the mean of all the output arrival time. So let us say so here the formula will be input rise arrival time okay is equals to minimum of output fall arrival time minus fall delay okay. Basically, input fall arrival time is basically minimum of output rise arrival time minus rise delay okay. So, these are the two equations for the multiple fan out gate.

I will take an example here okay it will be more clear from there. So let us say I have a inverting type of gate which is having two inputs a and b, I need to find the arrival time at the input a and b and the see the rise and fall delay of the gate is given 2 by 1 then it is driven by two paths actually two fan outs are there or this output is connected to the two gates.

So, the arrival time of this path is 3 by 4 and this path is 5 by 3. How can I find the input arrival time? So, the input rise arrival time at both the nodes a or b does not matter here okay a or b does not matter here. So here it will be min of output fall arrival time okay. So, output fall arrival time is 4, 3 okay minus fall delay, fall delay is 1 here, fall delay is 1 here. So, this will be min is 3 minus 1 is 2. Basically, input fall arrival time a or b node both nodes is min of what is the min of this will be basically rise arrival time. Rise is basically the 3 this 3 and 5, 3, 5. So output arrival time there are 3 is there, 5 is there minus then the rise delay. Rise delay is 2 here so the min of this is 3 minus 2 is 1 okay. So, the input rise and fall arrival time at a and b is 2 by 1 here also 2 by 1. So, this is the time input arrival time for non-inverting gates okay non-inverting gates. So, in case you have basically the case 1 is single input and single output, single input and single output okay. This is a case of a buffer actually how I can find the input arrival time. So basically, if I draw the waveforms first this is input, this is output and let us say this is t equals to 0 here, this is my waveform here. Now this is my t1 okay, this is my t2, this is the output arrival time. This is the t1 is the output rise arrival time, t2 is the output fall arrival time and this is my input arrival time, and this delay is basically t rise, and this delay is basically from here to here is basically t fall okay. So now I need to find it out the input arrival time. So, the input rise arrival time is basically t1 minus t rise. So, this t1 is output rise arrival time minus rise delay okay. So, this t1 corresponds to this t1 here. So similarly input fall arrival time is basically t2 minus t fall. So t2 is basically output fall arrival time minus fall delay

okay. So, this is for the single input and single output gates. So, these are the formula, these two are important formula for the fall arrival time. This is input rise arrival time correct. So, if I have put this one in a box, this I will put in a box.

Now I have the output node is driven by multiple paths actually okay. So, the second case basically case 2 multiple fanout. So, what is the case is that you have multiple fanout is there, then you have to here just you have to take the mean of that. So, if you have multiple fanout input rise arrival time is basically minimum of output rise arrival time minus rise delay okay. Now input fall arrival time is basically minimum of output fall arrival time minus fall delay. So, these are for the multiple fan out gates. So let us take an example, so multiple fan outs actually. Basically, let us say I have one example here. So here let us say I have two inputs. This is a basically buffer, so the bubble is not there okay. non-inverting gate basically bubble is not there. I have two inputs a and b then output c. c has fan outs, so let us say this is one fan out and this is another fan out. So, this is 3 by 4, and this is 5 by 3 and the delay is 2 by 1 correct. So now I need to find out the input arrival time at a and b. This is given to me, and I have to find the input arrival time a and b. So, the input rise arrival time is basically the minimum of input rise arrival time minus rise delay okay. So here if I go min of, so output rise arrival time is 3, 5. So this 3 corresponds to this 3, this 5 corresponds to this 5 minus rise delay, rise delay is 2.

So, this will be basically 3 minus 2, this is 1 okay. Input rise arrival time is 1. Similarly, you have input fall arrival time. It is basically minimum of output fall arrival time minus fall delay. So here if you can see I have basically two paths are there, fall is basically 4, 3. So this corresponds to this 4, this 3 corresponds to this 3 here minus fall delay is 1.

So, this will be basically 3 minus 1 is 2. So, input arrival time rise and fall together is 1 by 2. So, the input rise and fall arrival time together is basically 1 by 2. So here it is applicable for both the inputs 1 by 2. So, this is the input arrival time.

So, in this lecture we discussed about different types of path like critical path, short path and false path. Then we discussed about how to find the output arrival time if you have input arrival time and rise and fall delay are given. So, we discussed for the inverting type of gate and non-inverting type of gates. Similarly, we will find we discuss about how to find the input arrival time if my output arrival time and rise and fall delay is given to us. So, we discussed some examples and how it can be used to find the input and output arrival times. This is very useful for static timing analysis.

Thank you for your attention.