VLSI Physical Design with Timing Analysis

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Week 05

Lecture 28

Pin Assignment and Power - Ground Routing

Welcome to the course on VLSI Physical Design with Timing Analysis. In this lecture, we will discuss about pin assignment and power and ground routing. So, the content of this lecture includes pin assignment and power and ground routing. In case of pin assignment, we will discuss about how we can formulate the problem and there are two approaches to solve the pin assignment problem. So, one method is concentric circle approach and the second one is called a topological pin assignment method. Then we will go to the power and ground routing.

So, here we will discuss about the design of a power ground distribution network. Then we will discuss about two different types of approach. We will discuss about the planner routing for full custom design style and mesh routing for the semi-custom or standard cell based design style. So, basically in case of a chip planning, there are three steps are there.

One is called the floor planning and the second one is called pin assignment and third one is called the power and ground routing. So, in this case, we will discuss about the pin assignment first. So, the problem formulation for the pin assignment includes basically during the pin assignments, all the nets are assigned to unique pin location to optimize the overall design performance. So, what are the design performance actually? So, here we want maximum routability and minimizing the electrical parasitics. So, whenever we assign a pin and find out its location inside a chip, we always look for how we can maximum routability and minimize the electrical parasitics of the interconnects.

So, there are two types of pin assignment, one is called external pin assignment and the second one is called internal pin assignment. First of all, we will discuss about the external pin assignment. In case of external pin assignment, we connect each incoming and outgoing signal to a unique IO Pin. So, whenever we do this kind of assignment, our goal is to minimize the wire length. This is the first goal.

Then the second goal is minimize the electrical parasitic effects and the third goal is to reduce the signal integrity and coupling between the wires. So, these are the three basically objective we need to satisfy when you are doing the external pin assignment. So, let us take an example of a pin assignment here. Here you can see there are 90 pins are there here and there are 90 pins is there in the chip. So, we need to connect them.

So, this is before the pin assignment, this is after pin assignment. So, what is happening here is that after pin assignment, so all the pins will be connected to unique pin. So, one net will be connected to one pin. So, you have 90 pins here, here also 90 pins. So, this is happening in a PCB printed circuit board.

So, it can also be done inside a chip also. This external pin assignment can be done inside a chip also. So, whenever you have multiple blocks, how we can connect those blocks to the IO of the chip. So, here each pin pair is connected by a wire or a route. So, pin pair means this is one and this is one.

So, this is called a one pin pair. Pin pair is connected by one route. So, one route means this is one wire, route means wire. So, now we will discuss into the internal pin assignment. So, in case of internal pin assignment, our aim is to reduce or minimize the congestion interconnect length between the cells.

So, what are the cells? Cells are maybe the standard cells, maybe the blocks between them, connection between the blocks. So, basically here we are doing inside lower level modules. External pin assignments happens in the top level modules. So, in case of internal pin assignment, we are doing in the cell level or standard cell level. So, here you used to connect the cells, pins that are functionally or electrically equivalent. So, whenever we are connecting these pins, we connect them based on a functional equivalent pins and electrical equivalent pins. So, we will discuss about what is functional equivalent pins and what is electrical equivalent pins. So, two pins are functionally equivalent. When you swap them or exchange them, that does not affect the design's functionality. When for example, here I have this is one pin and this is another pin.

So, if I exchange both of them, then the functionality of the design will not be changed. So, that is called functional equivalent pin, but they are not electrically equivalent. Means they are two different nets. They are not electrically equivalent. Functional equivalent does not mean that they are electrically equivalent.

Electrically equivalent means that they are basically connected in a same metal. So, they are called equipotential nets. So, equipotential means potential at this point, let us say this point is A and potential at this point B is same. They are the same net. So, this is called electrically equivalent pins.

So, this is called electrically equivalent pins. So, these two definitions are very useful and whenever you are doing internal pin assignment. Let us take an example. So, here this is before pin assignment, this is after pin assignment. So, this is a pin assignment is internal here.

So, here if you can see here, there are two routes are here. This is one route, this is another route. But if you can see this length of the wire is longer. As these two nets are functionally equivalent, we can route them like this. So, these two nets can be routed with a shorter length of the interconnect or a route.

So, this is a better internal pin assignment. So, let us take the example of electrically equivalent net. So, if you can see here from here to here, this connection is there. From here, this point to this point, there is a connection is there. The length of the interconnect is very large. But this pin A, this is pin A and this pin B. These two are electrically equivalent. If they are electrically equivalent, I can bring this connection to here. So, if you can see here, the connection is now come to here. Similarly, this movement of from A to B is called electrically equivalent pins. And movement of from here to here, this exchange is basically because of the functional equivalent pins. So, from here to here, that is called functional equivalent pins. So, after passing through this electrical equivalent and functional equivalent things, we have a very reduced interconnects after the internal pin assignment. Now we will discuss about the pin assignment using concentric circles. So, this concentric circle is very interesting concept of pin assignment.

So, what is happening here is that we need to establish connection between a block and all its related pins. So, we need to establish a connection between the blocks and all its related pins. So, what is the mean in is that minimize the net crossing, number of net crossings should be as minimum as possible. So, we employed two concentric circles. One is called inner circle and the second one is called the outer circle.

The inner circle is for the pin of the block which need to be connected to the outer circle. So, we have outer circle is for the pins of the other block. We have two blocks is there. One block is inside the inner circle, one block is outside the outer circle. So, assume all the outer pins are fixed location because the outer pin is already fixed.

So, how we can do the pin assignment here? So, I have a set of pins. So, that is called black and set up the pin on the chip which is red which the block pins must connect. This black pin should be connected to the red pins actually. So, what is this black pin? So, these are the black pins and these are the red pins. So, this black pins and this should be connected to the red pins. So, our main task is to do the pin assignment using the concentric circle such that each pin on the block is connected exactly one pin on the chip and vice versa. So, our aim is to use the concentric circle method to connect the pins in the inner circle to the pins on the chip. So, there are few steps are there. One step is to

determine the circles. So, there are two circles are drawn such that all the pins belong to the block or the blacks are outside the inner circle, but within the outer circle.

So, this is the inner circle. So, all the black dots should be outside the inner circle, but inside the outer circle. So, this is inner circle and this is outer circle. So, outer circle will be drawn such a way that all the chip pins or the red dots or red pins will be outside the outer circle. Now we need to determine the points actually. So, what we need to do since the center of the outer circle and the center of the inner circle is the same, then you can draw a line from the red pins to the center and also we will draw the lines from the black dot or the black pins to the center.

So, this is basically find out some pins on the circle. So, these are the points after the drawing the lines. So, these points and these points are important for us. So, now after we find out those points, then we need to move each outer points to its projection point on the outer circle. Move each outer red points to its projection on the outer circle.

Similarly, we move each inner black points to its projection on the inner circle. So, these are the points now we forget about now the pins. Now we will look into the dots on the inner circle and dots on the outer circle. Now these two need to be connected. So, these two is basically done using a initial mapping. So, the initial mapping is an assignment from each outer pin to a corresponding inner pin. So, choose a starting point and assign it arbitrarily. So, let us we will take one pin from the inner circle and one pin from the outer circle and connect them either we can go clockwise or counterclockwise after doing the all the initial mapping, but this initial mapping is not the best solution. This is the first solution of our pin assignment, but we need a better or best solution. So, we can change this pin assignment in a different order till I will get a better solution.

So, what we need to do is we repeat the same procedure based on one criteria called shortest Euclidean distance. So, the Euclidean distance should be as minimum as possible. So, after we do the process repeatedly, then this is the one of the mapping and finally we will get the best mapping. So, this best mapping will be connected with the actual pins inside the block. This is the block pins and these are the chip pins. So, these two will be connected with each other. Now we discuss about the concentric circle approach, then we will go into the topological pin assignment. So, what is this topological pin assignment is that it has certain advantages over the concentric circle based method because it considers external block positions and multi pin nets. So, it enables pin assignment when external pins are behind each blocks or the obstacles. It can also enable pin assignment when external pins are behind other blocks or obstacles.

How it is possible? We will see in the example. So, let us take two blocks, one block is your main component M. So, this is your main component then I have an external block B is there. So, how I can do a pin assignment here? So, I need to draw a line from the

main block M passing through B and I need to connect to a farthest point. So, this is my farthest point from the block M. So, this black dot is the farthest point from the block M. So, you have this midline M to B is drawn from M through the centre of B. So, it is going from M to the centre of B. So, D is the farthest point. So, then it will intersect the B block. Now what we will do? We will draw a basically perpendicular line to that line.

So, this line will draw which is perpendicular to the previous midpoint line. So, this is your midpoint line and this is my perpendicular to the midpoint line. So, then we have multiple points are available on the perpendicular line. So, this is the left side of the midpoint line left side and this is the right side of the midpoint line.

So, then we will assign all the pins. Now we will assign all the pins in the right side of the midpoint line to the points here. These are the points. So, these are the points. So, these are for the right side.

This is for the right side pins. Now after you we have pins in the this line, then that will connect to the outer circle of the M. The pins are then projected onto the outer circle of M. Now we can connect them using the previous concentric circle method. Now this is a separate example where we can have multiple blocks pins can be connected. How can we connect multiple blocks pin using the topological pin assignment? This is a separate example. So, I have two blocks. Here I have a block A and block B. So, this block A and block B need to be connected with a main component M. So, this main component M is there. So, what I need to do now, I have a line going through the midpoint of the each of the block. So, if I can there are two lines are there. This is let us say this is the line 1. This one is line 1 and this one is the line 2. So, the line 1 is passing through the midpoint of block A. Line 1 is passing through the midpoint of the block A. You can see this is the midpoint of the block A and the line 2 is passing to the midpoint of the block B.

So, now I have D1, D2 and D3. So, these are very useful things because this will help me to map the pins to that line actually. So, now what I have to do? Now I have D1. D1 is the farthest point on block M to A. So, and the D2 is this point actually which is the closure point on M to B on block E. So, now I have D3. D3 is the farthest point on line M to B on block B. So, these three parameters are very useful. So, if M has a concentric circle method, then there will be line drawn between M and the other blocks. So, how this line will be mapped with the pins of the block A and block B? So, here the method. So, if you can see here the D1 to D2, so this distance, so the D1 to D2 will be having these pins 1, 2, 3, this 1, 2 and 3 of block A.

D1 should have 1, 2, 3 of the pins of the block A. Now, we have basically other pins of block A. Other pins of the block A will go to D2 to this distance actually D2 to D1. So, if I go here, I have this 1, let us say this is 4, 5, 6, 7, 8 also that will go here of the projected line. So, these are the pins in the projected lines and D3 to D3 that will contain the pins of

the block B only. Now we can apply the concentric circle approach to connect this pin to the main component M.

The topological pin assignment method is very useful for assigning the pins while we have multiple blocks which need to be connected to the main component. So, now we discuss about the power and ground routing. So, the power and ground routing is one of the most important part of our chip design and VLSI physical design flow. The reason is that it governs the overall performance of our chip. The chip planning determines the layout of the power distribution network. It also basically includes the placement of the supply IO and the bumps. So, it depends upon the packaging type. There are multiple ways of packaging. You can have basically pad inside the chip for doing the wire bond packaging or you can do a QFN or you can do flip chip packaging. So, depending upon that how we can do the IO placement that is also included in case of power and ground routing.

So, there are other factors which is very much important which is basically placement of the blocks in a high active region. So, our main aim is to reduce the IR drop. So, it is possible if we place the IO's close to the high activity region such that the IR drop can be minimized. So, what are the goals basically of this power and ground routing? It is basically it is a highly iterative process. It is used early simulation of the major power distribution of the components and it also includes the quantification of chip power.

So, early simulation of the major power distribution component is essential to be given as an input to our power and ground routing algorithm and also how much your power budget that needs to be provided. So, there are two things one is called the total chip power and the second one is the maximum power density. So, the total chip power is the overall power consumption of the chip. The maximum power density is related to the in particular location of the chip what is the power consumption. Let us say this is the total chip area, this is the total chip boundary and here this is the area where we have very much high activity is going on.

So, the total power at this area divided by the divided by the area will give me the power density. The power density is important because at one part of the chip if it is consuming high amount of the power then it will leads to hot spot. If your power dissipation at a particular region is higher then that leads to hot spot. So, we need to spread out the power such a way that there should not be a hot spot inside the chip. So, we need to take those total chip power and maximum power density into account while doing the power and ground routing.

We also need to check the chip level power fluctuation because of different activity at different regions of the chip. Let us say I have one of the region is off and other region is on because of dynamic voltage and voltage scaling. Let us say this is the power line and

if I do a switch off and switch on this is block A and the block 1 and block 2 if I switch off for block 1 then there will be fluctuation in the power at block 2. So, these things need to be taken into account while doing the power and ground routing.

So, also the similarly applicable for clock gating. So, whenever you are doing the clock gating there is also a fluctuation in the power and ground lines. So, there is a specification need to be given as an input to your power and ground routing algorithm. So, one is the maximum power consumption, average power consumption and multi cycle fluctuation all these need to be provided. So, if you can look into this diagram it has lot of information. So, these are the IO PINs, these are the IO PINs, this G stands for the ground pin, ground IO and the V stands for the VDD IO.

So, these are the basic things. Then each of the block has two rings. So, let us say this is block 1, this is block 2, each of the block has two rings. This block has two rings. One is VDD, one is ground. Now the chip has two rings. So, this is VDD let us say and the other one is the ground. So, now, so, ring of the chip boundary this one should be connected to the ring of the each of the block and that ring also need to be connected with the IO VDD and IO Ground. So, and there is a connection between the block is called the trunks. Trunks connect the rings to each other or to the top-level power ring. So, now we will go into the how we can design the power and ground distribution network.

So, each cell must have a power that is VDD and ground connections. So, these connections of the supply nets are large and it should span through the entire chip. It should span through the entire chip and remember that the power distribution network basically is routed first before your signal route because it has more priority compared to the signal routing. Signal can go has multiple way you can route, but the power has a dedicated network that should be placed first or place routed first before you go for the signal routing. There is no compromise in the power and ground distribution network.

So, we first fix our power and ground network before going to the signal routing. So, basically the power and ground nets, so, the has should have the following characteristics actually. So, whenever we are designing our power and ground nets, we should have dedicated metal lines for the power and ground such that there should not be any congestion because of the signal routing. And we should use the thick metals because the thick metals has low resistance. So, and this is the that is this thick metals are used from the top level layers.

Let us say I have a metal 8. So, the metal let us say I have a process called which has till metal 8. So, the metal 8 and metal 7 is a is used for your VDD and ground. So, if the top level metal is the metal 8, top level metal is metal 8. Now we should have sufficient vias. If you do not have sufficient via then that lead to two effect one is called electro magnetization and reliability issues. So, whenever you have multiple connection, then

those connections should have multiple vias. So, if you have a wider metal, if I have a wider metal and let us say this is a horizontal metal and vertical metal. So, this is horizontal. So, we should have multiple vias here. So, this is improve the reliability issues. So, the supply nets should be wider than standard signal routes for because it basically holds the high current loads.

The wider metals have lower resistance and slow voltage drop. So, there are two approaches. One is called the basically the planar approach used for analog and custom blocks and the second one is the mesh approach used for the digital ICs actually. So, we will discuss about this Hamiltonian path actually. So, this Hamiltonian is a path in undirected or directed graph that visits each vertex exactly once. So, if you can see here, this red dot line or this line is basically a Hamiltonian path.

So, if you can see here, there are few things to note down from here. For example, you have a ground network. It is connected to one side of the block. All the ground network is connected to the one side of the block. All the VDD network is connected to the other side of the block. Since they both are not coming in the same side, so same metal can be used for ground and the VDD line.

So, this is the main point of a planar routing. So, here we need to planarize the topology. So, both the ground and VDD nets must be routed on one layer. So, it can be done using the Hamiltonian path and the net segments are assigned the appropriate routing layers based on our requirement. So, then we should have a width of the net segment which is determined basically based on the total current that all the cells to which it connects. So, basically the width of the metal will be determined based on the total current of each of the cells which it is connected.

So, then we have a mesh routing which is used for our digital flow. So, we should have a create a ring whatever I discussed in the previous example. So, here we should have a create a ring for core area of the chip and possibly individual blocks there are two things. So, you need to construct the ring for core area of the chip and also each individual block. Then we need to connect the IO pads, IO pads means the VDD IO and the ground IO to the ring that this is the second step.

Then we need to create a mesh. The mesh basically consists of set of strips at defined pitches on two or more layers. So, this mesh network is basically low resistance network compared to your ring network. So, we have basically that creates the metal one rails which will connect your all the standard cells. So, the mesh power mesh consists of a set of strips at defined pitches on the two or more layers and metal one rails will connect all the standard cells in the design because your VDD and ground networks is connected in metal one in a standard cell. Connecting the metal one to the mesh so we do the connection from the metal one rail to the mesh. If you can see here these are the VDD

line and ground line of the standard cells and these other lines are the top level layers top level metal layers that need to be connected to the lower level VDD and ground. So, these are in metal one. Now we have basically this power rail. So, this is your mesh this grid is basically the power grid is the mesh and this outer ring this is your ring.

This is your ring and these are your IO PADs actually. And these are the connections between the IOPAD. So, this is for metal one to metal four connections. If you can see here this is the first one is your metal one in the blue and the top this one is your metal four. So, in between you we have VIA1 this is VIA1 the yellow is the VIA1 then the metal two is in green. So, this is metal two then we have basically VIA2 is again yellow this is the yellow and then you have metal three is red here this is your metal three M3.

Then this yellow is your metal four M4. So, this is the way it is connected from metal one to metal four. Now for top level metal the width of the metal is wider. So, here basically we have metal four to metal six connections. Here is the metal four to metal six connections. So, these are the top level metal from metal four to metal six connection.

Now I have metal six to metal eight connections and the width of the metal in the top level is wider. Width of the metal in the top level is wider. So, one is for the VDD let us say this is VDD then this is ground like that it will repeat. So, this is all about the mesh routing which is very useful for digital IC design.

Thank you for your attention.