VLSI Physical Design with Timing Analysis

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Lecture 29

Introduction to Placement

Welcome to the course on VLSI Physical Design with Timing Analysis. In this lecture, we will introduce the placement. The content of this lecture includes introduction and levels of placement, then problem formulation, how we can formulate mathematically the problem of the placement, then design style specific placement problem, then we will do the classification of different placement algorithms. So, if you look into this VLSI physical design flow, we discussed about the partitioning first, then we discussed about the chip planning, then we are discussing the placement in this lecture.

So, this placement is one of the most important steps in a VLSI physical design flow. There are different types of placements at different levels of abstraction. One is called system level placement, one is called board level, one is called chip level placement. So, I have three levels of placements. So, we will discuss each one of them individually. The system level placement is basically what it does is that place all the PCB together basically in a small area such that the total area occupied is as minimum as possible. The goal is to reduce the area. So, if we have multiple components placed in a PCB and that can lead to overheating. So, this overheating is lead to the malfunction of the complete system. So, the heat generated by each PCB should be dissipated properly. So, that should be proper heat sink connected to the each of the PCB like in case of our processor inside our laptop or a PC or a workstation should have a cooling mechanism of a fan connected to the processor to cool down the processor.

So, some method to cooling the chips or the PCB should be attached to the system such that the system should not malfunction. Then there is a board level placement. So, in case of board level placement, we are designing the PCB. In this case, we are designing the printed circuit board PCB. So, what we are doing here arranging the chips and solid state devices on a fixed area in a single printed circuit board. So, the components are typically fixed. So, it is done by some person where all the components are fixed, rectangular blocks and some of the blocks are pre placed actually, some of the blocks are pre placed

in the board level. So, in case of board level placement, no specific limit on the number of routing layers. So, there is no layer limitation. However, there is two constraints.

If I increase the number of routing layers in the PCB, the cost will also increase, but there is no limitation in the number of layers in the PCB. So, but the primary goal of the board level placement algorithm is to minimize the number of routing layers to optimize the signal routing, it also reduce the cost of the PCB. And the second goal is meeting the system performance specification, especially the high performance circuits should be designed properly such that the speed of the overall system should not be compromised. In case of board level placement, the heat dissipation should be uniform across the board. So, if it is not uniform, then we need to take care or add some fan to the system cooling down the heat dissipated inside the PCB.

So, chips generating maximum heat should not be placed close to each other to avoid overheating. Let us say if you have two chips, both are generating some amount of heat, then both should not be placed together to avoid overheating. Then we will go to the chip level placement. Then we will go to the chip level placement. So, in case of chip level placement, one of the limitation is that number of routing layers are determined by the foundry or the process you are using. It will be determined by the foundry or the process that you are using. So, this is basically limited by the number of routing layers and fabricated in one side of the substrate. So, whenever you fabricate the chip, it should be fabricated in one side of the substrate. So, some bad placement can lead to the un-routability. Your design cannot be routed.

So, the placement plays a vital role how you can route each of the blocks together and all the nets are routed properly. So, the placement plays a vital role how to avoid un-routability problem. Accurate determinants of routing area in a chip level placement is essential. So, accurate determination of the routing areas is essential in case of a chip level placement. So, the main objective of chip level placement is to find the smallest possible area for a placement that is routable. So, we should find out a smallest possible area for the placement that can be routable. So, what is this problem of placement? So, what is the given to the problem and what is the output of the problem? So, the problem is basically we have a set of blocks. We have given set of blocks and its shapes are given. Height and width and aspect ratios of the blocks are given. Then pin locations are also given and a netlist.

Netlist means connection between the blocks are also given. These are provided to us. So, what is the placement problem here? The placement problem is to construct a layout indicating the position of each of the block such that all the nets are routed. That is the first goal and the second is that total area of the layout is minimized. So, there are another type of placement is called performance driven placement. In case of performance driven placement the goal is to minimize the total delay of the system. So, here the speed is

critical. So, we have to improve the speed looking at the critical part of our design. So, here we need to minimize the length of the critical path inside the chip. We need to basically minimize the length of the critical path inside the chip, inside the board or inside the system.

So, the quality of the placement is based on several factors. One is the layout area and second one is the completion of the routing and the third one is the circuit performance. So, the quality of the placement depends upon all these factors. Let us say these are the blocks given as input to your placement problem. And if you can see here that these are the block A, this is block A and this is block B, this is block C, this is block D like that. So, each one has the numbers written on the blocks. Those are basically nothing but your nets connecting between the blocks. So, here if you have one pin, pin 1 is also there in every other blocks. So, they need to be connected with each other such that my overall area is minimized, overall well length should be minimized. This is two placements are given to me.

One is the first one is the placement 1 and the second one is the placement 2. Then I can see which one is the best placement. If you can see here in the P2, you have lot of interconnect is going inside the bounding area and in case of P1, the interconnect distance is very small. So, P1 is a better placement, P1 is a better placement for this given problem. So, how can I formulate the placement problem? So, I have B1, B2, Bn to the blocks to be placed on a chip. Basically we have those blocks are given to the placement problem and each of the Bi is having its aspect ratio. Aspect ratio is nothing but its height and the width that is given to us. So, then we need to estimate the total wire length which is denoted by ni for each of the nets. Now what we need to do is that we need to formulate the problem. So, the problem of the placement is to find a iso-oriented rectangles. So, what is iso-oriented rectangles means that here what we are doing you have axis aligned rectangles means rectangles should be parallel to x-axis or y-axis. For each of the blocks on the plane to be denoted by R equal to R1, R2, Rn. So, these are the blocks or rectangles such that no two rectangles should overlap. No two rectangles should overlap means the coordinate of R1 and coordinate of Rj there should not be any overlap. So, Ri intersection Rj should be nil, null or phi.

Ri intersection Rj is phi for all possible combination of the blocks. This is essential to avoid overlap of the blocks. So, this is one of the constraint to the placement problem objective function whatever we are optimizing. So, then we have placement is routable. Let us say this Qj is sufficient to route all the nets actually. So, if your Q is Q1, Q2, Qk represents a rectangular empty areas allocated for each routing between the blocks. So, we need to assure that your Q should be routable means all the nets should be routed the rectangle should be routed and total area of the bounding box should be as minimum as possible. Total area of the rectangle or bounding box R and Q should be minimized. The

total wirelength is basically is found out by summing all the nets. This is need to be minimized total wirelength should be minimized for all the nets.

So, these are the nets N1 to Nm is nets representing the interconnection between the different blocks and Li is the length of the net Ni. So, we are calculating all the length of each of the nets and we are optimizing or minimizing the length of the interconnects. So, then we have if you have a high performance circuits then the length of the critical path or the longest path in the design should be minimized. So, we will look into different design style specific placement problem. So, we have multiple different design style the full custom design style is one of them. So, in case of full custom design style this placement problem is same as your packing problem. So, the packing problem is that whenever you have multiple things I need to put it into a box. So, I keep the bigger ones in the below and the smaller one in the top. Let us say I have multiple books are there the bigger books I put in into the in the below of a box. But the overlap of the books are allowed in case of packing problem. However in case of a placement problem overlap of the blocks are not allowed. Overlap of the blocks are not allowed. So, here what is the problem in case of packing problem the overlap of the blocks are allowed. But in case of placement problem no two blocks should overlap. So, then the second thing is as irregular shapes can lead to unused area. If you have different very irregular shaped blocks then you should have unused area left out in case of a full custom design style. We need to think each of the blocks such a way that we should all of them will be packed properly and there should be as minimum unused area as possible. Then the second category is called the semi custom design style and the standard cell is one of them. So, it is simpler than full custom placement because your cells have uniform height. So, this height of the standard cell is determined by the who is providing the standard cell to the third party company which is providing the standard cell to you for designing.

So, the height may be height of the cells can be 9 track, 10 track or 7 track also. So, depending upon the cell height all the cells have uniform height. So, there is no problem of placement. The cells are placed in a row. In case of standard cells all the cells are placed in a row. Then we need to minimize the layout area is equivalent to minimizing the summation of the channel heights, minimizing the width of the widest row. So, whenever I am minimizing the overall bounding box the basically some of the channel heights should be minimized and width of the widest row should be minimized. All the rows should have equal width to reduce the overall area. So, since the standard cells are placed in a row wise fashion so the row which is giving the highest width determines the overall bounding box. So, that width of that row should be minimized. The channel area includes the cell row and the second one is the routing or the channel area. So, earlier case there is a channels between the cell rows for routing purpose. But now there is over the cell routing where the channels in the standard cell have almost disappeared. So, leading to the channel less design style. So, now because of the over the cell routing

concept there is no channel in the in between the cell rows in case of standard cell based design style.

Now we have gate arrays the partitioning problem and the placement problem is quite similar in case of it gate array based design style. The placement algorithm assigns sub circuits or gates to the slots because this array all the arrays are same element. So, basically the placement problem is quite similar to the partitioning problem in case of a gate array based design style. So, assigning each block to a slot, slot means one of the unit of the gate array. Ensuring the two no two blocks share the same slot because it will overlap with each other and placement should be routable.

These are the two constraints. So, there are different types of placement algorithms are there which is the based on different outputs or inputs or process. So, we can divide that into three categories. One is the based on the process, one is based on the output, one is based on the input. So, the based on the process is three different types one is called simulated based approach this is one type then the partitioning based approach that is called the second type. Then there are other different placement algorithms are there that is the third type. This is on the how we basically using the method we optimizing. So, method based on the methods we are optimizing in the placement problem. Then the second one is based on the output whether my output is a deterministic or probabilistic. So, based on that I have two different category one and two. Now based on the input I have two types of placement algorithm based on the input type.

So, one is called the constructive algorithm and the second one is called iterative algorithm. So, we will discuss each one of them in detail. First we will discuss based on the input so I have constructive algorithm and iterative algorithm. In case of constructive algorithm the inputs is set of blocks along with the netlist. Inputs to the algorithm is set of blocks along with the netlist. And the algorithm what it does it finds the location of each of the blocks. In case of iterative improvement algorithm so what we have a initial placement and we can get that initial placement from the constructive placement algorithm. Then that placement is getting better at each iteration of your algorithm. So, in case of constructive placement we have one iteration but in case of iterative improvement algorithm we have multiple iteration to improve the placement. So, then we have basically based on the output classification of the placement algorithm based on the output.

So, this is one category the first category is deterministic placement algorithm. So, what is deterministic is that if the input is same your output is always same. Input means the netlist and the number of blocks is same your output is always same in case of a deterministic placement algorithm. The function is based on the fixed connectivity rules. Determine the placement by solving simultaneous equation that are deterministic simultaneous equation which are deterministic and it produces the same result for a given

placement problem. So, if your input to the placement algorithm is same then the output will be the same in case of deterministic placement algorithm. In case of probabilistic placement algorithm this is the second category which is based on the output. So, you are basically it works on the randomly examining the configurations. You may produce a different result for the same input placement problem. Even if the blocks and netlist everything given to the placement algorithm is same your output result may differ because of the random numbers that is used in the probabilistic placement algorithms.

Then we have based on the process. How we are optimizing? Simulation based algorithm is based on some natural phenomena. So, there are three types of placement algorithm one is called simulated annealing. Discuss this simulated annealing in detail in case of float planning. Then the second one is called simulated evolution and the third one is called the force directed placement. So, then there is a second category is called the this is the second category of the based on the process is called the partitioning based algorithm where the netlist and the layout are divided into smaller sub netlist and sub regions. So, your netlist and the layout is divided into smaller subunits and sub netlist and sub regions and the process is repeated such that each of the sub netlist and sub regions can be handled properly and all are routed properly. So, the one of the example of this partitioning based placement algorithm is the min-cut placement algorithm is the min-cut placement algorithm. There are other placement algorithms are also there. For example, cluster growth algorithm is one of them then we have quadratic placement algorithm then we have resistive network optimization algorithm. So, these are all other category of placement algorithms.

So, we discussed about the introduction of placement algorithm. Here we discuss about different levels of placement and how it is useful for doing the placement in the system level, board level and the chip level.

Thank you for your attention.