VLSI Physical Design with Timing Analysis

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Lecture 47

Timing Constraints in latch based system

Welcome to the course on VLSI Physical Design with Timing Analysis. In this lecture, we will discuss about what are the timing constraint in a latch based system. So, the content of this lecture includes timing parameter of a latch, then we will discuss about two-phase latch, we will discuss about the maximum timing and minimum timing analysis. So, we will discuss about latch. So, before going to the latch, we have already discussed about the flip-flop. So, what are the main difference between a latch and a flip-flop? So, you have a latch and a flip-flop.

So, the flip-flop is edge triggered and the latch is level sensitive. Either the positive level or the negative label. So, we have two different types of latch. One is called positive level sensitive latch, positive level sensitive latch or we have a negative level sensitive latch. So, in case of positive level sensitive latch, the latch is transparent during the positive half cycle. So, the latch will be transparent during this time and this is transparent means it will pass the data from input to the output. So, let us take a latch here and you have a clock here, then you have a D pin and this is Q pin. So, what it does is that when your latch, when the latch will pass the data from D to Q when your clock is positive. So, it is a positive level sensitive latch. So, and it will not pass, so it will be a opaque during the negative half cycle. So, this is for a positive level sensitive latch. Similar analysis holds for the negative level sensitive latch. In case of flip flop, we have two types of flip flop is there. One is called positive or rising edge triggered flip flop and the second one is called the negative or falling edge triggered flip flop.

So, in case of flip flop, it will not pass the signal all time, it will only pass when your clock is rising. It will only pass the signal D to Q when your clock is rising or clock is falling based on the time. So, for a positive or rising edge triggered flip flop, it will sample the data only in the rising edges like this is the first rising edge, this is the second rising edge. So, only it will sample or pass the data from D to Q in the rising edge and it is completely opaque or it will not pass the signal in rest of the times. So, it has a very

sharp edge, but latch is bit flexible and it passes the data completely half cycle. So, that is the main difference between a latch and a flip flop. With this discussion, we will go to the different parameters of a latch. So, what are the parameters we have latch has? So, latch has multiple parameters what are used for timing analysis. So, basically, we will discuss each of the parameter in detail. So, first one is the clock to Q t, tCQ or I can write t clock to Q maximum. So, this is called the latch clock to Q propagation delay or max delay. Similarly, the second one is tCCQ or t clock to Q minimum. So, this is latch clock to Q contamination delay or the minimum delay. Then the third parameter is T setup. So, the latch, the setup time of the latch, then the fourth one is T hold is the hold time of the latch.

These are quite similar to flip flop, but the latch has two more extra parameter which is called t data to Q or t D to Q maximum. This is basically latch D to Q propagation or the max delay. And the sixth one is T C D Q or T D to Q minimum. This is the latch D to Q contamination delay or the mean delay. So, these are the latch parameters. So, the first four is there quite similar to flip flop. So, flip flop has the same parameter. However, these two are the specially used for latch. These are the extra timing parameter of latch. So, these 5 and 6 are the extra timing parameter of the latch. Let us go and look into those things in detail. So, you have a latch is there. This is D, this is Q and this is clock. So, we can plot the different signals, then we can define those parameters. So, here if you can see you have a clock. This is your clock. Now you have a D, this is the timing diagram for the latch. So, let us this is the D, then your Q will appear after sometime. The Q will appear after sometime. So, there are two delays there. The Q will appear after the rising age of the clock. It will take some minimum time and some maximum time. So, what is the minimum time? That is called here you have a minimum time and it can also take some time to it will take some maximum time to settle to the actual output and it takes some minimum time or it start to glitch. So, this one this time is one timing parameter and this time is another timing parameter. So, this time is my T clock to Q minimum and this time is my T clock to Q maximum.

Now after this clock to Q parameter, now we have two more parameter which is called T D to Q maximum, T D to Q minimum. How can you define those parameters? Let us say my data is coming inside the positive half cycle. It is happening coming inside the positive half cycle. So, this is your D and Q will come after the D, but it will take some minimum time and it will take some maximum time. So, this is let us say the minimum time and this is the maximum time.

Let us say this from this to this is my minimum time and from this to this is my maximum time. So, I can write this one as my T D to Q, D to Q minimum and this one as my T D to Q maximum. So, basically we have two extra parameter which is not there in case of a flip-flop. Now and here the setup and hold information is slightly different compared to the flip-flop. So, how I can define the setup and hold for this? Let us say I

have a data. So, I will do it in the top to easy understanding. So, my basically your data is coming just before the falling edge of the clock. So, just before the falling edge of the clock and it is falling down just after the falling edge of the clock. So, what is the minimum time before this to this? What is the minimum time your data? This is your data. So, what is the minimum time before the falling edge of the clock? Your data should be stable such that it can be sampled by the latch properly is called the setup time.

So, this is your setup time and this is the minimum time after the falling edge of the clock your data should be stable such that it can be sampled by the latch properly that is your hold time. So, this is your basically p setup and this is your p hold. So, now it is slightly different from the flip-flop. We are checking the setup and hold in the falling edge of the clock signal for positive level sensitive latch. So, we will discuss about two-phase latch first.

So, what is the assumption is that here we do not consider any time borrowing. What is the assumption? We are not considering any time borrowing and path the path takes no more than 1 clock cycle. So, here this is assumption all the combinational logics are evaluated within 1 clock cycle. So, if you can see here I have a latch here.

I have a latch here. I have a latch here. So, L1, L2, L3. Now I have a this is phi 1, this is phi 2, this is phi 1. Now we have a combinational logic is there. So, this is combinational 1. Then you have a combinational logic is there, combinational 2. So, this is my D1, this is Q1, D2, Q2, D3, Q3. This is phi 1. So, the phi 1 is this one and this is phi 2. Now we have phi 1 and phi 2. Now we will see how my data D basically your clock period is this one. Come here till this one is your t clock. This is your t clock. Here first we will do the max timing analysis. So, I need to first pass the signal D1.

Let us say this is my D1. So, D1 is changing inside my positive half cycle. This is my D1. Then my Q1, Q1 will change after some time. This I have to take the max of the delay. So, this delay is basically t D2Q maximum, t D2Q 1 maximum because we are dealing with the latch 1 and this is my Q1. Now the signal is at Q1. So, now I have to go to D2. It will take some time to go to D2. So, how much time it will take to go to D2? How much time it will take to go to D2 is basically it will take some time to go to D2 this much time. So, inside this positive half cycle of phi 2 inside the positive half cycle. It can be early, it can be late, but if it is coming inside the positive half cycle then it can be sampled by latch 2 immediately. So, now this delay from here to here, this delay is my t combinational 1 max. So, because this is my t combinational 1. Now after that we have basically latch 2 is now transparent because it is basically this is the positive half cycle of the latch 2. So, the latch 2 is transparent then it can sample your data D2. So, now we have Q2 basically which will come after a delay of this one which is a basically latch parameter.

This delay is basically your this delay is t D2Q to maximum. Now we have basically D3 which will take some time to appear, but it should be available by this period to be sampled immediately. So, this delay is my t combinational 2 maximum because this is my combinational delay. So, D3 is this D3. Now I have a time period this t clock which consists of 4 parameters. What is the constraint here? Your constraint will be t clock should be greater than equals to the first parameter this one t D2Q 1 maximum. So, this is coming from this one then comes the second one this one plus t combinational 1 maximum then the third one t D2Q 2 maximum then the fourth one is this one t combinational 2 maximum. So, this is my constraint equation in case of a two phase latch.

$$T_{clk} \geq t_{d2q1}^{\max} + t_{comb1}^{\max} + t_{d2q2}^{\max} + t_{comb2}^{\max}$$

This is the constraint equation in case of a two phase latch where we are doing all the operation in one clock cycle. The path is not taking more than one clock cycle means we can borrow timing inside the latch but you cannot borrow across the cycle. We will discuss this time borrowing part in a separate lecture. For the time being you assume that both the combinational 1 and combinational 2 is executed or completed in one clock cycle. So, what is the sequencing overhead here? The sequencing overhead in this case is basically t combinational maximum plus t combinational 2 maximum should be less than equals to t clock minus t D2Q 1 max plus t D2Q 2 max. So, what is the sequencing overhead? We are basically finding the delay of the combinational path which is ideally it will take this much of time but if you do the sequencing or the basically synchronization using latches what is the extra delay we are adding to the path? So, this extra delay is basically this much. So, this is my sequencing overhead in case of a latch based system.

$$(t_{comb1}^{\max} + t_{comb2}^{\max}) \leq T_{clk} - t_{d2q1}^{\max} + t_{d2q2}^{\max}$$

Basically 2 D2Q is the sequencing overhead. So, now the same two-phase latch we are doing the second analysis which is called the minimum timing analysis. So, we will basically draw the latch based diagram then we will discuss the timing diagram. So, this is the latch 1 and we have this is D this is D1 and this is Q1 and you have some combinational delay. You can say this is combinational delay then your another latch is there this is phi 2 this is D2 and this is Q2 and this is L2. So, now we will discuss the minimum timing analysis.

So, here also we have phi 1. So, now we will do the minimum timing analysis. So, why this diagram is like that? Because we are considering basically the phi 1 basically it is arriving late means timing axis it is coming later and your phi 2 is coming early. In this case how my hold violation will happen. So, what is the thing here is that we have phi 1 and phi 2 then we have your D is changing let us say your D is here. So, now I have D1

so which is basically changing somewhere here before the basically positive half cycle of the phi 1.

Now it will take some time to come to Q1. So, what is that time? Q1 from the rising edge it will take some time to come to Q1. Let us say this time since I am doing minimum timing analysis this delay will be my t clock to Q minimum because I am taking from the rising edge of the clock. Now I have D2 what is the time it will take to minimum combinational delay. So, this time from here to here is basically my t combinational minimum. Now my hold time is basically this much from here, hold time is from here to here. So, my this one is my t hold, this one is my t hold. So, there are one more parameter is here which is basically this window from here to here this is basically your t non-overlap. This is my t non-overlap. Now tell me in one side my basically t hold should be there in other side all the components should be there. So, let us say my equation I am writing my equation t hold should be less than equals to what are the things will come. The first one is my t non-overlap because I am doing this calculation from this clock edge this falling clock edge. So, it should come t non-overlap plus t clock to Q minimum plus t combinational minimum. So, this is my constraint. So, for hold time if your non-overlap time is larger then it helps to avoid hold constraint. So, this is my hold constraint for a two-phase latch.

$$t_{hold} \leq t_{nonoverlap} + t_{clk2q}^{\min} + t_{comb}^{\min}$$

So, what will be my combinational delay in this case? This t combinational minimum should be greater than equals to t hold minus t clock to Q minimum minus t non-overlap.

So, this is my constraint in terms of combinational delay what should be there.

$$t_{comb}^{\min} \geq t_{hold} - t_{clk2q}^{\min} - t_{nonoverlap}$$

So, if your non-overlap time is larger then there is a less chance of having the hold violation. But non-overlap time if it is larger then your evaluation time for doing any operation through the latch also reduces. So, there is a trade-off between non-overlap time versus the available time for evaluation. So, we need to decide how much non-overlap time is suitable such that we can satisfy both my performance versus the hold constraint.

So, I will add one more point here. So, this hold time whatever it is there it is the parameter of latch 2 which is determined doing spice simulation it is a constant number but we cannot change that once the latch is used but we can change the non-overlap time we can change the combinational minimum. So, what is the point here is that your t hold should be less than your t non-overlap plus t clock to Q minimum plus t combinational. So, when you are using a latch from a standard cell library so you do not have anything to

play with what is the hold time that is given by the latch itself and also clock to Q minimum you cannot change it. These two are basically as a designer you cannot change so this t hold and this one cannot be changed. However these other two parameters like t non-overlap and t combinational delay is in the hand of a circuit designer.

So, we can use the t non-overlap or t combinational minimum to satisfy our hold requirement. We discussed about the two-phase latch-based system then we discussed the maximum and minimum timing analysis of a two-phase latch-based system. Thank you for your attention.

Thank you.