VLSI Physical Design with Timing Analysis

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Week - 10

Lecture 48

Timing Constraints in Pulsed Latch-based System

Welcome to the course on VLSI Physical Design with Timing Analysis. In this lecture, we will discuss about how to do timing analysis in case of a pulse latch based system. The content of this lecture includes maximum timing analysis of a pulse latch based system and minimum timing analysis of a pulse latch based system. So, now we will discuss about another type of latch called pulse latch, okay. So, we will discuss about the second type of latch called pulse latch. So, in case of two-phase latch, we are using phi 1 and phi 2 which is out of phase or they are inverted version of each other. But in case of a pulse latch, we are using a small pulse to all the latches. The same pulse will be applied to all the latches. So, the same pulse will be applied to all the latches in the system. So, how the system will look like? You have a basically latch 1 here, latch 2 here, then you have a combinational logic is there, then it is going to this one, then your pulse is phi p, this is phi p. Now, this is d 1, this is q 1, this is d 2, this is q 2, okay. Now, you have two cases here. Now, we will do for maximum delay constraint, okay. The first case is max delay constraint. So, what we are doing here? We have two cases, case 1, let us say A, case 1, case 1 where your T pulse width is greater than T setup, T pulse width is greater than T setup.

So, how the things will look like? So, here we have a basically pulse which is going to all the latches at the same time. So, when the pulse is high, then it will evaluate, when the pulse is low, it will not evaluate, but the combinational logic will do their job. So, pulse is used to only sample the data. So, if you can see here, we have a pulse like this. So, this is your pulse width, okay.

So, this is your T p w, okay. Now, we are basically giving the data T 1, okay. So, let us say this is d 1. So, your data is changing inside the positive half cycle. Let us say this is d 1, then your q 1 will appear after a delay of d 2 q, okay. So, this is maximum delay I need to take because I am doing the max timing analysis. So, from here to here, this delay is my T b to q, okay, maximum, okay, of the latch point. Now, the data is available here, this q 1, now the data is available here, this q 1. Now I need to consider d 2, okay. So,

how the d 2? So, the d 2 will basically change after some delay, d 2 will change after some combinational delay. So, from here to here, this delay is called T combinational 1 maximum, okay. So, now, this since my pulse width, okay, my pulse width is greater than, this pulse width is greater than my setup time, okay, your data can come inside the pulse to be sampled, okay, not a problem. So, now, we have this, what will be the constraint in this case? What will be my timing constraint in this case? The timing constraint in this case will be basically T clock should be greater than equals to T d 2 q maximum plus T combinational 1 maximum. Since you have only one latch is used, you can use, basically you can remove the one also, then this is same as your T p d q plus T p d. So, this is the constraint for a pulse latch-based system, okay.

$$T_{clk} \geq t_{pdq} + t_{pd}$$

So, what is the overhead here? This overhead is basically T p d, okay. So, what is the sequencing overhead? The sequencing overhead is basically T combinational should be less than equals to T clock minus p d 2 q T combinational maximum, d 2 q maximum. So, this is your sequencing overhead while you are using the pulse latch-based system.

$$t_{comb}^{\max} \leq T_{clk} - t_{d2q}^{\max}$$

But in case of a two-phase latch, the overhead is 2 p d 2 q maximum. So, this is the time period from here to here. So, this is my T clock actually. Now we will consider the case 2, b case. Case 2 where my basically the pulse width T pulse width is less than T setup, okay. So, everything is same. I am not drawing the latch diagram right now.

I will just draw the timing diagram. So, we will start with the pulse, okay. So, the phi p, I will have a pulse which width is smaller than my setup time of the latch, okay. So, now this is the pulse phi p. Now I have data d 1, okay. Data is coming early because my pulse width is less than setup time. So, what will happen is that you have to consider q 1 which is basically this q 1. So, this q 1 will take some time to come out, okay. So, this time is basically my T clock to q minimum, T clock to q minimum. Now basically your data need to be come to d 2.

So, I need to look into how much time it will take to go to d 2. So, we have a big combinational delay is there. So, it will take more time. So, let us say I will take more time to reach d 2, but we have one problem here. What is the problem? Earlier case your d 2 can reach the pulse anytime, but since your pulse width is less than my setup time, it should come earlier than my rising edge of the pulse, okay.

So, here it should come earlier than my setup time because my setup time is larger than the, let us say the setup time of the flop is larger, T setup than my pulse width T p w. So, to satisfy my setup time, the combinational part should be evaluated and reach before the

falling edge of the pulse. This is my hard edge. Before that falling edge, my data d 2 should reach the latch 2. So, this time before my falling edge, your d 2 should be evaluated.

So, this time from here to here is my T combinational maximum. This will be maximum. Now what will be my constraint now? So, I have very interesting constraint here. If you can see here, from here I need to consider till this point, till this point, but if I include my this one, then I can satisfy my setup time. So, what will happen is that your T clock, this is my T clock and this is my T p w. So, let us say T clock plus T p w is in the left hand side. It should be greater than equals to, what are the things there? T clock to q maximum plus T combinational maximum plus T setup. This is my constraint. So, my T clock should be greater than equals to clock to q maximum T combinational maximum plus T setup minus T p w. So, this is my constraint.

I can print it into a box. So, now, we have the timing constraint where your pulse width is less than T setup is this much. So, I can combine the both the things and I can write the combined equation here. The T clock should be greater than equal to maximum of T d to q max plus T combinational max which is coming for a case where my T pulse width is greater than T setup. This is the constraint coming from this and the second constraint comes, you have T clock to q maximum plus T combinational maximum plus T setup minus T pulse width. So, this is the case for T pulse width is greater than T setup. This is a case where T pulse width is less than T setup. So, we have two cases. We need to take the max to find the time period.

$$T_{clk} \geq \max(t_{d2q}^{\max} + t_{comb}^{\max}, t_{clk2q}^{\max} + t_{comb}^{\max} + t_{setup} - t_{pw})$$

Similarly, you can find the sequencing overhead in this case T combinational maximum should be less than equals to T clock minus max of let us say this from here to here is called T 1 and this constraint is called T 2.

This expression is then I can write T 1 comma T 2. So, this is my sequencing overhead in case of pulse latch-based system.

$$t_{comb}^{\max} \leq T_{clk} - \max(T_1, T_2)$$

Now we will go to the mean delay constraint, the case 2, mean delay analysis in case of pulse latch-based system. So, let us take a latch L 1, this is D 1, this is q 1. Now I have a combinational delay.

Why this latch is done like this basically is that we are looking into the same timing edge that is why these two latches are drawn in the same line. So, whenever you are considering the hold violation, we are considering the same clock edge that is why two latches are in the same column. So, now we will discuss how I can do the timing analysis

in this case. So, if you can see we have one pulse is there. So, now I have basically the phi, phi p I need to plot first. So, the timing diagram of phi is this one. This let us say I did little bigger to make it more clear, but you can make it smaller also not a problem. So, this is T p w pulse width. So, this is D 1. So, the D 1, so it is coming earlier to the pulse like this. So, this D 1 is same as this D 1. Now you have q 1, q 1 is this q 1. So, it will take some time, but when it will come appear? It will appear after the rising edge of the clock. So, this delay it is my T clock to q minimum because I am doing mean delay analysis. So, I have to take T clock to q minimum. After q 1 now I have to consider D 2. So, D 2 will appear after this combinational delay. So, this combinational delay should be minimum delay from here to here. This is your T combinational minimum. So, now your hold time will be around the falling edge of the pulse.

So, this is my hold time. As I discussed the setup and hold will be around the falling edge. So, this hold time is around this one. So, this is your T hold actually. So, my T hold requirement will be now will be T hold. So, your data should be stable at least till this hold point. Okay. So, my T hold requirement is that T hold this one and plus p p w should be less than equal to my I will start from here. So, this one, this clock is I am starting from here T clock to q minimum plus T combinational minimum. Then you do not have any hold violation. So, this is my hold constraint in case of a pulse latch.

$$t_{hold} + t_{pw} \leq t_{clk2q}^{\min} + t_{comb}^{\min}$$

So, the T combinational minimum should be greater than equals to T hold plus T p w minus T clock to q minimum to satisfy my hold requirement.

$$t_{comb}^{\min} \geq t_{hold} + t_{pw} - t_{clk2q}^{\min}$$

The combinational delay should be more to satisfy the hold requirement. As you can see there is no overlapping pulse here unlike a two phase latch. So, the hold requirement is severe in case of a pulse latch. In this lecture, we discussed about the maximum and minimum timing analysis of a pulse latch based system.

Thank you for your attention.

Thank you.