VLSI Physical Design with Timing Analysis

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Week - 10

Lecture 50

Crosstalk Analysis

Welcome to the course on VLSI Physical Design with Timing Analysis. In this lecture, we will discuss about crosstalk analysis. The content of this lecture includes introduction to the crosstalk, then what is the impact of crosstalk on the delay, then we will discuss some of the techniques to avoid the crosstalk. So, basically in deep submicron technologies, crosstalk is one of the most important parameter in the signal integrity of the design. So, it plays a very vital role in the signal integrity of the design. So, people spend lot of time to do this analysis to conclude that there is no issue due to crosstalk. So, what is this crosstalk actually? It is a noise. Noise means which is not required. It is not intended or not intentionally given, but it is there. So, it is non-intentional coupling of activity between two or more signals.

So, there are multiple signals going inside the chip. They couple with each other and disturb each other. So, that is the reason it creates a crosstalk noise. So, what are the causes of the crosstalk noise? There are several causes of the crosstalk noise. Some of them are increasing the number of metal lines. So, increasing the number of metal lines, we have lots of signal is going in different metals and there is metal to metal capacitance is there. So, there are two types of crosstalk is there. One is between the across the metal and between the same metal. So, inter-metal or intra-metal. So, there will be inter-metal crosstalk. Then the second one is intra-metal crosstalk. So, intra-metal means that let us say I have a metal 1, I have another metal 1, what is the coupling capacitance between them? So, this is called same metal. This is M1, this is M1, same metals. But inter-metal means that we have M1, this is M1, this is M2. So, there is some capacitance between them.

This is M2. So, this is called inter-metal crosstalk. So, the increasing the number of metal lines also increases the crosstalk noise. Then it also depends upon vertically dominant metal aspect ratio. So, it also depends upon the metal aspect ratio. Aspect ratio means width and the length. So, it depends upon the width and the length of the metal. Then the third point is that larger number of interactive devices and interconnects. Because of the large number of interacting devices and interconnects, long interconnect lines we have

crosstalk. Then the fourth point is that higher routing density. So, if more routing is happening in a small area, there is a chance of crosstalk. And it is possible because of the finer geometry, because the process allows us to put the metal close together. So, there might be multiple different signals is going in the same small area. But it satisfied the DRC rules. So, we can fabricate it. But there is some coupling between the signals. So, that is one of the reason. Then the fifth one is faster waveforms due to higher frequency. Whenever you are going for higher frequency, you have sharp rise time. You have a signal which is rising very sharp.

So, that will couple more compared to the slow rising signal. So, rise time is sharp, T rise is sharp. Then the crosstalk is higher. Then the sixth one is that whenever you are working in the low supply voltage, small glitch will lead to a crosstalk. It will lead to changing of the logic value. So, these are the main reason of crosstalk noise. So, it is caused by capacitive coupling between the neighboring signals. So, between the neighboring signals, what is the capacitive coupling is there, that is the main cause of crosstalk. So, there are two types of signal is there. One is called the victim signal and one is called the aggressor signal. The signal which is affected is called the victim signal. The affected signal is called the victim signal. Its signal will degrade. And the signal which is affecting, that is called aggressor net. So, affected signal is called the victim net or the victim signal and affecting signal is called the aggressor net or aggressor signal. Net can be victim as well as an aggressor. One net can be a victim as well as an aggressor. So, if you can see this circuit, you have different nets are there, N1, N2, N3. Three nets are there, very long interconnect. So, these are the drivers, okay.

So, this is one, this is the buffer, this is one buffer and long interconnect is there. So, if you can see here, there are several coupling capacitors are there, CC1, CC3, CC4, all these are coupling capacitor. The signal in one line will couple with the other line and it will degrade the transition time, delay and it will create glitches in the victim net, okay. The aggressor net will affect the victim net. So, there are broadly two types of noise effects due to crosstalk. One is called the glitch and the second one is a timing issues. So, the glitch basically is a noise caused by a steady victim signal when the victim signal is steady due to the coupling of switching of activity of neighbouring aggressor. So, your victim signal is steady and the aggressor signal is switching. During that time, it will create a glitch in the victim net. So, in case of timing, we will encounter crosstalk delta delay.

Why it is happening? So, your victim net is switching and aggressor net is also switching and the aggressor net will create a delay in the victim net. So, that is why it is called crosstalk delta delay. Now we will go into the glitch where your aggressor net is switching but the victim net is steady. The steady signal net can have a glitch. The glitch can be positive or negative due to the charge transferred by the switching aggressor through the coupling capacitor. So, we have a coupling capacitor between the basically

adjacent lines. So, those coupling capacitor helps in transforming some amount of charge from the aggressor to the victim that causes glitch. The glitch can be positive or negative. So, let us look into this diagram. So, you have a gate, NAND gate which is basically is a aggressor net.

Then you have another line is there which is basically a victim net, which is a victim net. So, we have a coupling capacitor between these two lines, between the aggressor net and the victim net. So, there is a transition is happening in the, transition is happening in the aggressor net and the victim net is stable. It is steady. It is not doing any kind of transition. So, what is happening is that some amount of charge is transferred to the victim net through these coupling capacitors. So, some amount of charge is transferred to the victim net through these coupling capacitors. So, through this coupling capacitor. So, the steady state value of the victim net in this case is zero or low is restored because So, there is a fight between this glitch, this glitch and there is a basically the pull down network. It has a pull down network is there.

So, there is a fight between them. So, the pull down network is pulling it to the ground. And this glitch is basically coming from the aggressor net. So, since the pull down network if it is stronger then it will basically dissipate the glitch. So, now we have two types of coupling, capacitive coupling. So, first case we are discussing here. The capacitive coupling to a floating line. Let us say I have a line and I have this one is the floating net. So, assume a voltage at node x experiences step change of delta vx. So, it is changing by delta vx. So, we have a floating net y is there. So, how much charge will be transferred to the y net. How much voltage will appear in the y net. So, this you can do using the resistive divider method. Basically these two capacitors are in series. So, the voltage across them is basically voltage across these two point is Cxy divided by Cy plus Cxy multiplied by delta vx.

$$-\Delta V_Y = \frac{C_{XY}}{C_Y + C_{XY}} \Delta V_X$$

So, this amount of voltage will appear in y node. So, this is kind of noise appearing into the floating net. So, this is the second type of capacitive coupling where you have one line x is there and the other line is also a driven line. The driven line is y, y is the driven line and the interferer or the aggressor is x. So, the x is the aggressor net and y is the victim net. If you can see you have few observation here is that your x axis is the time and y axis is the height of the voltage or the voltage height of the glitch. So, whenever your rise time of the signal vx, so the rise time is sharp, t rise is sharp implies that the height of the glitch is high. Height of the glitch is high. Sharp means you are doing a this is sharp transition. If I am doing a slow transition like this, tr is slow then height of the glitch is short.

Height of glitch is short. So, if you can see here whenever the t rise is 5 picosecond, height is higher, height of the glitch is higher. This is the height. Whenever my tr is 500 picosecond then the glitch height is smaller, but the width is larger. So, this height and width of the glitch is very important whenever you are doing timing analysis of the victim net. So, basically if you can look into this one, the magnitude of the glitch is caused is dependent on variety of the factors. What are the things height of the glitch will depend? One the first one is obviously the coupling capacitance between the aggressor net and the victim net. Then the second one is the basically the rise time, t rise or t fall of the signal in the aggressor net. So, that is important. And the third point is that the victim net grounded capacitance. Victim net grounded capacitance is this Cy. It depends upon Cy also. Then the fourth one very important victim net driving strength. If your victim net is driving with a strong driver then it can overcome the glitch. But if it is a weak driver then the glitch will more compared than expected.

Glitch will be more. So, there are different types of glitch is there. One is called rise and fall glitch. For example, if you can see this is called the rise glitch because it is going from 0 to 1 and the fall glitch it is going from 1 to 0. Then we have second category is overshoot. Overshoot is this one. If it is going beyond the VDD value then undershoot basically whenever it is going down below the ground. So, all these are possible whenever you have crosstalk related glitch. So, we will discuss about the crosstalk delay analysis. So, here what is most important part is that how good your parasitic extraction engine. So, the parasitic extraction of a typical net in a nanometer design contributes from many neighboring conductors. So, since I told you you have wire density is higher, you have more nets are going in a smaller area and smaller area you have lot of coupling capacitors. So, that will lead to basically huge contribution of coupling capacitors to the interconnects. So, there are two types of neighboring nets are possible. One is the basically neighboring net is steady means not switching. Then the inter signal capacitance can be treated as grounded.

So, in this case when the neighboring nets are not switching means the aggression net is not switching then the inter signal capacitance can be treated as grounded. And the second case is that when it is switching the charging current through the coupling capacitor impact the timing of the net. So, if you look into this diagram, so whenever there is no switching in the aggression net this CC is basically called the grounded capacitor. Then we have a basically this is aggression net and this is the victim net and this is your distributed RC line and you have a NAND gate driving that distributed RC line. So, with reference to this diagram we have three different cases are possible. We will discuss one at a time. So, this capacitive charge required from the driving cell in various scenario. One first case is that your aggression net is steady. There is no switching in the aggression net. Second case is that aggressor switching in the same direction as the victim net. And the third case is that aggressor switching in the opposite

direction of the victim net. So, if your aggression net is steady, so we have two capacitor here. One is this is the coupling capacitor and this is the capacitor of the victim net. So, that need to be charged to VDD. This VDD it is charging. Since CC is grounded because your aggressor is not switching the total capacitance because these two are in parallel, total capacitor is CG plus CC and the total charge will be multiplication of VDD. So, this is your total charge Q. Then in this case no crosstalk is considered from the aggression net. So, here there is no crosstalk is possible because aggression net is not switching. So, what is the voltage before and after the transition? So, let us say you have a V of CG is 0. Initially it is 0 and it is moving to 1.2. So, the CG will be VDD. Basically there are two conditions possible when this transition is happening. Your aggression net may be low if your VCC is 0. So, now after charging the VCC will be VDD. Because one line is VDD, this is my victim net and the other line is aggression net is grounded.

So, this capacitor is charged to VDD. Since this is low, this is grounded, so this capacitor is VDD. But when your basically aggression net is high, so this is aggression net is VDD and your victim net before charging it was 0. So, in this case this capacitor will be minus VDD. But after charging one side is VDD because your victim net is changing from 0 to VDD. So, this capacitor is basically this is also VDD. So, the voltage across this capacitor is 0. So, the voltage across this capacitor is minus VDD before transition. After transition, voltage across this capacitor is 0 because both the plates of the capacitor has the same potential. So, here the aggressor is switching in the same direction. So, both are switching in the same direction. This is the second condition, aggressor and the victim net is switching in the same direction. So, in this case if the slew of the aggressor net is faster than the N1, the actual charge required can be smaller than CG times VDD. If the signal is rising faster in aggressor, then the actual charge required can be even smaller than CG times VDD. Since the aggressor net can also provide some charge for charging the CG.

So, since they are moving in the same direction. So, your aggressor and the victim is doing the transition in the same time. So, here the transition is happening at that time and the same time your victim is also doing the transition. So, if you can look into this, the charge before transition in both the cases is 0. Both the cases is 0. Before transition both the cases is 0. And after transition you can see both the aggressor and the victim has the same potential. So, the CC is 0. You can see your CC is 0. Now what will happen to the CG? CG is charged to VDD. CG is charged to VDD after the transition. CG is charged to VDD after the transition. So, what is the impact? It will reduce the delay of the victim net. So, which is called as a negative cross-talk delay. It will reduce the delay of the victim net. So, if this aggressor is not there, the delay is let us say that this one, the dotted line, this is the delay without the aggressor. And this is the delay with the aggressor. So, my delay is reduced. So, this is a negative delay. So, this is a negative delay. So, it is used in case of a mean path analysis because while doing the mean path analysis, we always deal with the minimum delay of the path. So, this is used for mean path analysis. The

similar kind of thing will also happen when your aggressor and the victim is switching in the opposite direction. So, the coupling capacitor will charge from minus VDD to plus VDD and the total charge coupling is basically 2 times cc into VDD. This is the total charge before and after the transition. So, because one is moving in this direction, other is moving in the opposite direction at the same time. The CG if you can see, the CG is basically initially 0.

Let us say the CG is initially 0, then after transition your CG will be VDD. After the transition, the CG will go into VDD. So, this is my initial condition if then the CG will be VDD after the transition. Now what will happen to my cc? The cc I need to check what is the cc condition. So, this is 0 and this is VDD. So, the cc will be minus VDD. The voltage across cc is minus VDD. Voltage across cc is minus VDD. And after you do the transition, then your, this will be 0 and this is VDD. So, the voltage across the cc will be VDD. So, we are basically doing the analysis from this part to this part actually, this part to this part.

So, now what is the impact of this kind of transition? Whenever there is an opposite transition, then it will increase the delay. This is called positive cross-talk delay. This is normally used for max path analysis because it will increase the delay. So, without cross-talk , this is the delay. This is the transition without cross-talk and this is the transition with cross-talk. So, your effective delay increases. So, your effective delay increases. Since effective delay increases, so your, there is an increase in the delay, so that we can use it in case of max path analysis. So, how we can utilize this one in static timing analysis? The cross-talk analysis verifies the design with worst case cross-talk delay for the data path and the clock path. We have two paths. One is called the data path. This is your data path what we discussed in our week, second week lecture. So, this is your data path and this is the capture clock path. So, we need to consider for the worst case, data path should be late and clock path should be early for setup check. So, we are doing the setup check.

So, your launch clock path and the data path have positive cross-talk. So, this is launch clock path and the data path should have positive cross-talk delay because that I need to make it worse and this capture clock path should be negative cross-talk, should be negative cross-talk delay. So, it should have a negative cross-talk delay for setup check. So, your launch clock path should have a positive cross-talk and data launches late and data path should have a positive cross-talk. Data takes longer for data to reach the destination.

Similarly whatever we discussed the capture clock path should reach early. So, hold analysis to check the worst case condition, your launch clock path and the data path have negative cross-talk and the capture clock path should have the positive cross-talk , just opposite the setup condition. So, your launch clock path should be negative cross-talk,

data path should be negative cross-talk delay and the capture clock path should have positive cross-talk to consider the worst case hold check. So, this need to be considered while doing the static timing analysis. So, there are several techniques is there to avoid cross-talk . One is shielding the lines, then we will increase interconnect space, then so your victim net should have a faster slew rate, then we should have a very good supply voltage which is having less fluctuation. We can introduce guard ring to avoid cross-talk , we can use deep n-well to isolate our blocks and you can do isolation of the blocks. All these are techniques used to avoid cross-talk , but it will indirectly impact your increase the area of your design or something it is not come free. So, but we need to take the cross-talk into account while doing the static timing analysis because it is used in case of sign off phase of your static timing analysis. Thank you for your attention.

Thank you very much.