VLSI Physical Design with Timing Analysis

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Lecture 09

Delay Parameters of a Combinational Circuit

Welcome to the course on VLSI Physical Design with Timing Analysis. In this lecture, we will discuss about the delay parameters of combinational circuits. So, there are several delay parameters which is involved in the combinational circuits those will be discussed in the detail in this lecture. The content of this lecture includes the combinational circuits. So, we will first discuss about the combinational circuits. So, the delay parameters of a logic gate which is basically the basic building block of the combinational circuits. So, the delay parameters includes the propagation delay and transition time and then we will discuss about the delay of a timing path. Let us say we have a delay of the individual gates, how you can find the delay of the timing path? First of all, we will discuss about what is a combinational circuit. So, the combinational circuit is a circuit such is a circuit or a block.

If you give any signal to that one, if you give any signal to that one, it will come out after a delay after certain delay. So, if the input changes, then the output will respond immediately. So, these are the inputs and these are the outputs. So, it is a bunch of line, it can be one or multiple output lines. So, the thing is that let us say I will apply some input to some combinational circuit. Let us say I will take an inverter which is very easy to understand. If I give a pulse to that one, the output will come out after certain delay. It will come out after certain delay. So, there is one more point involved here. Let us say the delay of the gate is let us say t inverter. The pulse whatever I am applying to the gate should be larger than T inverter, then only it will come out. So, there is a case 1. So, the pulse, the input signal whatever I am applying, the delay of that pulse is let us say T pulse.

So, when you will get the signal at the output? When your T pulse is greater than T inverter. So, then the pulse will appear at the output of the gate. The case 2, T pulse is less than T inverter. Then the pulse will not appear at the output. So, this property is called inertial delay property of the combinational circuit or logic gates. This property is called the second category is called inertial delay property. This property is called of the logic gate is called inertial delay property. So, this is the behavior of a combinational circuit.

So, the pulse width, the width of the pulse basically let us say if I change this pulse, this is your pulse width. So, this is your pulse width. So, that should be greater than T inverter, delay of that inverter such that the pulse will appear at the gate and we can measure the delay. Now we know that if we pass a signal through a combinational circuit or a logic gate, it takes some time to appear at the output. How we can use that information to measure the delay and use that in timing analysis? So, how we can use that concept to measure the delay of the gate and use that concept in the timing analysis? So, here we need to define some parameter here.

One is called the propagation delay of a combinational circuit or a logic gate. So, you can specify here the logic gate. Then we will go to the combinational circuit in this lecture itself. So, propagation delay of logic gate first. So basically, whenever you have any logic gate, we need to consider, we need to measure between 50% of the transition point of input output waveform. Let us say I have a inverter. So, if I give a pulse here, so the 50% of this point to the 50% of the output point, output point we need to consider. So that is called your propagation delay. So, there are two types of propagation delay. One is called the rise propagation delay, one is called the fall propagation delay.

So, whenever we define the rise propagation delay, we define between 50% of the input to the 50% of the output when the output is changing from low to high. Your output with respect to the output of your rise propagation delay is defined. Whether the input is rising or falling does not matter, but your output should rise. So then it is called the rise propagation delay. So, this is the behavior of the output signal. This is the output signal. In case of rise propagation delay, whenever you are measuring the rise propagation delay. So, whenever you are measuring the fall propagation delay, we need to measure it from the 50% of the input to 50% of the output when your output is doing a transition from high to low. So, your output is changing from output signal is changing from high to low in case of fall propagation delay. So, now we can define average of that one which is called the average propagation delay which is called (TpHL + TpLH) / 2.

So, in this lecture, I will use this TpLH by Trise also and this is called Tfall. So, I will use either TpLH or Trise and TpHL or Tfall. So I will use this notation throughout the lecture. So, now we will discuss this definition in detail. Let us talk about the inverting gate. Whenever I have a inverting gate, let us say I have a inverter. I have a inverter here. So, I will have input and I have output. So let us say I will plot in the same scale at time t equals to 0. So this is the waveform for the input and this is the waveform for the output. So let us say this signal is doing a transition like this. Now my output is doing a transition like this. It will take a delay. It will create some delay like this. So now this one to this one, the 50 percent. So, the supply voltage is VDD here. This is VDD here. This is 0 volt. This is VDD. This is 0 volt. This is VDD. I have to take VDD by 2. This is the input VDD by 2. This point to this point. What is the output is falling? So, TP high to low. TP high to low. So, this delay is basically TP high to low. Similarly, if you take this point and this point.

So, this is output is rising. So, it is called TP low to high or I can write this as T fall or I can write this as T rise. So, this is for inverting gate.

Now, we discuss about the non-inverting gate. So, let us say I will consider a buffer. So, I have a buffer here. So, this is input. This is output. I will plot that same thing in a same scale. So, I have here input. I am doing a transition like this. So, now output. So, this is your VDD point. This is your 0 volt. So, let us say this is your VDD point and this is your 0 volt. So, now your output will follow the same waveform with some amount of delay. So, this 50 percent to this 50 percent, this is called your T low to TP low to high because this is low, this is high or you can say T rise. So, now from here to here, this is T high, this is high to low. So, TP high to low or T fall, correct. So, this is the definition of rise propagation delay and fall propagation delay in case of an inverter, inverting gates and non-inverting gates. You can say this was whatever we discussed in the last lecture. Non, basically we have positive unate and negative unate. So, positive unate means that your non-inverting gates and inverting gate means your negative unate type of gates. So, this is the definition. Then we have two more parameter which is also important. One is called the basically rise transition time and fall transition time.

So, if you can see whenever your signal rise from 10 percent to 90 percent, either 10 to 90 or some cases they do 20 to 80 depending upon the depending upon its uses either you can do 10 to 90 or 20 percent to 80 percent of its maximum value. Similarly, fall transition is taken for the signal from 90 percent, sorry, so either 90 percent to 10 percent or 80 percent to 20 percent of its maximum value. So, if I have an input signal, I will give an example here. If I have an input signal, this input waveform, I have a waveform like this. So, this 10 percent to 90 percent, this distance is your basically rise transition. You can, this is called rise transition. You can write as slew rise. So, this one is your called P fall slew, correct. So, this is for the input signal.

Similarly, we have, this is for the input signal. This is for the input signal. Similarly, you can define it for the output signal also. So, let us say I am doing, going through a buffer. So, I am doing the waveform. It will delay some amount. So, now I have, let us say I will take 90, sorry, 10 percent to 90 percent, this is your T-slew rise. Similarly, this is your from 90 to 10 percent, that is your T fall slew. This whatever the analysis we did, it is for a buffer. So, if you can look into this table here, which is called a dot-lib, which is used extensively in timing analysis, used extensively in static timing analysis. Static timing analysis. So, if you can see here, you have some parameters here. So, here what is the thing here is that your cell rise. Cell rise is your T p, cell rise is same as your T p low to high or T rise whatever I defined in the previous slide. Similarly, cell fall is basically your T p high to low because your output is changing from high to low or T fall. So, for a logic gate, these two parameters are characterized prior before doing the timing analysis of a path. So, similarly, if you can see here, you have rise transition and the fall transition. So, this rise transition is related to your output rise transition, output signal rise transition and this is

related to output signal fall transition. Output signal fall transition. So, here we will discuss about how these tables, what is the use of that table and how it is created.

Let us say I have a logic gate. Let us say consider an inverter. Here whenever I give a input signal to that one, I have a output waveform also at the output. So, the delay the cell rise or T p low to high, the cell rise whatever we saw in that table or T p low to high is basically a function of two things, most important two things. One is your function of your output load capacitance, the C L and the input transition time, input transition time. So, in case of a inverter, basically your cell rise will depend upon your fall input transition time, the function of C L output load which is common for both of them and input fall transition time.

Similarly, your cell fall or T p high to low is a function of C L output load capacitance and your input rise transition time. Why this is? Why rise and fall? Because whenever you are finding the cell fall, let us say if I have a, whenever I have a input or I can go back to the here. So, here if you can see your T rise will depend upon the fall transition time. I can draw it in different color. So, it will depend upon the fall transition time. So, basically you can write in a particular notation T fall, T fall slew at the input side. Similarly, your T fall is depending upon your T slew rise at the input side. So, this is the reason your cell rise will depend upon the input fall transition time. Similarly, cell fall will depend upon the input rise transition time. Then we also need the output transition time.

We also need your output transition time. Your output transition time, let us say this is rise is a function of whatever you are discussing is for a inverting gate and the things will change for a non-inverting gate is a function of t he C L. So, output rise transition time will also depend upon. So, your basically your output is rising in case of inverter. So, it will depend upon the fall input fall transition time. Output transition time fall is a function of C L comma input rise transition time. So, there is a question comes we are most worried about the cell rise and cell fall, why you are calculating the output transition time?

So, we are most worried about the delay of the gate, why you are calculating the output transition time? So, you have to think for a minute, and you can see that let us say I have one inverter followed by another gate is there, the NAND gate is there, then you have a NOR gate is there. So, I can give the input at this point where I can find the delay of the inverter, which is function of the input transition time; for the second gate, I also need a input transition time to find its delay of the second NAND gate. So, I need to evaluate what is the transition time at that point. Similarly, for the NOR gate also I need to find out the transition time at this point. So, I have to evaluate four parameter, one is called at this point I need to evaluate four parameters, one is called cell rise, cell fall, then the third one is output transition time rise and similarly output transition time fall. So, these four parameters should be characterized for each gate. So, that is why whatever I showed you, you have cell rise is one parameter, cell fall is another parameter, then rise transition is a

third parameter and the fourth is fall transition is the fourth parameter that is needed for each gate to be characterized and stored it in a table, then the STA will use that to do the timing analysis. So, let us take a path, let us take a path and do the timing analysis.

So, delay of a timing path. So, I will create a path here, I will create a path here. Let us say inverter, then you have a, let us say NAND gate, then you have a NOR gate, this is a path. So, this is the input and this is the output. So, if you can see here, we need to find the complete delay, complete cell rise for the complete path, and cell fall for the complete path that is called the TPLH for the path, TPHL for the path. So, how I can do that? So, let us take some of the things whatever I was talking: P rise of 1, P fall of 1, T rise of 2, P fall of 2, P rise of 3, and T fall of 3. So, this is the three parameter whatever I got it from that library dot lib files and I am not considering a transition time at this stage. So, let us say my delay of this T rise, all these things will take some parameter, but let us say I will find the total TPLH of the path, how can I do? So, let us say I have this first parameter. So, first of all, you see all things are inverting. So, all things are inverting in nature. So, if I can check this is one parameter, T rise 1 will add with T fall 2 and this will add with T rise 3. So, now my output is rising, T rise 3 means output is rising obviously. So, rising means TPLH of the path. So, if I do right here, this will be T rise of 1, T fall of 2 plus T rise of 3. Now, in case second case, in the second case, so I have T fall of 1, T rise of 2 and T fall of 3. So, now I have T fall of 1 plus T rise of 2 plus T fall of 3. So, let us say I have these numbers given to me, then I can find the path delay. So, T rise of 1 is let us say, T rise of 1 is 2, T fall of 1 is basically 3, T rise of 2 is basically 4, T fall of 2 is let us say 4 and T rise of 3 is let us say 6, T fall of 3 is basically 3 say. Now, I have to find the, let us say this T rise is the path, T rise is the T rise, T fall of the path. So, now my T rise will be, I need to add this like this.

So, 2 plus 4 plus 6, it is 12. Now I can add in a like this. So, T fall is a path. T fall is basically 3 plus 4, 3 plus 4 plus 3, which is 10. So, your rise delay, T rise is greater than your T fall. So, your rise propagation of this path is greater. So, the rise path is critical compared to the fall path. So, in this lecture we discussed about rise propagation delay, fall propagation delay, rise transition time and fall transition time, how it is used, how these four parameters are used in case of a dot lib for doing the timing characterization of the complete path.

We take an example of a timing path using inverter, two input NAND gate and NOR gate and we show that how the timing is calculated in the path using those T rise and T fall.

Thank you for your attention.