Power Electronics

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Lecture - 36

Effect of Switching Time lag in Inverter

Till now we talked about inverters, so till now we assumed that inverter switching, the top switch and the bottom switch, switch on and switch off are instantaneous but most of the time, not all the time, this semiconductor switches will have finite turn on and turn off time. So, we have to appropriately get the gate pulses, especially in a leg or in a pole the top or bottom devices such that there should not be any short circuit through the DC link. So for example, in this figure, see, one leg is shown here.

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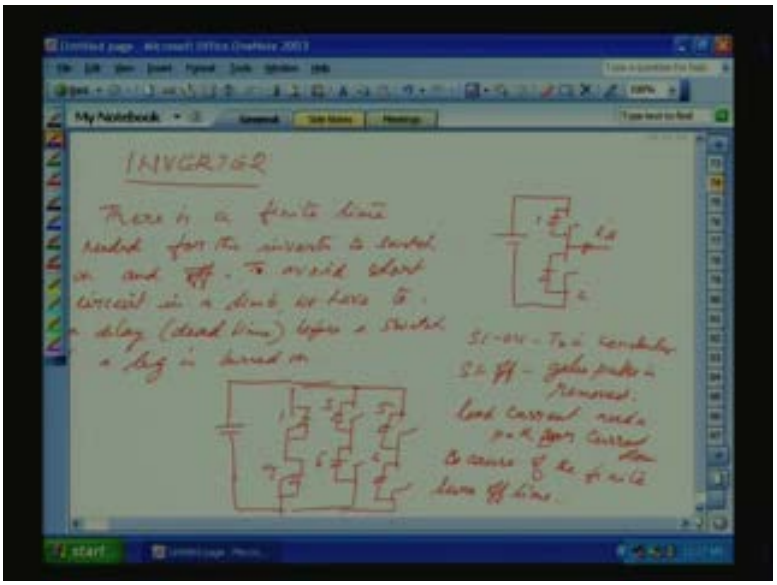

So, let us say S_1 is turned on. Now, due to PWM action, when S_1 is turned off, we will be immediately turning on S_2. So, let us take a condition where S_1 and S_2 have finite turn on and turn off time that is a practical condition. So, even though S_1 gate pulse is removed, S_1 will take some finite time to turn on. Now, the moment if S_2 is given; before S_1 turns off, S_2 will turn on. So, what happens? There is a short circuit and heavy short circuit current will flow. So to take care of that one, the a pole or in a leg, whenever a device is turned off and when the next device is turned on, there is a delay time between the turn off and the next turn on device is … This is called dead time. So, it has effect on the output. So, we will study that effect in this class.

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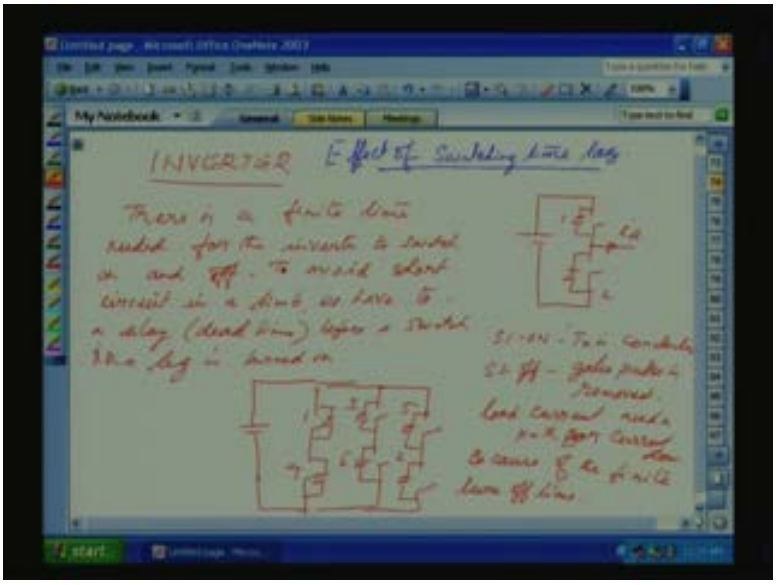

So, effect of switching lag times that means switchings are not instantaneous, there is a lag is there, there is a dead time is there, we are going to study effect of switching lag times, switching time lag. So, as written here, there is a there is a finite time needed for the inverter to switch on and off that is what I explained before. This is turned on and now, once the gate pulse is removed, this will turn off. But according to our so for assumption, immediately we will be turning on this one. So, before if you turn on this one, before this is turned off, there will be a short circuit in the limb. So, we have to give a delay, dead time before a switch, before a switch in a leg is turned on, before a switch in a leg is turned on.

So, what happens? S_1 is on, when S_1 is on, depending on the current direction, even though the gate pulse is given, even though the gate pulse is given, depending on the current direction, if the current is positive; let us say current is in this direction, S_1 is on, then the transistor or the power device will be conducting but for an inverter operation, this current can be negative also. See, in the negative case, current will be flowing through diode but diode, the moment it is reversed biased or the current is removed, it will quickly switch off.

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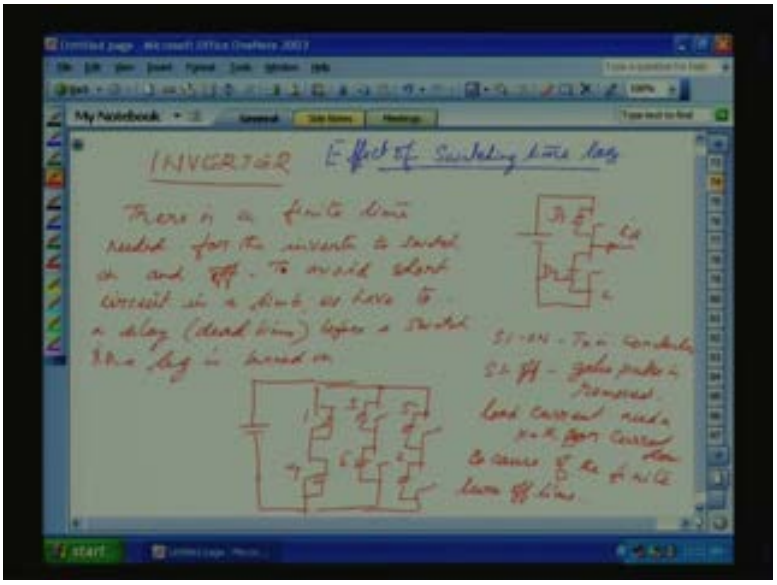

But the devices; transistors or MOSFET's, it requires a more or some more time to turn on and turn off. So, when S_1 is on, in this case, current is flowing through the transistor. Now S_1 is off, as I told before, S_1 is off, now we are giving a switching lag time that is S_2 is turned on after some time. But in this case because the current is negative, when the S_2 is turned on; the device, the transistor is not conducting here, here the diode D_2 will be conducting, diode 2 D_2 will be conducting, here it is D_1.

So, in this case, instantaneously, the moment this is turned on, the current through ia starts decreasing but current cannot change instantaneously. So, this load current will force it to come through diode. So, in this case, the switching lag, switching dead time will not have will not have effect because diode will conduct immediately respective of whether the transistor is turned on or not.

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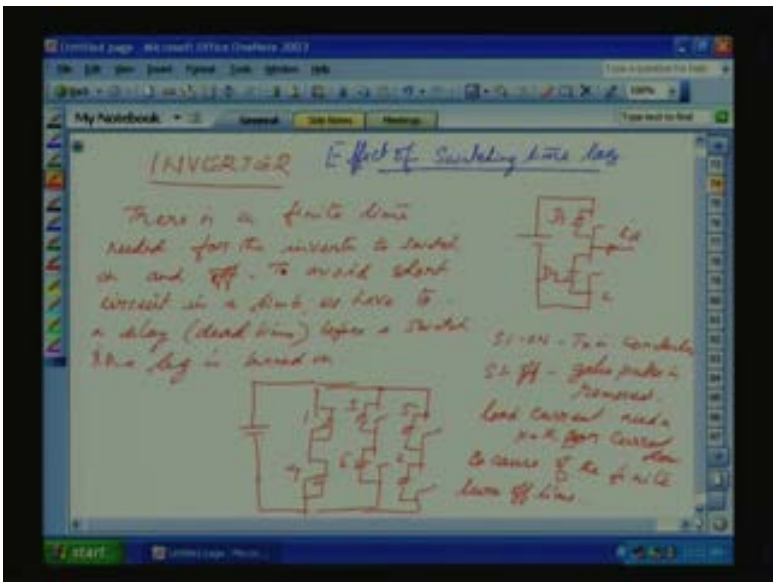

But if you see, let us take a case, now transistor is turned on, even though the diode is conducting, if we give instantaneously the transistor gate pulse if you give it; see it can turn on immediately. Before it is turned off, there can be a short circuit. So, we have to give; even though the diode is conducting or transistor is conducting, we have to give a finite turn on time, finite delay before it is or the incoming device is turned on. So, let us study the effect of this one. Again, we will draw the switching circuit.

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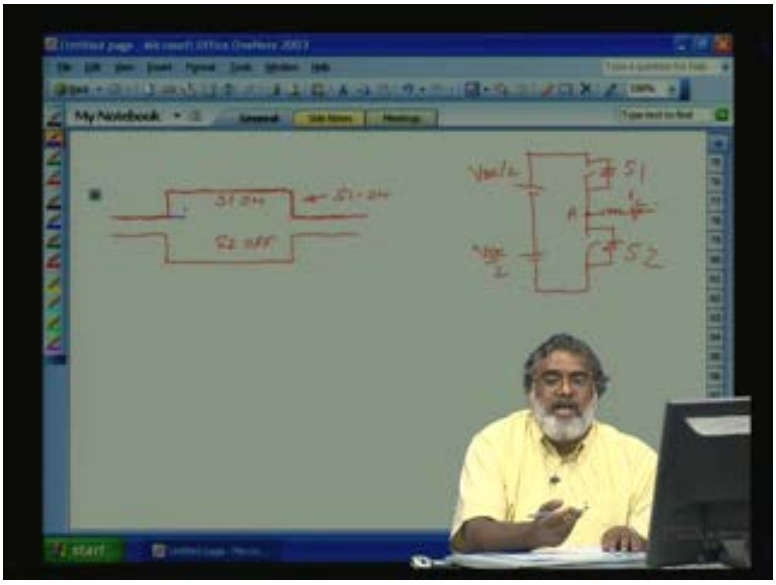

Let us take the one limb or one leg; this is V_{DC} by 2, V_{DC} by 2, this is the diode, this is A, then the current direction is like this. Let us say, the ideal switching time that is so far we concerned instantaneous turn on and turn off. See, let the ideal switching time is like this, S_1 turned on, S_1 is turned on; so if the switchings are instantaneous, this is S_1, S_1 switch S_1 that is S_1, this is S_2. If the ideal switching, during S_1 is turned on, S_1 on, during this period, S_2 will be off. So off, we will represent as a negative pulse like this. At this point only S_2 is on; so S_1 on, S_2 off.

If you see, the switchings are instantaneous but what we said? We will give a delay. So, instead of turning on here, we will give a delay of let us say delay of td. So, we mark with … So, let us say the delay, so depends on the device. Let us say, for thyristors, it will require converter gate thyristors into large time, 30 to 40 micro seconds but for a present IGBT or power transistors, you will get few micro seconds. But still when the PWM switching, it can affect the output. So, we will study the effect of that one. So, we will give a delay and then turn on.

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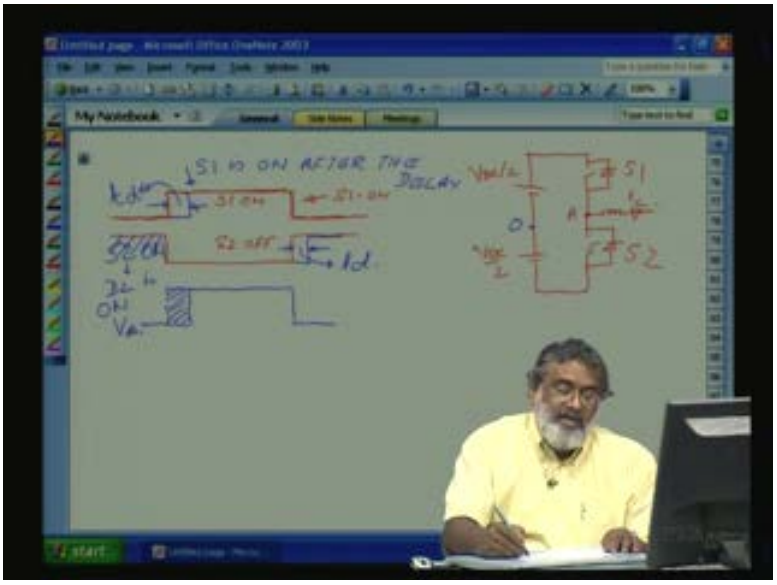

So, this is the delay we are giving; instead of turning on here, S_1 is turned on, S_1 is on after the delay; this delay we will mark as td. Similar way, at this point, we have to S_1 is turned off and S_2 is turning on here but here also S_2 turning on, we are delaying by this much, again td. So, simultaneous turn on and turn off of device is avoided. So, this can avoid the short circuit, DC link short circuit. Here also, we are giving a dead time of td. So, this will take care of that one. But what will happen to or what will happen to the output voltage waveform?

Let us say S_2 is, till this point, S_2 is turned on that is S_2 is on, S_2 on. Now, according to this current direction, this point till this point, D_2 will be conducting. S_2 is on and D_2 is conducting, D_2 is on; now because of the current direction, current direction this is direction we are taking, positive. Now, we want to turn on S_1, so we will remove the gate pulse here. But even though the gate pulse is removed here, S_2 diode will be conducting. Now, diode will be conducting, after some time only, we will be turning on S_1. So, what you say? Previously, we want the output voltage to go like this; if we say the V_{AN}, V_{AN} or V_{A0}, this is our V_{A0}, V_{A0} should have gone high here. But because of the delay, it has gone high here only. Again, at this point when S_1 is off, immediately diode will conduct that is instantaneous.

So, if you see here, for the pole voltage, this much area is lost due to the dead time, this much area is lost. But since the diode or whenever the diode conducting, the conductions are instantaneous that time even the dead time will not have effect. But whenever the switching device active device is instead of diodes, transistor conducts, because of the delay this much area is lost.

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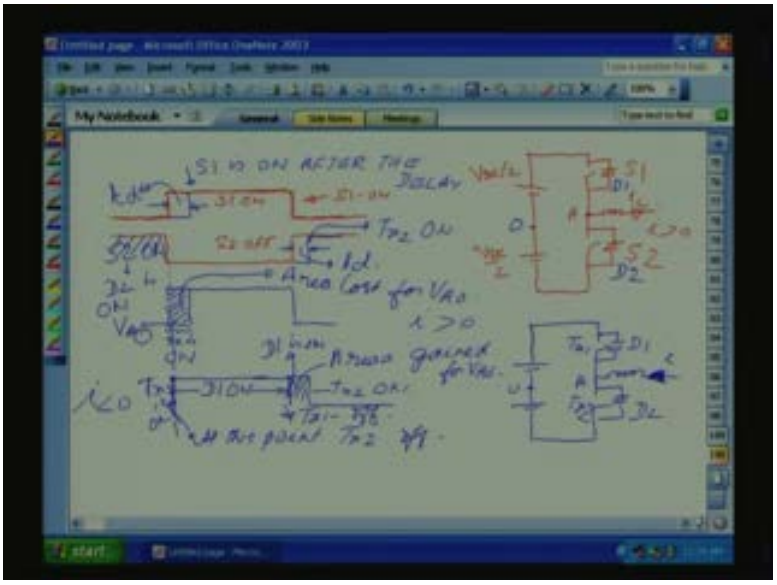

Now, till this period, D_2 will be conducting, till this period this period, D_2 will be conducting, D_2 is on, this much area is lost, area V_{A0}, this is V_{A0}, area lost for V_{A0}. So, this we will say, this condition is when i is positive that is greater than zero, according to this connection. Now, when i is negative, negative means this is positive, this current will be in this direction, negative; then let us say, in that case, what happens? In that case, D_2 will be conducting. When S_2 is on, the transistor will be conducting; not D_2, transistor will be conducting. So, the moment gate pulse is removed, immediately D_1 will be conducting. So, dead time will not have effect.

Let us see now i is less than zero; this is this condition, we will say i is greater than zero. Now, let us take the condition i is less than zero, this we will draw with a different colour. Now, the current is negative, so the direction we will put it like this; current is moving in this direction, i. So, this condition, we will represent as i is negative, i is less than zero. Then what happens? Let us take here, again according to the same switching here, when current is less than at this point, what happens? Till this point, current is negative means transistor is conducting here.

So, here again, we will draw the part again so that it will be clear. So, till this period, till this period, what is conducting? Transistor is conducting that is this one, transistor; this is transistor 1 or transistor 2, transistor 2 is conducting 2 is r. Now, the moment the transistor is removed, S_1 is on. So, V_{A0} will be here, V_{A0} will immediately go high and till this point, till this point, we are turning on S_2. See, current is less than negative, less than negative, D_2 will be conducting. At this point, the transistor is off; here, at this point, at this point, transistor 2 is off. So, what happens? Transistor is off but current cannot change instantaneously, so diode will immediately conduct.

So, from here to here, D_1 will be conducting. At this point, what we will do? Transistor one is off but since D_1 is conducting, transistor turn on turn off will not have effect. So, D_1 will continue to conduct till this d td period. So, here also D_1 is on. Now, when T_2 is on at this point, here, this is at this point, Tr_2 on; at this point when Tr_2 is on, D_1 the

current will be transferred from here to the Tr_2. So, from here onwards, Tr_2 is conducting, Tr_2 is on.

So, if you see here, when the D_1 area is, D_1 is conducting because of the dead time, the V_{A0}, this much area is gained, area gained that is volt-second, area gained for V_{A0}. So, what happened? It can affect the fundamental. How it can affect? Let us go to the next page. So, what we studied so far? What we got the information now; due to dead time, the pole voltage that means due to dead time, due to dead time sorry so what we have, due to dead time, time, there is a, there is a change in area that means volt-second in the pole voltages.

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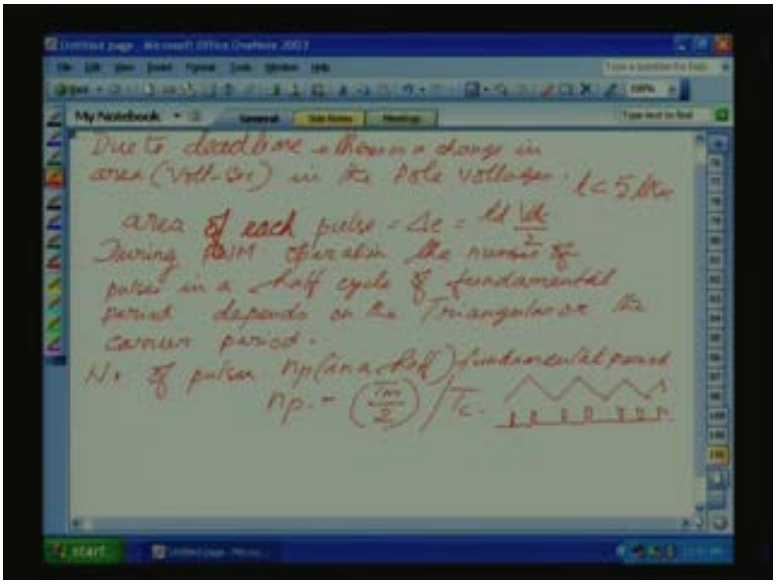

So, how it can affect? What is the area of each pulse? Let us say the area of each pulse that is delta e is equal to td that is the dead time into Vdc by 2, this td may be 5 to or less than a micro second. Usually, td let us say td less than 5 micro second, so we may think that it is negligible. But let us take a PWM operation; during PWM operation, during PWM operation, may be six step operation it is okay but during PWM operation, the number of cycles the number of pulses in a half cycle of fundamental period, period depends on the triangular period or the carrier period or the carrier period.

That means the number of pulses, let us say the number of pulses N_P in a half fundamental period is equal to half fundamental period is the modulating wave; so Tm by 2 divide by the carrier period. This is N_P, number of pulses and this number of pulses if you see here, due to carrier period, whenever the sign touches the triangle; you have these types of pulses, small pulses.

So, this type of pulses if you say, half period, you can see lot of pulses together and if you see, it will look like a rectangular waveform. So, this can be approximated as a, the whole thing is approximately equivalent to a square pulse like this. So, let us find out the area of the pulses, area of the pulses, the height; see these pulses we can approximate to a rectangular pulse of height h and this period is equal to Tm by 2 that is Tm by 2.

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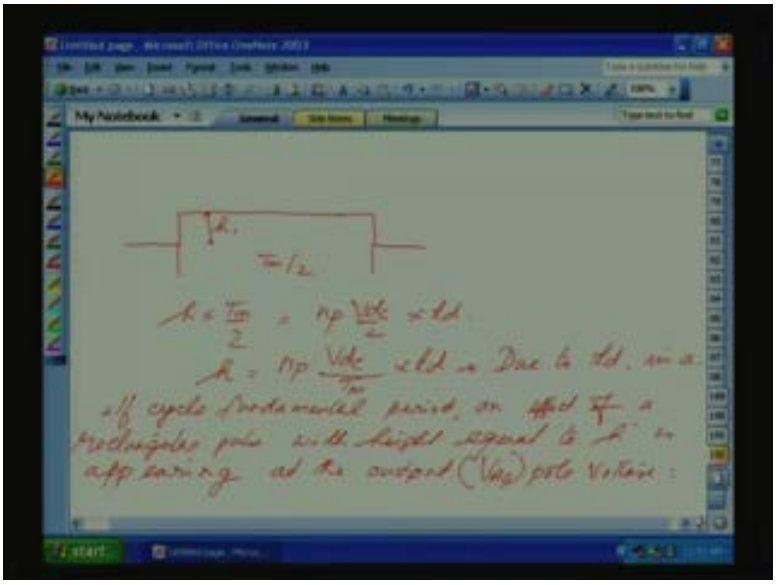

So, what is the area? h into Tm by 2 is equal to number of pulses into Vdc by 2 into td, it is a rectangle, approximate. This is the total area in a half cycle because of the number of pulses, these are equivalent to a, we are equating to a square pulse or rectangular pulse of height h into Tm by 2. So, what is h? h is equal to N_P into Vdc divide by Tm into td. So, what happen? So, dead time effect due to dead time effect, td, in a half cycle fundamental period, an effect of a rectangular pulse with height equal to h is appearing at output voltage, output V_{A0} pole voltage, pole voltage.

Even though we have used sine triangle PWM for nearly sinuous or average variation, now there is an effect of rectangular pulse. Let us see how this affects? This also depends on the current error direction. So, let us see, how this affect happens? So, let us study the effect of this dead time effect now.

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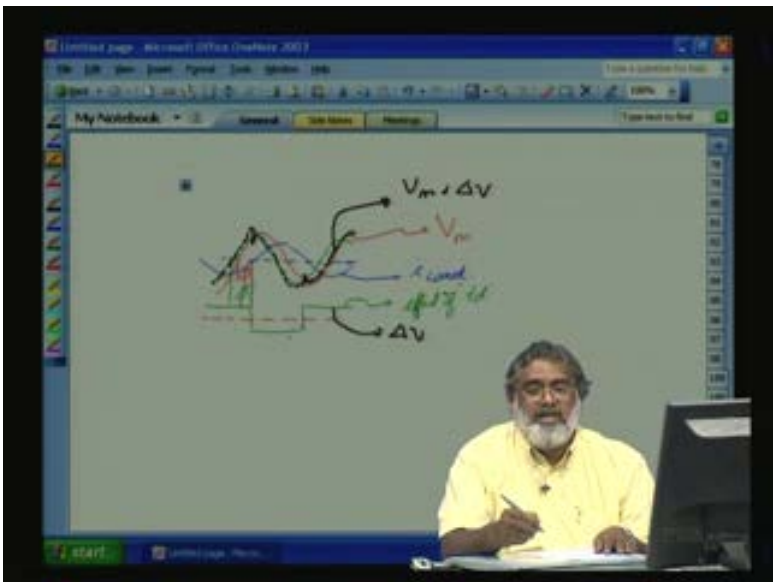

Let us see, this is our reference current, then this load current and this is our x axis. So, this is our i load. Now, the reference wave form, the actual current, actual waveform what we want from the PWM modulation, let this be this one. So, this is the wave form what we want. So, between the current and the voltage, there is a face difference of 5, this is our modulating waveform what we want, Vm from PWM; this is from the PWM operation, what we want.

Now, let us see the rectangular pulse due to the dead time effect. So, if you see here, with current, I will draw it here, according to the current direction that is current, current is negative as I told we have an increase in the increase in the effect. So, there is an increase approximating with, so this is, this also, this effect of, this is the effect of dead time. So, if when the current is negative, there is an increase in the pole voltage waveform; when the current is negative current is positive, there is a decrease in the pole voltage waveform. So, what we get instead of the V reference? This also get added to this one, so if you add this one, the wave form will be approximately like this that is here, suddenly there is a decrease, again there is an increase here. So, this will goes like this. So, there is a distortion in the output V_{A0}.

So, if you say, this is the Vm plus our, this waveform we will say, delta v, effect of dead time. So now, the new fundamental waveform if you see here, new fundamental waveform is here approximately. So, there is a shift in the fundamental waveform. If you see here, what is the shift? Shift is this phi dash, this is phi dash. So, we are adding a rectangular pulse.

Now, apart from the fundamental, due to the effect of rectangular, it can also contain fifth, seventh and low order harmonics. So, even though we are using sine triangle PWM, with large carrier frequency and dead time effect; if the dead time is very large, it can introduce fifth and seventh effect and the current waveform, instead of sinusoidal, it will be distorted with an effect of, with an effect of fifth and seventh visible in the current waveform.

So, many applications, people think we can give large dead time so that the short circuit is safe but this is the problem here. So, let us write the phasor diagram; phasor diagram how it looks? We can draw the phasor diagram here, let us see.

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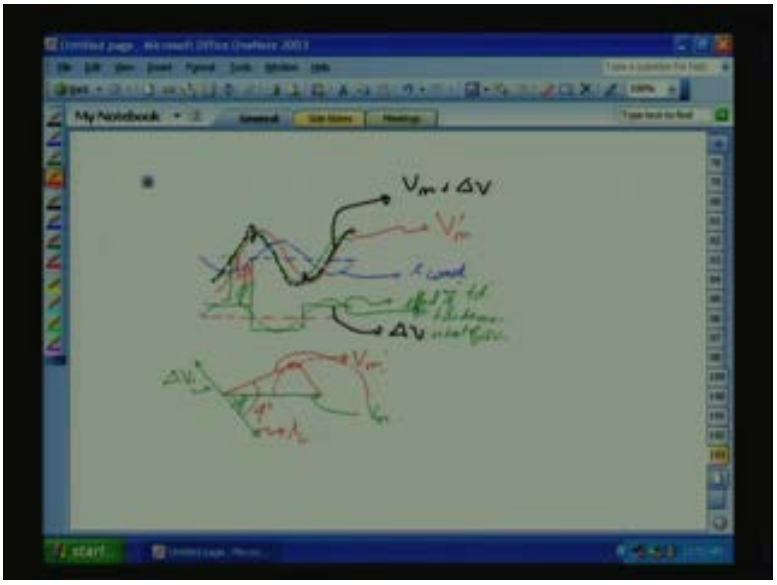

This is our reference Vm, now our i loads, this is our phi from this figure. Now, according to this one, the fundamental component of this one is exactly opposite to the current component of this one, the fundamental component of this one will be approximately here. This is fundamental of delta V. So, exactly opposite, so that means exactly here it will come. So, fundamental we will take it as delta V_1 this one.

So, what happens? The net V reference, the net V reference next modulating waveform Vm dash will be here. So, this is our new Vm dash that is exactly this waveform, new Vm dash; this has to Vm dash, this is our new Vm dash and the new angle will be phi dash. So, with various load operation as i_L, let us say i_L varies, i_L varies then this will, this can go like this. So, let us say unity power factor, then i_L will exactly come here along with V_L. Then what happens? The net Vm dash gets reduced. When im is in this direction that is with unity power factor, it is regeneration opposite side, then the Vm will increase.

So, what happens? Even though we are operating the system for a particular modulation index, we will not be getting the correct modulation index. So, it can affect or output waveform can get distorted. So, what it shows?

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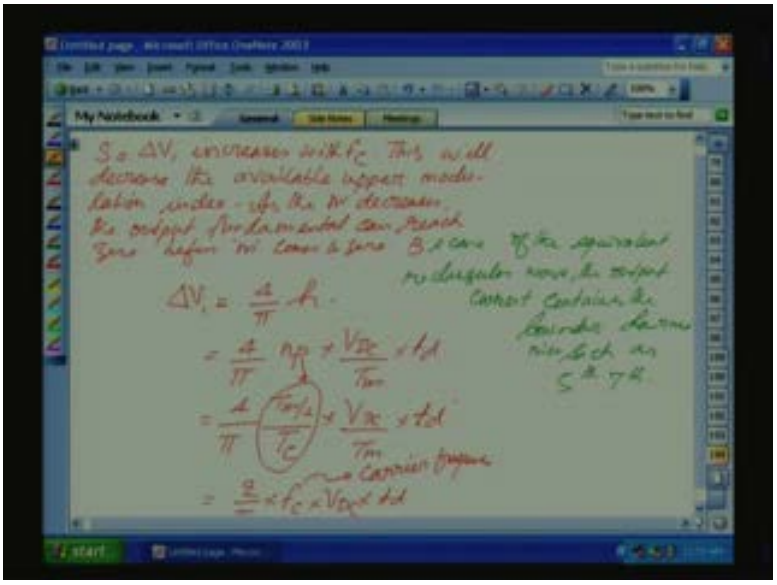

The delta V_1 we can say, 4 phi into h height that is equal to 4 by phi into N_P into V_{DC} by Tm into td, dead time is the fundamental law of the equivalent square wave, rectangular wave that is equal to 4 by phi Tm by 2 divide by TC into V_{DC} divide by Tm into td because we know N_P is equal to Tm by TC. This is equal to 2 by phi. What is Tm 2 by TC? This we can approximately write F_C into V_D into td, F_C is the carrier frequency. So, what it shows?

It shows delta V_1 increases with F_C for a fixed dead time. This will decrease the available upper modulation index, upper or the maximum modulation index. So, what is the effect? As the modulation index m decreases, the output voltage, the output fundamental can reach zero before m comes to 0. That means the relation the modulation index that is the sine triangle PWM that is output is proportional to our modulating may be is lost here. Also, because of the equivalent rectangular wave introduced, the D_2 dead time, the output current contains, output current will contain the low order harmonics, harmonics such as fifth and seventh.

So, even though PWM waveform we are using high frequency PWM, output current get distorted. So, many high performance drive application when we require near sever speed operation, dead time effect has to be compensated. So, for dead time compensation, we require the direction of the current. So, a typical way to reduce this one, we can see in the next slide.

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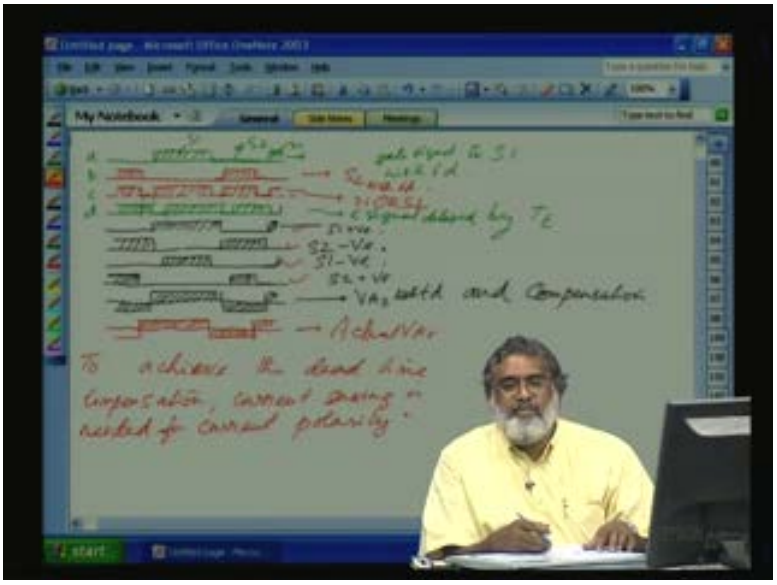

So, let us say, this is the actual gate signal to S_1 that is the top switch S_1 or S_1 or S_2, we can take it any signal because when it is 0, this is S_2; so, this is S_1, here it is S_2. Now, with dead time let us say, the conventional logic signal to S_2 that is b sorry this is not the actual signal, the gate signal to S_1 with dead time; sorry this is the gate signal to S_1 with td.

Now, let us draw the gate signal to S_2 with td. So, this is gate signal with td to S_2, S_2 signal with td. Now, what we can do? We will OR this logic signals that is we will generate this one; k, the zero line for the logic OR gate is like here. This signal is S_1 OR with S_2. Now, this signal let us delay by td that means here, see let us say this is a, this is b, this is c, this is d. So, d is, the c signal delayed by T, c signal delayed by Td that is this one, the top signal is delayed by td here that means this is the one, td.

Now, from this one, we will generate the actual signals for S_1 positive, S_1 gate pulse and S_2 gate according to current is positive or negative. So, let us take, I will say S_1 positive is the signal one, the current is positive. So, I will turn on the device here, actual signal, I will generate here; this is the S_1 positive. Suppose you take positive current is positive, now what about S_2? S_2 current is then S_2 current is negative, this is S_2 negative when the current is negative. Then, from the delayed signal, when S_1 is negative, this is S_1 negative.

Now, S_2 positive that is current is positive. So, if you this is S_2 positive, so if you see here, the output voltage, the gain dead time effect, the gain lost and gain removed gain, gain lost and gain volts second gain can be compensated like this. So, the output voltage waveform will be V_{A0} will be like this. This is the actual output waveform, this is zero that is V_{A0} with td with td and compensation, dead time compensation and the actual signal without compensation, what we require if you see here, it is like this that is actual V_{A0}.

So, actual V_{A0} and the compensated V_{A0} if you see, the areas are same, positive and negative areas but the waveform is slightly delayed by td that is okay; td for a switching

device is equal to around few micro second so that will not affect for a motor fabrications application, this delay is very negligible. But here what we want? To achieve this one, you require, to achieve the dead time compensation, to achieve the dead time compensation; current sensing current sensing is needed. This is not a problem because most of the motor drive application, current sensing is required.

So, with current direction, current polarity, for current polarity; then depending on the current polarity, the signals gate signal - S_1, S_2, S_1 negative, S_2 positive, we can give based on the original signal with the dead time. So, the whole dead time is derived by td only. So, this way dead time compressive can be achieved. There are various techniques available, this one technique. It is possible to achieve the waveform and the current and voltage distortion output voltage during PWM operation with that time can be compensated.