Design for Internet of Things
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Lecture – 08
Design with an LDO

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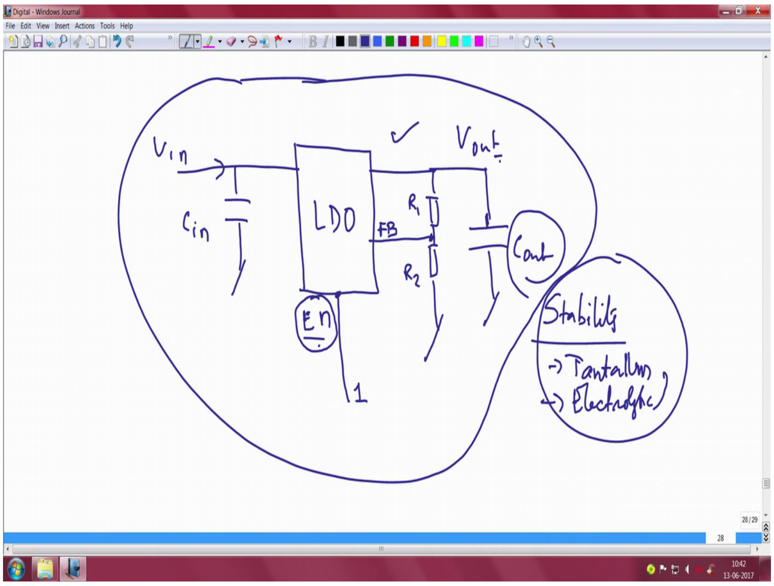

So, this LDO is quite simple to use you can see that these 2 resistors that you have to install on your LDO over that you buy and put an output capacitor C out, and then an input capacitor and that is all that is required for this circuit to work and so let me give you an overview of this LDO types.

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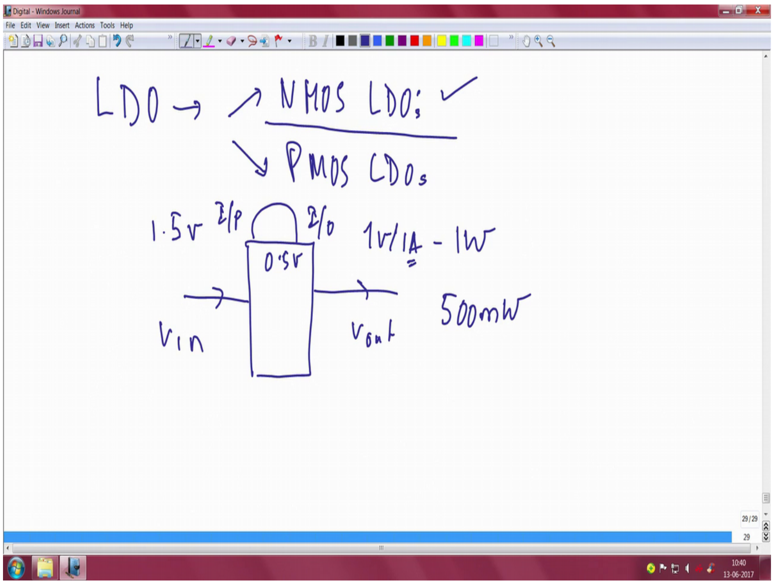

LDO when you want to buy you do not have to worry. So, much about it, but it is important to know what are the types of LDOs, which are available to you will get n CMOS or n MOS LDOs and PMOS, PMOS LDOs, alright.

So, you can. So, where are they used and in what conditions do they is each one of them used thing is, if you are looking at input V in V out typically in the range of let us say 1.5 volts at the input and regulated 1 volt at the output then you can be more or less sure that must be a n MOS kind of a LDO, because that is what ultimately I mean that is what people are most of the companies which give you offerings will actually used as a technology. You can have this 1 amp given at 1 volt to given at 1 amp. So, you will be dissipating one watt, but the difference the drop out is only 0.5 volts right. And if it is one watt if it is 1 amp you only have 500 mill watts of dissipation. You do not need any great heat sink you do not need any great heat sink between input and sorry let me. So, input this way IP and IO. You are dropping only 0.5 volts you are dropping only 0.5 volts and the current that is being drawn continuous to be 1 amp sorry it is about 500 mill watts.

So, that is typically what a n MOS that you can buy in the market. PMOS on the other hand is perhaps not with this kind of a input voltage ranges, but it could be much higher.

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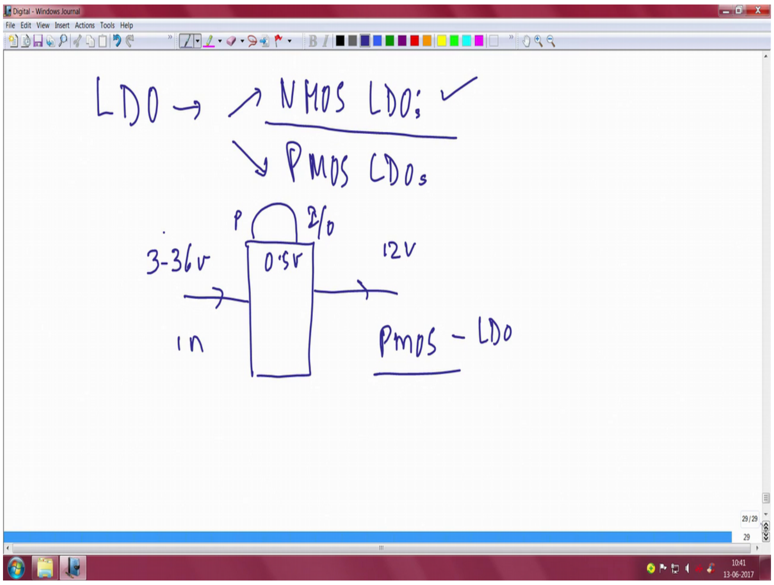

You can you can have let us say 3 to 36 volts as an input and output is also configurable. Let us say you can configure it to 12 volts and so on and so forth. If this is the kind of a configuration you can be more or less sure that this must be a PMOS based LDO. In other words, all; that means, is the series pass element is either a an n MOSFET or a p channel n channel MOSFET or a PMOS channel MOSFET, that is how it means does not mean anything else.

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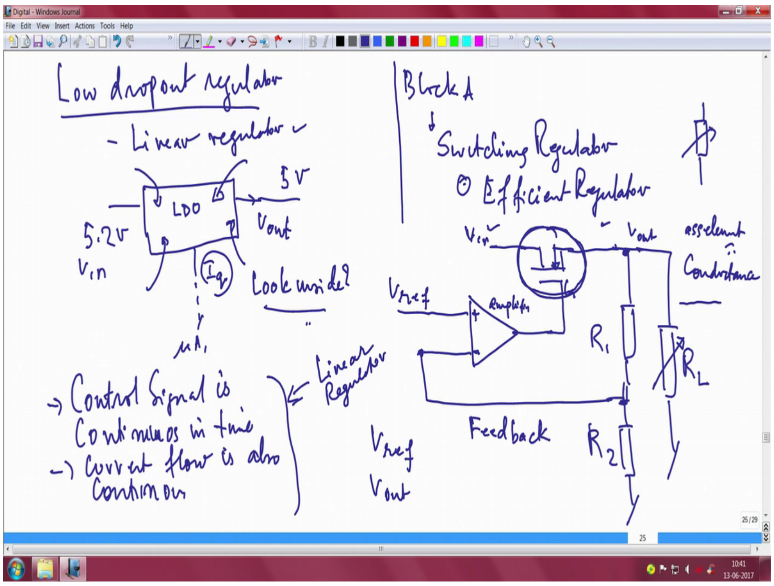

In other words, if you go back to this picture, let me re draw the picture you look at this picture here this you can see is typical of what you would call a n MOS n MOSFET series element right. So, in n MOS series element what would you do, this V in is typically connected to the drain which is V dd the output is taken from the source and the gate actually is the error amplifier output essentially is being driven by this system to in order to keep the system in regulation. So, this is typical what you would do in a n channel n MOS or n channel n MOSFET series pass element, if it is PMOS you just reverse and then build the circuit accordingly, right.

So, but you can see that whatever be the series pass element, the circuit remains the same. The external for the external viewer for the designer it continues to be the same and issues that we discuss are also the same. So, really you should not worry about whether it is n MOS or p MOS, but you should keep this in mind right. Now I must also draw your attention to this little thing I mention to you about the let me go back and show you something about I am just trying to see if I really explain that node ruptures I didnt. So, let me quickly explain that part as well. So, that will help you connect several things in this course. So, let me re draw and for convenience, let me re draw this n channel the series pass element based or n MOSFET based LDO internal circuitry, what will I do I will draw the sorry let me yeah that should define the space may be not be sufficient.

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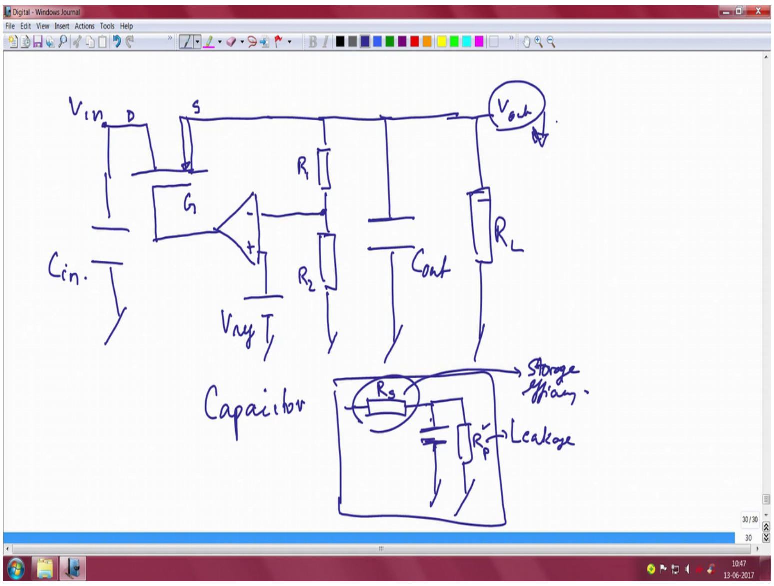

So, what I will do is, I will take a fresh sheet, and we will draw from here very good. So, I go like this right and I take the gate this is a n MOS n MOS n channel MOSFET. So, if it is an n channel MOSFET, this must be the drain this is the source and that is the gate. And what I do I need to provide the feedback. So, this is R 1 and this is R 2, this is the point where I sense and I will be connecting it to the error amplifier, to which is connected V ref right. The output actually drives the gate, what is this point V out what is this point V in and this is V ref and you can see this is a quite simple to do.

Obviously you cannot take the V out without providing without looking for the stability without adding the stability capacitor, which is very critical right and then you have the load this is R l this is C out. I also mention to you that we need an input capacitor and that is seen this C out, you have to be very careful because it is the one that provides stability to this voltage loop. In other words, if you take a capacitors equivalent electrical circuit you would put one parasitic resistor in series and one parasitic resistor in parallel right. This is providing or giving problem this is a capacitor. This is the series and this is the parallel registers these are 2 parasitics. You would not see them, but they have their effect on the performance of this capacitor.

So, what is this effect of this the effect of the series resistor is to reduce the efficiency of storage of this capacitor. And this parallel resistors problem contributed by this parallel resistor leakage right leakage is an issue with this this is giving you problem with respect to efficiency of storage efficiency takes a beating because this register drops the voltage across itself and then does not allow you to charge. So, this is the rate at which a capacitor is charged is charging will have a huge bearing on the series resistor, which is basically a parasite on the capacitor. So, it has everything to do with charging rate at which it is charging and the efficiency of charging it actually more than storage it is more about the efficiency of charging and then of course, leakage.

So, you have to choose you are trying to a regulate a V out here, and if you choose a capacitor which has a high series resistance; obviously, this is going to take a problem this is going to take a beating right. Because this is exactly what you do not want you do not want this V out you wanted to be precise accurate gave out all those specifications and it had actually meet those specifications, right.

Let us see what else you can do with that and so essentially what you are saying is that this C out register is important. So, let us move on with this n MOS and CMOS discussion series pass element discussion. See this one is being an n MOS series pass element requires at times depending on how this output voltage increases or decreases. There might be a situation where this gate voltage will have to be greater than the output voltage. Might how did actually turns out sometimes like that which means what happen.

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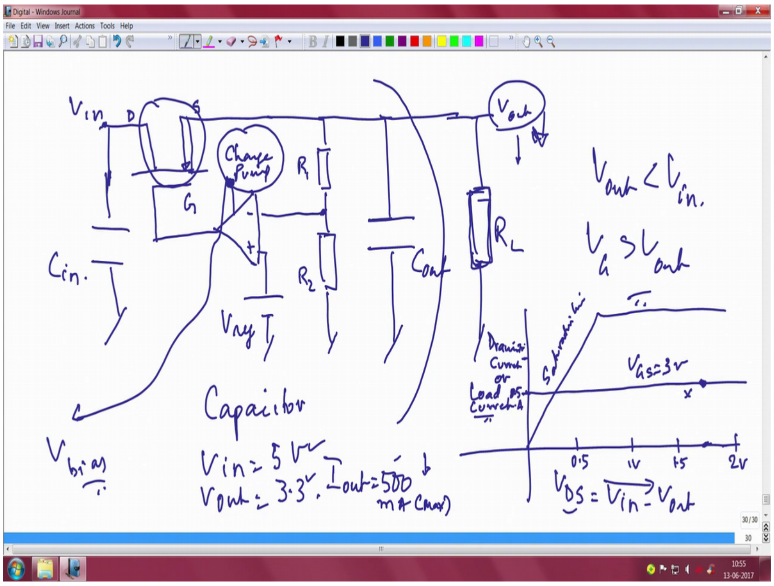

What would happen let us say the input is not the see basically the output voltage if it has to be if the gate voltage has to be greater than the output voltage. And the output voltage is lesser than the has to be always less than V out has to be always less than V in in a LDO. And you need a V G get voltage greater than sometimes V out how do you generate the situation how do you come out of the situation right. Typically, they use a charge pump or an external V bias. And some so, then and then I will have to provide this higher voltage in order to ensure that this n MOS series pass element actually works. Again you do not have to worry because all of this is actually implemented inside the chip an LDO chip, and it is of no issue for you and you do not have to really worry about, but nevertheless you should know that there can be a situation where the gate voltage has to be given higher than that of the source under certain loading conditions.

Let us go step by step and understand this is loading conditions carefully and let us see exactly how this LDO actually functions. For that what I will do is I will draw on the x axis and on the y axis, I will draw V D S I will draw V D S. And what is V D S, it is nothing, but V in minus V out right. This is V D S which is V in minus V out. And on the x y on the y axis I will show the load current. I will show the load current. So, we will say drain current nothing, but the drain current right that is nothing, but the drain current or also nothing, but the load current, so alright.

So, what would you show? I will show the saturation line. This is the saturation line essentially. And I will take an example of assume that you are interested in V in of 5 volts and V out of 3.3. 5 volts input V out is 3.3 and load current, I out is 500 mill ampere max basically right. Maximum current that this load can draw will be 500 milliamperes. Of course, it will depend on this load is always varying right it is a dynamically varying load. Sometimes you can have microcontroller sensor and all peripherals connected to it and therefore, it could be drawing a very high current sometimes only the microcontroller maybe on with all the other peripherals going down which means the current could be going down. So, it is a dynamic situation and all of that essentially means this R l is never fixed it is always changing over time. And this regulator has to ensure that this this regulator has to ensure that irrespective of what the how the load is varying it has to keep the system under high regulation.

So, if you wish to mark that point, let us say this is 0.5 this is 1 volt this is 1.5 volts and this is a 2 volts. This is the voltage that you want. So, V d s is nothing, but V in minus V out which is nothing, but the drop voltage right. The dropout voltage that is the voltage that drop should be dropped across the series element. That is the voltage that has to drop across the series element here you can see it is quite simple V 5, if V in is 5 V out is 3.3. So, V d s is nothing, but V in minus V out which is 1.7. So, 1.7 it comes somewhere here, let us say all right and now let us take drain currents let us say your 0.5 amps which is the maximum load current point comes here.

So, let me draw a line like this 1.7 comes here. I am sure you will all agree to this point now the. So, here you have a situation where the requirement is that yeah. So, you have 1.7 and this actually corresponds to the drop which is 1.7 and the maximum current which is 500 milliamperes. What you perhaps do not know is which you should actually know at this ends at this point is what is the V G S for this point to remain.

Let us put V G S has 3 volts, indeed it is 3 volts. If you put if you give a V G S of at the gate to the source between the gate and the source of 3 volts, this system will give you a drop of 1.7 volts across V D S and we will be able to give you a source, I will be able to source a current of 3 volts. Let us call this a some point let us say x right or some point here. Now take a situation where the load current increases and let us say it goes to 0.7 volts 0.7 amps. So, let me draw it for clarity again. So, that you will see the picture better this is 0.5 and let us say it goes to 0.7 right, and that is here now you do not want to.

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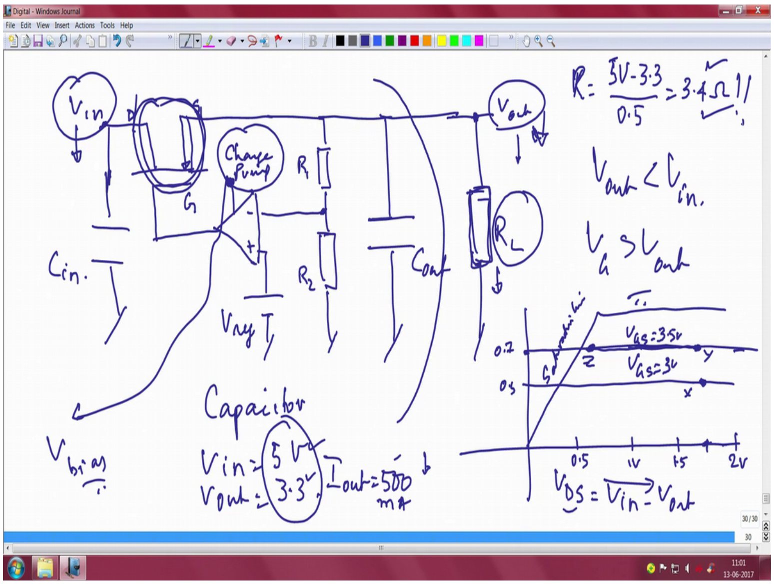

So, essentially what you have to do you this. So, this is the key here right only the load current has increased, you have to continue to maintain the same voltage drop across it, but unless you do something to ensure that the you have to do something which something essentially when they when I mean something unless you increase the V g s V g s to 3.5 volts, you will not get it back into regulation. So, you can see that unless you increase V g s the load current, a sourcing the required load current will not will not be possible. So, I think what is important here is for some reason it has I have written here 500 milliamperes max, but it is possible that for some transient condition it may even have taken. So, I will remove this word max. So, that we do not violate this discussion point here. So, this let us say is point y, this is your point y. So, that is point y.

So, here you have to give the additional V G S. So, that it actually moves. So, look carefully you have been violated this voltage drop across V d s, but you continue to keep it exactly at the 1.7 that is required. Now take another case all right you take a case where input reduces, you take a case where input reduces. If input reduces if input reduces graphically you have to keep your basically you have to if you want to keep this point in saturation, if you want to keep this point in a in regulation under the condition where V in changes, when there is a reduction in V in you want to keep this point in regulation. Unless you essentially reduce this drop you cannot do that right that is the key here, unless you reduce this drop you would not get back V out that you have planned for whatever that you wish to that you wanted to you are designed it for.

So, in other words here you can see V gs has line has remained the same only thing that the point has moved back. In other words, you have gone in the direction of reduction in V D S, this drop you are playing with this drop and let us call this point as z. So, essentially this LDO is moving from x to y to z and so on and so forth, based on either change in V in or change in any conditions at the output due to change in the output load condition let us output load conditions. Let us do some simple ohms law and demonstrate a simple concept here which will allow you to understand the whole discussion quite well.

Let us just put back these 2 things. You will see that you are drop is 5 volts at the input V out is 3.3. So, if you do if you want to calculate the resistance R this will simply be 5 volts minus, sorry it is not coming out well. So, let me write it here, let me calculate the resistance R, for some reason I want to calculate R, let us say 5 volts minus 3.3 maximum load current of 0.5 amps gives you 3.4 ohms right. You can substitute any number of values if you wish, what it means is this series pass has a resistance of 3.4 ohms nothing else.

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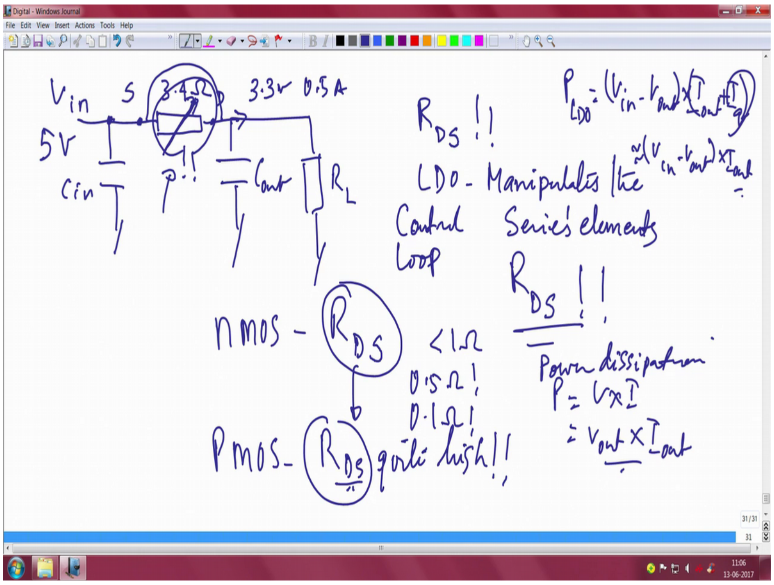

In other words, supposing hypothetically, if you replace this with a fixed 3.4 ohms register. You can give V in of 5 volts and you can take an output of 3.3 with a load current maximum load current of 0.5 amps.

Since this is not always the case, and the load continues to be changing all the time, you only need a mechanism where this resistance can also be altered at all times right. In other words this is nothing, but the source this is nothing, but the drain of a MOSFET and this change essentially is nothing, but the gate voltage that you are providing. In simple terms you need to modify the resistance between brain and the source also called the R d s. In other words, in LDO simply manipulates what LDO n d o LDOs control loop simply manipulates the series elements R D S nothing else than this, this is indeed the truth that is all I was trying to get it and if you load this. So, in other words n MOS n channel MOSFET typically has R D S very low, very low you want less than one ohm maybe 0.5 ohms maybe point one ohms and so on and so forth.

The lower the better the lower the better right you can be you will still be able to pass a lot of current with hardly any voltage drop across the device, and yet avoid and yet provide a large amount of load current. And that is why it is response is also really very good and we describe the dynamic response of an LDO in our previous discussions. So, compared to you know n MOS, PMOS or p channel MOSFET R d s is quite high quite high. That is all I we are trying to say I would not like to give any numbers because each manufacturers specifies a different values, but you have to note that essentially we are essentially trying to with all this control loop for technology, we are actually trying to vary the resistance between the drain and the source very effectively, and that is how the regulator is able to keep itself is able to provide the required assistance for us alright.

So, this is one important thing which you have to note. We can put down very simple equations for power dissipation, power dissipation power dissipation let us put it down power dissipation at the output simply is nothing, but the V out times the I out current right you can do this, and input power is of is also important, but it is quite simple it is nothing, but V in times the I in current and what is important is the power dissipation of the LDO this is very important this is nothing, but V in minus V out times I out output current nothing, but the drain current as we called it.

But please note some amount of current is also consumed quietly quiescent current for the LDO to function. So, we may want to add the quiescent current as well. So, since the quiescent current is very small you can approximate the power dissipation of an LDO as V in minus V out times the load current which is I out. So, that is a very important theme, you are if you I just to complete the discussion here you can see.

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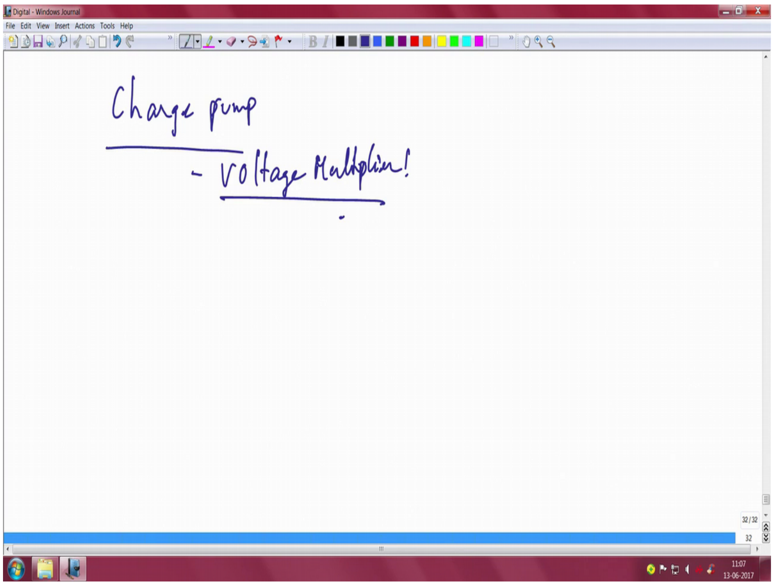

That we had to provide sometimes in order to ensure that the regulator of an n channel MOSFET is under providing a regulation, we had to provide sometimes higher voltage at the gate. And this is typically done using a charge pump charge pumps are another kind of devices which essentially are bit inside the LDO, but you can also buy them outside.

Essentially use volt is nothing, but a voltage multiplier, and so it is nothing, but a voltage multiplier and we will see how to build these for the purposes of our work at a subsequent time all right. So, this is one part of the story. The other part of the story is indeed that you may have to look at a data sheet and understand several parameters of an LDO. So, let us put down some important parameters for these LDO, and also see if we can actually conduct an experiment. Understand the experiment well and then come back and put the theory our understanding behind that experiment and then summarize everything about the LDO. I would like to stop here.