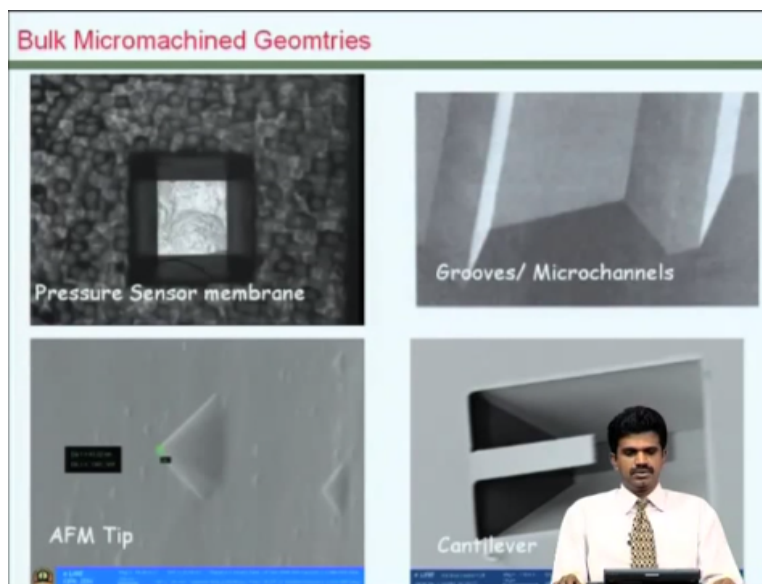


Micro and Smart Systems
Prof. K. J. Vinoy
Department of Electrical Communication Engineering
Indian Institute of Science – Bangalore

Lecture – 11
Bulk Micromachining of Microsystems

Good morning and my name is Vinoy. I will speak to you today about bulk micromachining for the fabrication of Microsystems.

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By bulk micromachining because you are basically etching into the bulk of the silicon wafer. We can form diaphragms or cavities as you see here, grooves or channels as you see here or we could even form cantilever structures like this freestanding above a large cavity. We can also suitably modify the processes required and form tips pyramidal geometries, conical geometries that could be used for applications such as AFM tips. All these are possible by bulk micromachining.

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Bulk Micromachining

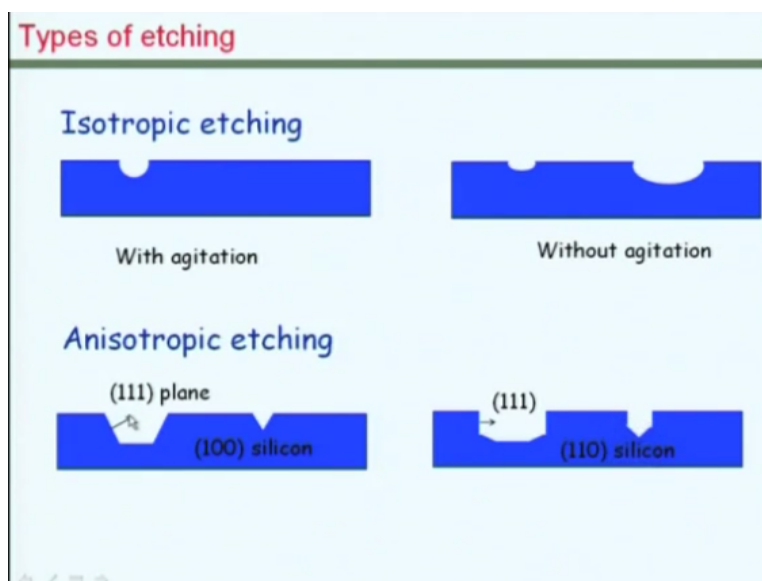
- > Microstructures formed by surface micromachining are thin.
- > For simpler fabrication of microstructures and/or to create larger vertical space around them etching into the substrate volume would be required
- > Thin diaphragms, cavities, and cantilevers can be formed by this approach.
- > In general silicon etching can be isotropic or anisotropic



Unlike in surface micromachining where the microstructures formed are very thin, we can build much larger structures, cavities, our channels by using bulk micromachine. Thin diaphragms are possible. We can even build as I have seen cantilevers by this approach. The silicon etching can be isotropic or anisotropic based on the type of reagent used. Isotropic as the name indicates would etch through whole directions of silicon irrespective of its Crystallinity.

Anisotropic etching on the other hand, we can make use of the crystal nature of the silicon and though being rotationally asymmetric to build very interesting geometries.

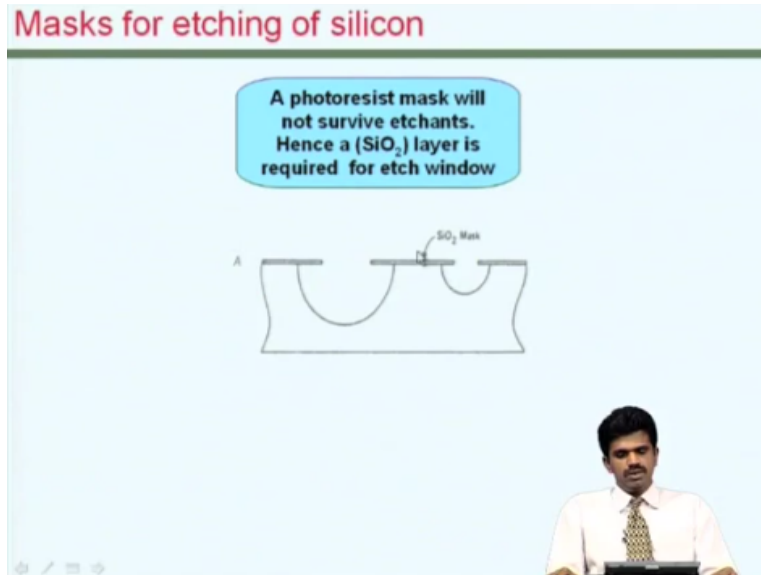
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These are explained by the geometries here. What is formed by isotropic etching are usually

irregular and depend on various process conditions. Whereas in anisotropic etching, we can choose the reagent so that it is anisotropic obviously and result in well-defined side walls to the cavities formed by etching. Depending on the silicon wafer crystallinity, the side wall could be different. We will see how and why about these a little later.

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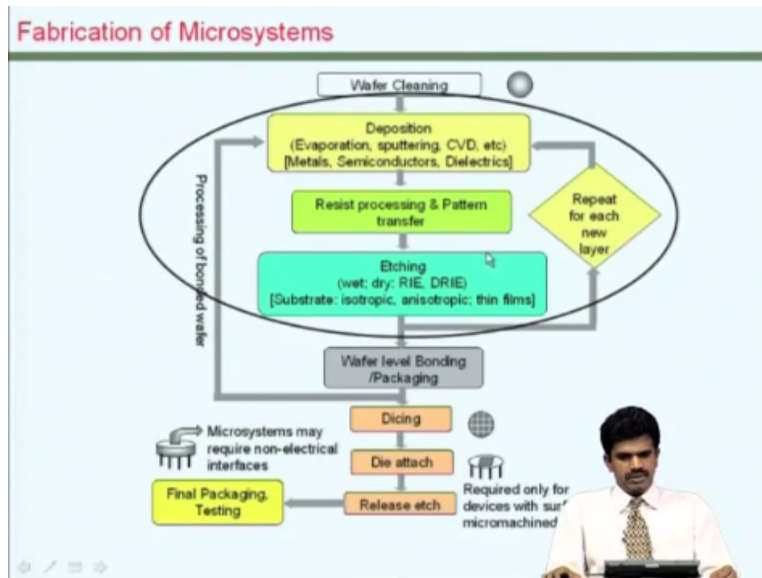


One interesting thing to note at this stage is that the mask material used for defining that etch window is not photoresist as you may have seen in order situations where thin films are etched. The etch process for thin films are fairly quick and during the etching of the thin film, the photoresist that was covering it may not have gone completely, whereas for etching silicon, more powerful etchants are required and usually for a longer time.

During that time, the resist may not sustain and hence mask layers are formed for creating etch windows. Silicon dioxide is a popular material for such mask windows. Silicon nitride is even better to function as mask window. What decides it is essentially the selectivity of the chemical that you would use for etching the silicon. So, in choosing the reagents for etching, we need to keep this aspect in mind.

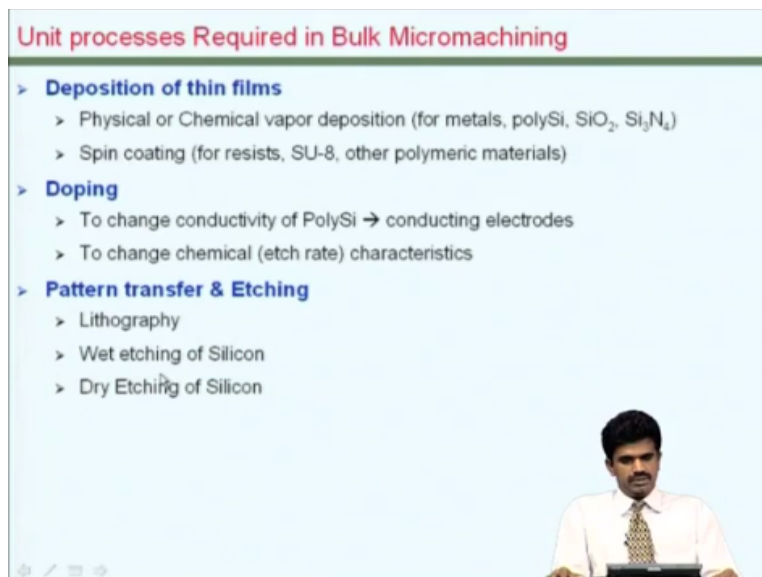
It should not, for sample, etch the mask layer or rather it should etch the mask layer far, far less than the bulk of the wafer silicon.

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Obviously, the steps involved are very similar to the overall process flow. The constituent steps include deposition pattern transfer and etch, and in this case various standard lengthened etching steps are required to form the cavities on silicon. So, the emphasis here is on etching itself.

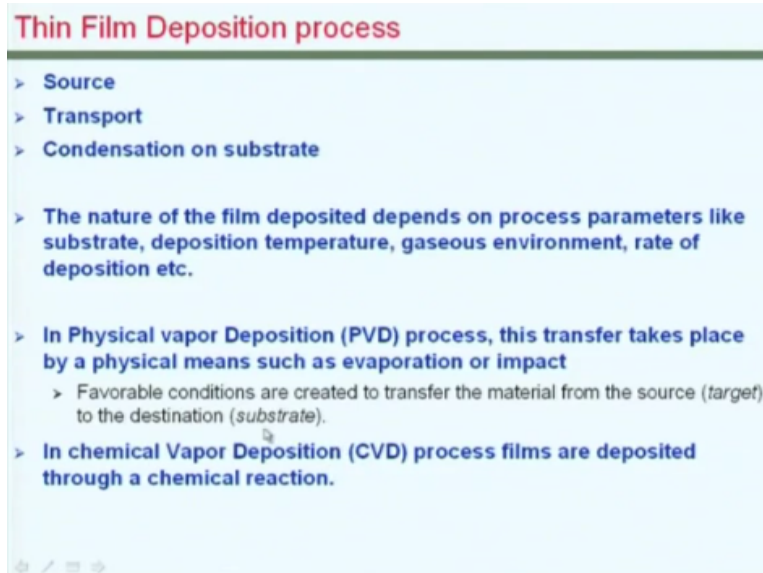
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But still all those unit processes are required for the successful completion of bulk micromachining. It obviously involves deposition of thin films as you have seen including silicon dioxide or silicon nitride. It would involve spin coating of resist or other materials. It may involve doping as you will see later to change the conductivity on the chemical activity of various layers. It would involve pattern transfer and etching.

Etching could be done using wet chemicals or even be done in the dry face. You will see many of these as we go by.

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Thin Film Deposition process

- > Source
- > Transport
- > Condensation on substrate

- > The nature of the film deposited depends on process parameters like substrate, deposition temperature, gaseous environment, rate of deposition etc.

- > In Physical vapor Deposition (PVD) process, this transfer takes place by a physical means such as evaporation or impact
 - > Favorable conditions are created to transfer the material from the source (*target*) to the destination (*substrate*).

- > In chemical Vapor Deposition (CVD) process films are deposited through a chemical reaction.

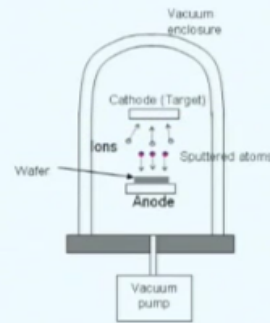
Thin film deposition process would start from a source material from which the material is transported and condensed onto the substrate material. The quality of the film will depend on various parameter, such as the substrate itself, the temperature at which it is kept, the gases that are following and the rate at which the film is deposit. There are physical techniques for deposition in which we physically transfer the atoms of the material from the target which is the source to the substrate.

We need to ensure favorable conditions for this transfer. There are techniques of deposition in which we form the film material right on the substrate after a chemical reaction. So, the reagents as the name indicates are in the gaseous form.

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Sputtering

- > **A physical phenomenon involving**
 - > The **creation of plasma** by discharge of neutral gas such as helium
 - > Acceleration of ions via a **potential gradient** and the bombardment of a 'target' or cathode
 - > Through **momentum transfer** atoms near the surface of the target metal become volatile and are transported as vapors to a substrate
 - > **Film grows** at the surface of the substrate via deposition



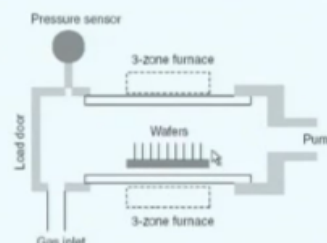
We will see these in subsequent slides. One of the physical methods is known as sputtering. In sputtering, we create a plasma with a neutral gas and these ions that are formed will hit the cathode and we keep the target at the cathode so that the incident ions would displace atoms from the target which is essentially the source material in this case and the sputtered atoms from the target would be made to deposit or stick on to the wafer which is kept at the anode.

To ensure the transfer to happen in this way, we need to make sure that these are arranged properly within a vacuum chamber. The film grows on this substrate which is kept at the anode.

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Process in CVD

- > **Mass transport of reactant (and diluent gases) in the bulk gases flow region from the reactor inlet to the deposition zone.**
- > **Gas phase reactions** leading to film precursors and by-products.
- > **Mass transport of film pre-cursors and reactants to the growth surface.**
- > **Adsorption** of film precursors and reactants on the growth surface.
- > **Mass transport of by-products in the bulk gas flow region away from the deposition zone towards the reactor exit**
- > **Types**
 - > Plasma enhanced (PECVD)
 - > Atmospheric pressure (APCVD)
 - > Low pressure (LPCVD)
 - > Very low pressure (VLCVD)
 - > Metallographic (MOCVD)



In the chemical vapor deposition on the other hand, the reactant gases are transported into the

chamber and we make sure the chemical reactions happen and the film material is essentially coming out of the precursors that are there in the carrying gases and the film which is the product of the chemical reaction that is happening in the gaseous form are absorbed onto the surface and also we need to make sure that the other by-products of the chemical reaction could be carried out in the gas flow.

There are several variants of chemical vapor deposition based on the temperature or pressure at which these reactions are carried out. As I mentioned, we need to make sure the pressure, we can ensure the temperatures and we can ensure the gas flow so that proper deposition would happen at the wafer.

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LPCVD of Si Compounds

CVD is used to form SiO_2 layers that are much thicker in relatively very short times than thermal oxides.

SiO_2 can be deposited from reacting silane and oxygen in LPCVD reactor at 300 to 500°C where


$$\text{SiH}_4 + \text{O}_2 \xrightarrow{500^\circ\text{C}} \text{SiO}_2 + 2\text{H}_2$$

SiO_2 can also be LPCVD deposited by decomposing dichlorosilane

$$\text{SiCl}_2\text{H}_2 + 2\text{H}_2\text{O} \xrightarrow{900^\circ\text{C}} \text{SiO}_2 + 2\text{H}_2 + 2\text{HCl}$$

SiO_2 can also be LPCVD deposited by from tetraethyl orthosilicate (TEOS or $\text{Si}(\text{OC}_2\text{H}_5)_4$) by vaporizing this from a liquid source.

Si_3N_4 can be LPCVD or PECVD process. In the LPCVD process, dichlorosilane and ammonia react according to the reaction

$$3\text{SiCl}_2\text{H}_2 + 4\text{NH}_3 \xrightarrow{800^\circ\text{C}} \text{Si}_3\text{N}_4 + 6\text{HCl} + 6\text{H}_2$$


It is possible to use the low pressure CVD techniques for depositing silicon dioxide from silane or from dichloro silane or even from TEOS. It is possible to deposit the silicon nitride by either LPCVD or PECVD technique. One needs to ensure the process conditions which are the temperatures and pressures appropriately so that the film growth could be controlled. As I mentioned, silicon dioxide and silicon nitride are useful as the masking material in bulk micromachine.

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Pattern Transfer Techniques

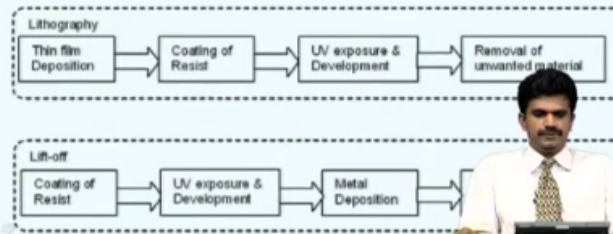
> In Lithography

> Resist coating → Spin coating → Soft baking → UV exposure → Development → Post baking → Etching of thin film → Resist stripping

> In lift off process a photoresist pattern is generated initially on the substrate instead of etching the unwanted material.

> The basic criterion for the lift off technique is that the thickness of deposited film should be significantly less than that of the photoresist and the developed patterns have vertical side walls.

> Metal layers with high resolution can be patterned using lift off technique. Metals such as gold (which can be etched with aqua regia) can be patterned with simple processes by lift off.



Pattern transfer can be done using Lithography or lift off techniques. In Lithography, we deposit the thin film first and on top of that, we put the resist by spin coating which is soft baked and exposed to UV beam developed and after one more baking stage so that the resist would stick to the surface where one can etch the thin film, after which if required the resist can be stripped off. Recall, once again this is etching the thin film this approach. To etch the silicon, we may want to keep the remaining thin film as the etch window.

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Etching of thin films

> Silicon Nitride etching

- > 1%HF → 60nm/min
- > 10%HF → 500nm/min
- > H_3PO_4 → 10nm/min (180C)

> Silicon Dioxide Etching

- > Buffered HF → 100-250nm/min
- > HF (very fast)

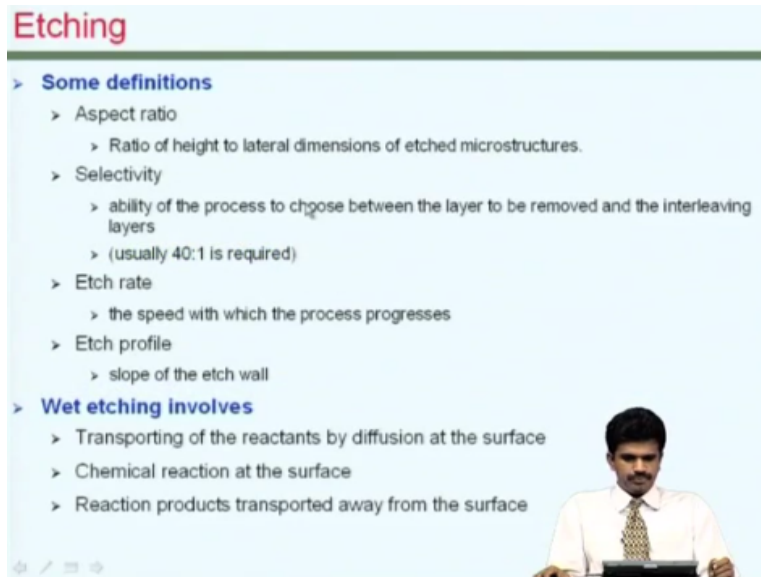
> Etch rates depends on how the film was deposited (film quality)



Etching of thin films of silicon nitride can be done usually using phosphoric acid. Silicon dioxide can be done using the etch of solutions. It may appear that the silicon nitride has lower or comparable etch rate as silicon dioxide, but it so happens that the nitrate films are usually thinner

and hence would work far better in the context of silicon etching.

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Etching

- > **Some definitions**
 - > Aspect ratio
 - > Ratio of height to lateral dimensions of etched microstructures.
 - > Selectivity
 - > ability of the process to choose between the layer to be removed and the interleaving layers
 - > (usually 40:1 is required)
 - > Etch rate
 - > the speed with which the process progresses
 - > Etch profile
 - > slope of the etch wall
- > **Wet etching involves**
 - > Transporting of the reactants by diffusion at the surface
 - > Chemical reaction at the surface
 - > Reaction products transported away from the surface

The slide also features a small inset image of a man in a white shirt and tie sitting at a desk with a laptop.

The etch characteristics are defined based on various parameters. Aspect ratio is the ratio of height to either of the lateral dimensions of the final microstructure. Etch selectivity is the ability of the process to choose between various material layers. The example that you have seen in the beginning, it is essentially the selectivity between silicon and silicon dioxide. Unless there is a large selectivity, the etchant could act as an O₂ and once that is gone the structural definition itself will be lost.

Hence, a high selectivity is usually required. Etch rate is obviously the speed at which the desired material is removed by the etchant. Etch profile is the slope or the angle of the side walls after the structure or geometry is formed by etching. Wet etching involves transporting of the reagents and some kind of chemical reaction and removal of the products of this chemical reaction, that is how we make the wet etching to happen.

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Isotropic etching

- > **Use acidic etchants**
 - > Rounded patterns formed
- > **Used for**
 - > Rounding of sharp edges (formed by anisotropic etching) to avoid stress concentrations
 - > Removing roughness after dry/anisotropic etching
 - > Thinning→ For creating structures / planar surfaces on single crystal Silicon
 - > Patterning single crystal , poly crystalline or amorphous films
 - > Delineation of electrical junctions and defect evaluation



As I mentioned, one of the simplest thing to imagine would be the isotropic etching usually done by using acidic etchants and results in rounded patterns as you could see from here and these shapes are usually unpredictable and depends largely on the agitation and various other process parameters. Isotropic etching is also used when rounding of sharp edges are actually required. This is typically required to avoid stress concentrations.

Isotropic etching can also be performed for removing surface roughness. It is useful when one would want to thin the substrate beforehand. It is useful even in patterning amorphous films or even poly crystalline and silicon films. There are several instances in which isotropic etching is really required and useful.

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Iso etching...

- > **Difficulties in isotropic etching**
 - > Masking.
 - > Etch rate is agitation and temperature sensitive,
 - > Difficult to control lateral and vertical etch rates
- > **Wet etchants for electronics materials**

Material	Etchant	Etch rate (Å/min)
Si	3ml HF+5ml HNO ₃ + 3ml CH ₃ COOH	3.5x10 ⁵
GaAs	8ml H ₂ SO ₄ +1ml H ₂ O ₂ +1ml H ₂ O	0.8x10 ⁵
SiO ₂	28ml HF + 170ml H ₂ O + 113g NH ₄ F 15ml HF + 10ml HNO ₃ + 300ml H ₂ O	1000 120
Si ₃ N ₄	Buffered HF H ₃ PO ₄	5 100
Al	1ml HNO ₃ + 4ml CH ₃ COOH + 4ml H ₃ PO ₄ + 1ml H ₂ O	350
Au	4g KI + 1g I ₂ + 40ml H ₂ O	1x10 ⁵
Cu	FeCl ₃	

There are challenges in choosing the right etchants for various materials. The etch rates and most favorable solutions for etching of some of the materials used in micro-machining are listed in this table.

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Anisotropic etching of Silicon

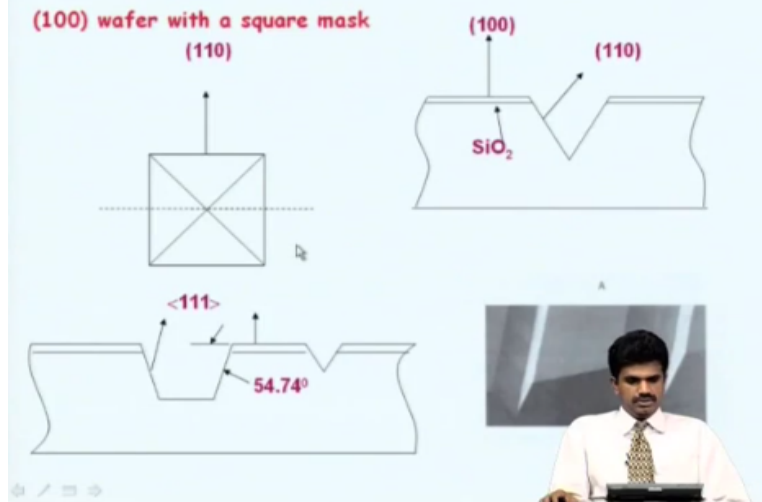
- > Anisotropic etching means different etch rates in different directions in the material (e.g., Crystalline Si)

The diagram illustrates two etching profiles. On the left, 'Anisotropic' etching results in a sharp, rectangular profile with a 'Slow etching crystal plane' and an 'Etch mask'. On the right, 'Isotropic' etching results in a rounded, undercut profile.

Anisotropic etching on the other hand make use of the crystalline nature of silicon in realising well defined geometry. As see from here compared to the isotropic etching which results in rounded geometries and also what is known as undercut which is essentially etching beneath the etch mask geometry. In anisotropic etching, if the geometries are decided well, we can ensure that there is minimal or no undercut and a continuous plane which would form the etch profile.

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Anisotropically etched features



Let us see how this is done in more detail. Depending on the width of the etch window and depending on the duration of the etch we can have either a V-shaped or a wider-shaped cavities, why is it so. It so happens if on a 100 wafer, if you align these rectangular windows properly, the plane that is formed at an angle is 111 plane and in atom in 111 plane of silicon structure are strongly bonded to those underneath them and hence are extremely difficult to be displaced by many reagents.

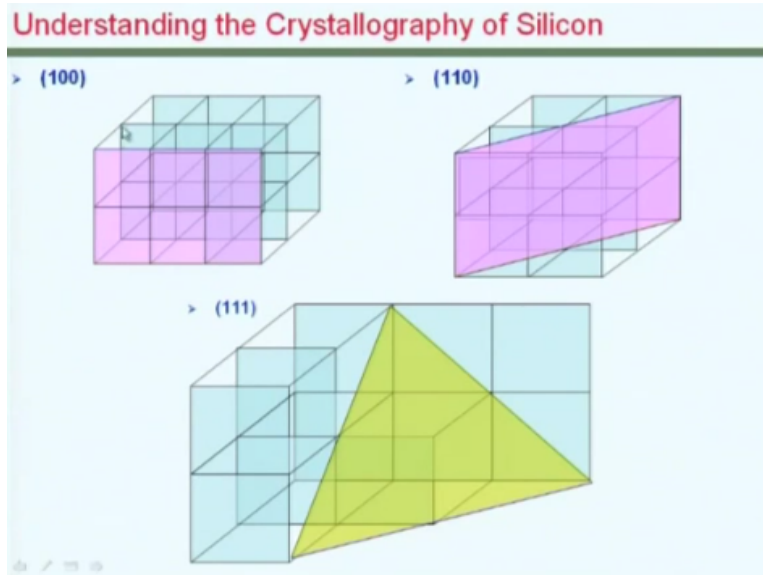
We essentially exploit this feature to build such microstructures cavities with regular well-defined geometries. How does it form. Once this window is defined as chemical reaction begin, we get the top surface to be removed but the last atom over here which would eventually belong to this 111 plane is very strongly bonded by atoms beneath it. So, it would be difficult to remove this atom here and on this side.

So, hence what you would get would be an etched surface but with the atom right beneath the etch window strongly bonded inward and this process would continue and the next 111 atom would be slightly displaced and this atom also would be strongly bonded to the atoms beneath that. Hence as the etching process continues, this plane gets defined and the etch floor would go down but the sidewalls would not remain vertical or inward curved.

Rather it would remain as a continuation of the 111 plane starting from the etch window opening.

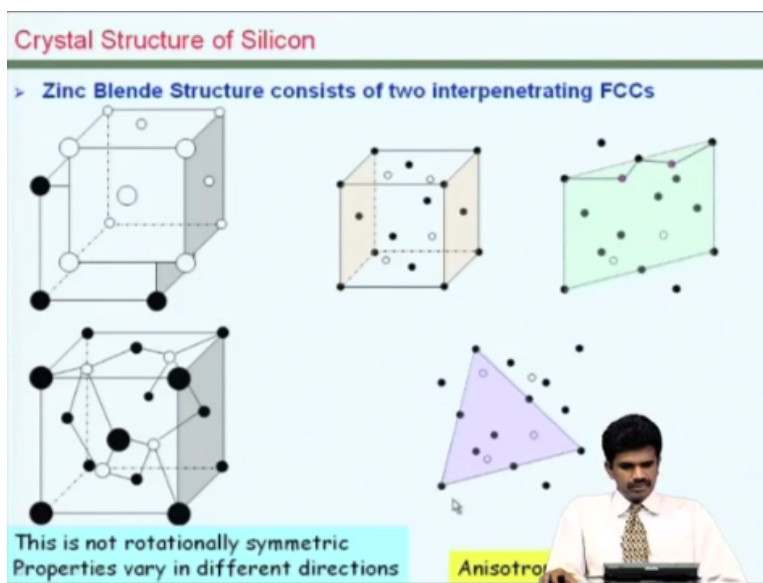
This obviously is particular about 100 wafer.

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For a quick overview, we can look at how Crystalline structures are defined. 100 surfaces are in which the wafer surface is aligned to any of coordinate directions with respect to the lattice arrangement. In 110, the surface is diagonal with respect to 2 of the axes whereas parallel with respect to one of the third. In 111, the surface of the crystal or the resulting plane is inclined with respect to all the 3 crystal directions.

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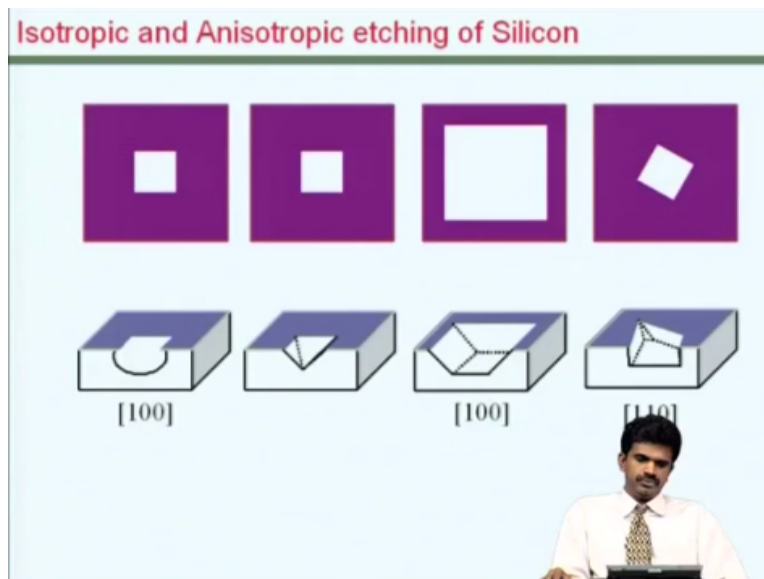
In the context of the silicon wafer which is essentially a zinc blende structure consisting of 2 interpenetrating FCCs. If you recall, this is 1-unit cell of that with dimension here which is the

single lattice constant and if you look at the various crystal planes in the 100 plane within a square of lattice constant A, we have all these 5 atoms which are essentially the FCC atoms. In the case of 110 plane which is shown here with light green colour.

We have all these atoms marked with this line on the surface, whereas all the other isolated atoms of the unit cell are off from the plane of this surface. Similarly, in a 111 plane from the unit cell, these 6 atoms are on the surface. These 6 atoms are very strongly bonded to atoms close to them underneath within the unit cell. Hence the structure of the silicon is not rotationally isotropic and the properties are different.

As you have seen here, once you hit this 111 plane, all the atoms are bonded very strongly to those below them and hence are difficult to be displaced. Hence, we get a smooth continuous plane if the etch window is aligned properly.

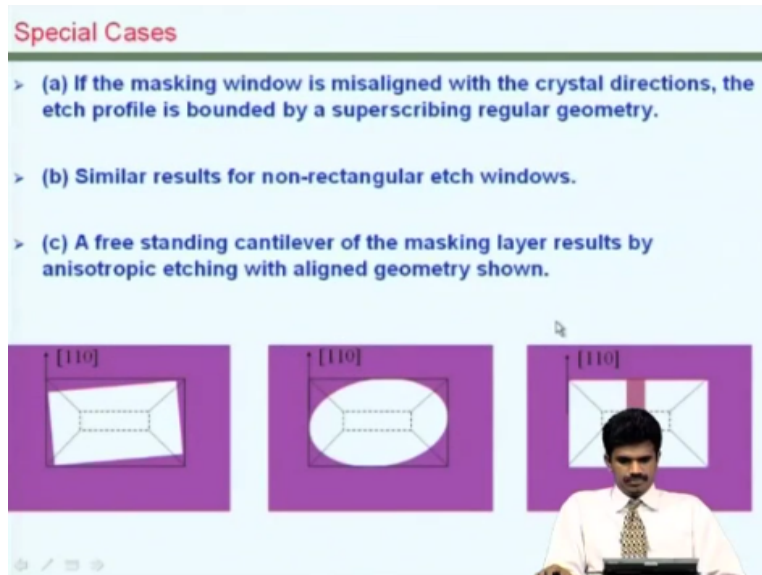
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So, unlike the rounded profile that is formed in isotropic etching. In anisotropic etching depending on the coverage area of the etch window, we can get that pyramidal shape or a truncated pyramidal shape, both these are for 100 wafers. Whereas in a 110 wafer, it is possible to have a vertical side wall and these side walls are also at the 111 plane. So, all these will depend on the relative alignment of various directions.

Hence we need to choose the window aligned with respect to the crystal orientation.

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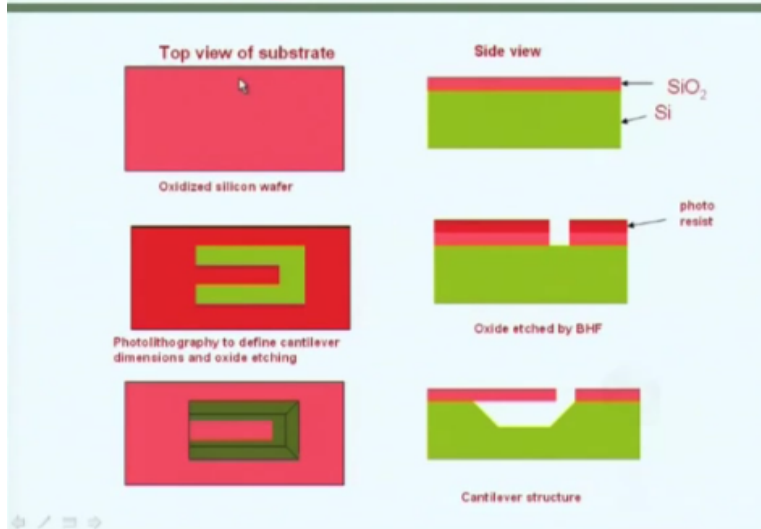


For example, if the etch window is off from the crystal directions, as you see in the figure on the left. If there is a slight angle, what would happen is we will get a rectangular truncated pyramid in this case but the base of it will not be aligned with respect to the etch window itself. Rather it will be a super-scribing rectangle from the etch window, and we can extend this and state that that when the etch window is not rectangular, it would still be a truncated pyramid with rectangle base, not a circular base even if the etch window is circular or elliptical.

This is important to remember. The part of this could still remain and we can extend what we said here to build freestanding structures like this in silicon by micromachine. Obviously what happens here can be explained in subsequent slides how we can actually such freestanding geometries.

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Bulk micromachining for a cantilever



What happens while etching is that when we form this surface, let us say we use oxide as the etch window film and create this cavity, the hole here in the etch window but as etch progresses what would happen is that 111 plane will get formed here as well as here. It will get formed here, it may get formed here, here on this side as well as on the side below the protruding parts. But the diagonal line here from this convex etch, the atoms on that side will not be as stable.

Because only if the plane is infinitely covered or entirely covered, the atoms are stable. In this corner, the atoms belonging to this plane or this plane are partially covered and hence these corners will get attacked and if you left it for long enough there will be undercut and this structure can remain freestanding at the end of the etch process. This is successfully utilised in realising cantilever arrays or cantilevered geometries.

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Cantilevers formed by Bulk etching




So, what is critical is that these edges are aligned with respect to the 110 directions on the surface of the silicon wafer. So, this gives you significant reason in aligning the geometries with respect to the crystal orientation of the silicon wafer.

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Anisotropic Etchants

- > Alkaline aqueous solutions of KOH, NaOH, LiOH,.... NH₄OH
- > Alkaline organics, Ethylene di amine, chorine, hydrazine
- > Performance of common Etchants
 - > KOH (Most popular)
 - > Use near saturated solution (1:1 in water) at 80°C.
 - > Selectivity with SiO₂ is not very good.
 - > KOH is incompatible with IC fabrication process , since it attacks Al bond pads.
 - > It can cause blindness if gets into contact with eyes
 - > Selectivity with silicon dioxide - 400:1 For KOH
 - > EDP –Ethylene diamine pyrocatechol +water
 - > Masking SiO₂, Si₃N₄, Au, Cr, Ag
 - > Selectivity with SiO₂ - 5000:1
- > Issues in anisotropic bulk micromachining
 - > Extensive real estate consumption
 - > Large area wasted between devices
 - > Device becomes fragile



Etchants used in an isotropic etching are usually alkaline aqueous solutions. KOH is by far the most popular material and it has reasonable selectivity with SiO₂, better with silicon nitride. The selectivity with silicon dioxide is of the order of 400:1. Another chemical which is used for etching silicon is known as EDP (ethylenediamine pyrocatechol) which is aqueous solution of this.

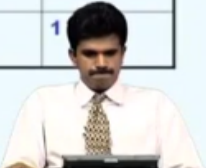
In this case, various materials could be used as the masking layer and higher selectivity is possible for etching silicon. There are some basic issues in anisotropic etching, bulk micro-machining of silicon. Because of the slanted sidewalls, larger real stage, larger area is required to form a cavity. This angle is predefined based on crystal directions and as you may have noticed is at an angle of 54.3 degrees with respect to the surface of the wafer.

Hence for large area geometries even larger area are wasted on the wafer and this can potentially make the wafer fragile.

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Anisotropic etching Silicon

Etchant	Temperature	Etch rate		
		<100>	<110>	<111>
KOH:H ₂ O	80	66	132	0.33
KOH	75	25-42	39-66	0.5
EDP	110	51	57	1.25
N ₂ H ₄ :H ₂ O	118	176	99	11
NH ₄ OH	75	24	8	1

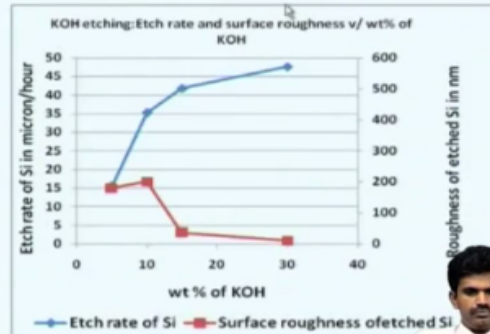


What you see here is the etch selectivity with respect to various crystal directions of silicon when we use various re-etchants agents for the bulk etching. One needs to choose the right one so that a significant difference exist between the 111 direction and the other directions.

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Etch variation

- > Silicon etch rate and etched Si surface roughness v/s concentration of KOH solution and Iso Propyl Alcohol at 75 C and 900 RPM, stirring rate.



There could be variations based on the composition of the chemical used, the temperature and also the agitation. These variations are usually predictable as long as these parameters are kept within control and hence the anisotropic etching is usually predictable for the overall geometries required.

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Selection of Silicon Crystal Orientation

(100) Oriented Si	(110) Oriented Si
Inward sloping walls (54.74°)	Vertical (1 1 1) walls
The sloping walls cause a lot of lost real estate	Narrow trenches with high aspect ratio are possible
Flat bottom parallel to surface is ideal for membrane fabrication	Multifaceted cavity bottom ((110) and (100) planes) makes for a poor diaphragm
Bridges perpendicular to a V-groove bound by (111) planes cannot be undercut	Bridges perpendicular to a V-groove bound by (111) planes can be undercut
Shape and orientation of diaphragms convenient and simple to design	Shape and orientation of diaphragms awkward and more difficult to design
Diaphragm size, bounded by nonetching (111) planes, is relatively easy to control	Diaphragm size is difficult to control <100> edges are not defined by nonetching

As we have seen depending on whether 100 oriented wafer or 111 wafer is used, different types of sidewalls are possible. In 110 wafers, many of the sidewalls could be vertical. If you recall, it is not possible to form vertical directions from all the 4 sides of the cavity in a 110 wafer. You can only make 2 of the sidewalls vertical and there will be some facets on the other side and when you need a long vertical sidewall channel, one can look at the possibility of using 110

wafers for that purpose.

As you may note, the sloping sidewalls can cause some inefficient utilisation of the surface area. We can get nearly flat surface on the bottom floor after etching in 100. The multifaceted nature of the 2 opposite sides in 110 can cause floors which are not parallel to the top surface when etched using 110 wafers. Several interesting geometries as you have seen could be formed using 100 wafer.

We can have diaphragms; we can have small cantilevers formed in 100 wafers. It is difficult to form such geometries with 110 oriented silicon.

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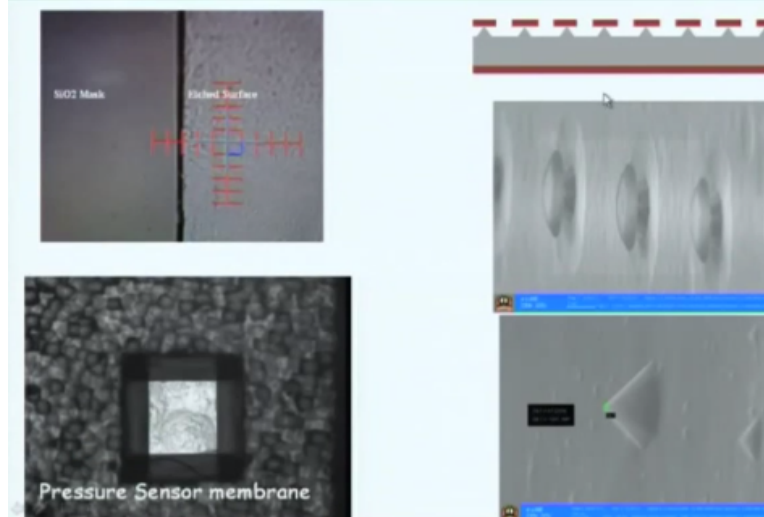
Silicon etching

	HF:HNO ₃ :CH ₃ COOH	KOH	Ethylene diamine pyrochatechol (EDP)	(CH ₃) ₂ NOH (TMAH)	SF ₆	SF ₆ /C ₄ F ₈ (DRIE)
Type	Wet	Wet	Wet	Wet	Plasma	Plasma
Anisotropic	No	Yes	Yes	Yes	varies	Yes
Rate (µm/min)	1-20	0.5-2	0.75	0.5-1.5	0.1-0.5	1-3
(111):(100) selectivity	None	100:1	35:1	50:1	None	None
Nitride etch	Low	<1	0.1	<0.1	200	200
SiO ₂ etch (nm/min)	10-30	10	0.2	<0.1	10	10
P ⁺⁺ etch stop	No	Yes	Yes	Yes	No	No
hazard			high			

So as I mentioned previously, based on the etch conditions, the etch speeds and also the directionality, the suitable chemicals can be identified chemicals can be identified for building geometries.

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Images of Etched geometries



What you see here is cavity formed below the diaphragm of a pressure sensor. In a pressure sensor, these diaphragms are stretched when pressure is applied. So, it has to be uniform and thin. So we can do this by etching from the other side and by having these regular sidewalls which is feature of an isotropic etching. We can have a predictable surface for the cavity. As you could see from here, the etched surface is inclined with respect to the silicon dioxide mask which is largely unaffected in many practical situations.

What you see here is one interesting geometry that could be formed by bulk etching. When we have this small windows and we start using isotropic etching, there will be undercuts and as these undercuts if the etch window dimensions are controlled properly, at the end of etch process there is the oxide that is remaining and there is significant undercuts. If you remove this oxide, we get nice conical geometries and as I mentioned these could be used for tips such as in atomic force microscopy.

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Etch stop technique

> Etch stop is a region at which the wet etching slows down

> Dopant selective etching (DSE)

- > Technique is useful for heavily doped layers, leaving behind lightly doped
- > Advantages of DSE
 - > Independent of crystal orientation
 - > Smooth surface finish
 - > Offers possibilities for fabricating release structures with arbitrary lateral geometry
- > Disadvantages
 - > High boron conc. introduces mechanical stress into the material

Etchant (Diluent)	Temp. (°C)	(100) Etch-rate (µm/min) for boron doping $\ll 10^{19} \text{cm}^{-3}$	Etch-rate (µm/min) for boron doping $\sim 10^{20} \text{cm}^{-3}$
EDP (H ₂ O)	115	0.75	0.015
KOH (H ₂ O)	85	1.4	0.07
NaOH (H ₂ O)	65	0.25-1.0	0.02

An important thing to note in the context of etching of silicon is about stopping of the etch process, especially in the context of the diaphragm that you have seen you need to have a precise control where the etch process gets stopped. It is difficult to time the etch process so that you dig through this 500 micron of silicon if you are using a low diameter substrate wafer and finish the process to leave a 5 or 10 micron thick diaphragm.

Hence, alternate ways of stopping the etch process is required in these cases. One of the popular approach is based on doping the wafer appropriately. In doping what we do is we introduce impurities and in a controlled fashion drive these in to the required depth and hence there could be a significant variation in the etch rates based on the doping concentration. So as you could see here when there is 10 to 20 per cm cube concentration, the etch rate drops to 0.15 micrometer per min compared to 0.75 when the concentration is far less.

So, the etch rate would be significantly lower when EDP or KOH or even sodium hydroxide aqueous solutions of these are used for etching silicon. This feature can therefore be utilized for realising a flat uniform thickness membrane, for example, for pressure sensor applications.

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Doped regions

- > For doping of semiconductors, controlled quantities of impurity atoms are introduced into the selected regions of the surface through masks on the top of the wafer.
- > Diffusion and Ion implantation are common methods for this.
- > Used as etch stop layers
- > N and P regions can be formed for active semiconductors
- > Diffusion
 - > Wafer placed in a high temp furnace and a carrier gas is passed. Boron and phosphorus are commonly used dopants
 - > The deposited wafer is heated in a furnace for drive in, oxidising or inert gas to redistribute dopants in the wafer to desired depth
 - > Silicon dioxide is used as the masking layer

Phosphorus Diffusion

Make	Tempress
Temperature Range	800-1200 °C
Dopant Source	POCl ₃
Bubbler Gas	Nitrogen (0.4hr/min)
Carrier Gas	Nitrogen (4 ltr/min)
Flow rate of Oxygen	0.6 l/min

Boron Diffusion

Make	Tempress
Temperature Range	900-1200 °C
Dopant Source	Boron Nitride Disc
Process Ambient	Nitrogen
Flow rate of N ₂	4 ltr/min

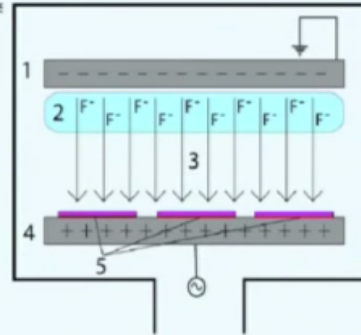
As I mentioned, this would require doping. One of the approaches is based on what is known as diffusion. In diffusion as in ion implantation what is done is that we introduce N and P type materials on to the semiconductor. In diffusion, the wafer is placed in a high temperature furnace and a carrier gas is used which is usually nitrogen to transport boron or phosphorus from the respective source material onto the surface of the wafer.

After this is deposited on to the wafer, these are driven in by keeping it once again at a high temperature with a gas flow. So, we can dope the desired thickness of the semiconductor by suitably choosing the process conditions. We select, the region where it is getting doped by using mask layers typically silicon dioxide could be used for that purpose.

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Dry Etching Techniques

- > **Material removal for IC's , MEMS**
 - > By physical
 - > By ion bombardment
 - > By chemical
 - > Chemical reaction through a reactive gas
 - > Or Combination
- > **Plasma etch**



For the successful realisation of micromachining, often dry etching techniques are performed. Dry etching is similar in principle to the sputtering technique that you have seen in the context of deposition. In sputtering if you recall, the ions from the plasma are made to hit the cathode where the target was kept that causes the atoms to get displaced from the target. In the case of etching what we do is instead of the target, we keep the wafer at the cathode.

So, these incident ions would displace atoms from the surface of the wafer. It could be a physical phenomena if you are only looking at ion bombardment but if reactive ions are used, obviously there could be selectivity and a chemical phenomena could be happening. So, there are several variants of dry etch possible and are utilized in micromachining of various microstructures.

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Dry Etching vs Wet Etching

- | | |
|---|--|
| <ul style="list-style-type: none">> Wet Etching> No expensive equipment required> Corrosive Acids or alkalies used> Waste products are also corrosive> Difficult to automate> Limitations in the aspect ratio for vertical structures | <ul style="list-style-type: none">> Dry Etching> Carried out in plasma reactor> Safe non-toxic gases, e.g. O_2 & CF_4 used> Waste products are easily discharged> Ease of automation> Extended processes for high aspect ratio |
|---|--|

Compared to wet etching, this kind of dry etching is usually far more expensive. We need to carry out these reactions in a plasma reactor which obviously at the low pressure and hence all the additional equipment required for that purpose. We use corrosive acids and alkalies for that etching whereas we can live with oxygen, carbon tetra fluoride and other non-toxic gases for etching in the dry phase.

It is easy to discharge the waste products in the case of dry etching and it is easy to automate and hence dry etching is usually preferred in the industry even though it is more expensive. Extended processes are required for high aspect ratio geometries. In wet etching, if you recall when you start with 100 wafers, the aspect ratio is very limited and there is always wastage of wafer surface.

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Etching Mechanisms in Plasma

(a) Sputtering

- > Physical removal of Si
- > Very good anisotropy
- > Poor selectivity

(b) Chemical Etching

- > Gas phase species react with Si to form volatile product
- > Very good selectivity
- > Poor anisotropy

Let us look at the various mechanisms that are possible in plasma etching. If you look at the simple physical removal where only the ion bombardment could be used, there is a chance that it is very poorly selected. If you only look at the chemical reactions for the removal of material, it could happen that it is an isotropic.

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Etching Mechanisms in Plasma

(c) Energetic ion-enhanced etching

- > Impinging ions damage surface, increasing reactivity (Cl_2 etching of undoped Si)
- > Good selectivity & anisotropy

(d) Inhibitor ion-enhanced etching

- > Requires two different species –etchants (Cl_2) and inhibitors (C_2F_4)
- > Very good selectivity and anisotropy

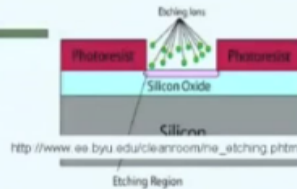
So, we need to have properly energized ions for good selectivity and anisotropy in realizing structures with well-defined profiles. Yet it may become a problem when you want to dig deep into the surface of, dig into the bulk of the wafer. It often requires attaching inhibitors, so that we can have a directionality in going deep into the wafer for deep structures with high aspect ratio.

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Reactive Ion Etching (RIE)

- > Wet etching causes undercut
- > Unidirectional etching is possible with RIE
- > High fidelity pattern transfer
- > **Steps involved in RIE Etching**

1. Reactive etching species are generated by electron/molecule collisions
2. Etchant species diffuse through stagnant region to the surface of the film to be etched
3. Etchant species adsorb onto surface
4. Reaction takes place
5. Etched product desorbs from the surface
6. Etch products diffuse back into bulk gas and removed by vacuum



Material Being Etched	Etching Chemistry
Deep Si trench	HBr/NF ₃ O ₂ /SF ₆
Shallow Si trench	HBr/Cl ₂ O ₂
Poly Si	HBr/Cl ₂ O ₂ , HBr/O ₂ , BCl ₃ /Cl ₂ , SF ₆
Al	BCl ₃ /Cl ₂ , SiCl ₄ /Cl ₂ , HBr/Cl ₂
AlSiCu	BCl ₃ /Cl ₂ /N ₂
W	SF ₆ only, NF ₃ /Cl ₂
TiW	SF ₆ only
WSi ₂ , TiSi ₂ , CoSi ₂	CCl ₂ F ₂ /NF ₃ , CF ₄ /Cl ₂ , Cl ₂ /N ₂ /C ₂ F ₆
SiO ₂	CF ₄ /CHF ₃ /Ar, C ₂ F ₆ , C ₃ F ₈ , C ₄ F ₈ /CO, C ₃ F ₈ , CH ₂ F ₂
Si ₃ N ₄	CHF ₃ /O ₂ , CH ₂ F ₂ , Cl ₂ /CHF ₃

Table taken from: *Semiconductor Devices - Physics and Technology* by S. M. Sze (pg. 440)

As I mentioned, in reactive ion etching what we have is that we properly choose the ions in the plasma so that these react with only the desired material on the wafer. This can be used for pattern in thin films and low-aspect ratio geometries on silicon. Various materials could be patterned by suitably choosing the etch chemistry and the materials used or the gases used within the chamber.

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Deep Reactive Ion Etching

- > High aspect ratio, deep trench silicon etching process.
- > The principle of the deep trench silicon etching process is an alternating fluorine based etching and passivation of the structures.
- > Masking layers can be made of photo resist or silicon oxide.
- > The main benefits of the DRIE are:
 - > etch rate of up to 6 μm/min
 - > aspect ratio up to 40:1
 - > selectivity to positive resist > 75:1
 - > selectivity to silicon oxide > 150:1
 - > etch depth capability 10 to 550 μm (through wafer etching)
 - > sidewall profile 90° ± 1°
 - > feature size 1 to >500 μm

For deep etching of silicon, for forming high aspect ratio geometries, processes known as deep reactive ion etching is required. In this case, what is done usually is that we remove material partially and then do a round of deposition scheme in which the sidewalls would get coated with something like a nonstick surface, so that a subsequent etching when the atoms get displaced,


they do not go and stick to the sidewalls. Rather they come out of the cavities.

Hence, it is possible to realized high aspect ratio geometries on silicon using deep reactive ion etching. Truly vertical sidewalls with very fine feature sizes are possible using this approach.

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Deep Reactive Ion Etching (DRIE)

- > Process alternates between etching and polymer deposition
- > SF_6/Ar used for etching
- > CHF_3/Ar used for polymerization
- > Selectivities: photoresist(100:1), SiO_2 (200:1)
- > Aspect ratio up to 30:1(sidewall angle $90\pm 2^\circ$)
- > Etch rates of 2 to $3\mu\text{m}/\text{min}$

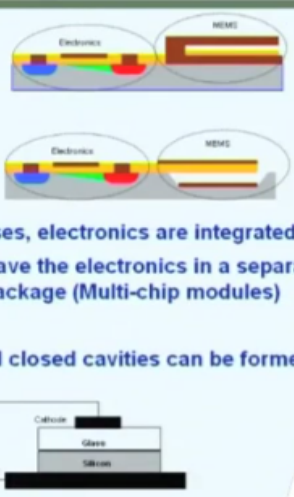


As I mentioned in this, we can use various combination of gases for etching various materials. We also use a step in which the sidewalls are coated with a kind of nonstick polymeric surface. It may go away after sometime, so these removal and attachment processes are cycled, so that high aspect ratio structures are possible.


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Integration with Electronics

- > CMOS First
- > MEMS First
- > Notice that in both cases, electronics are integrated on chip
- > It is also possible to have the electronics in a separate die and integrate these on a package (Multi-chip modules)
- > Thicker structures and closed cavities can be formed by **Wafer bonding techniques**

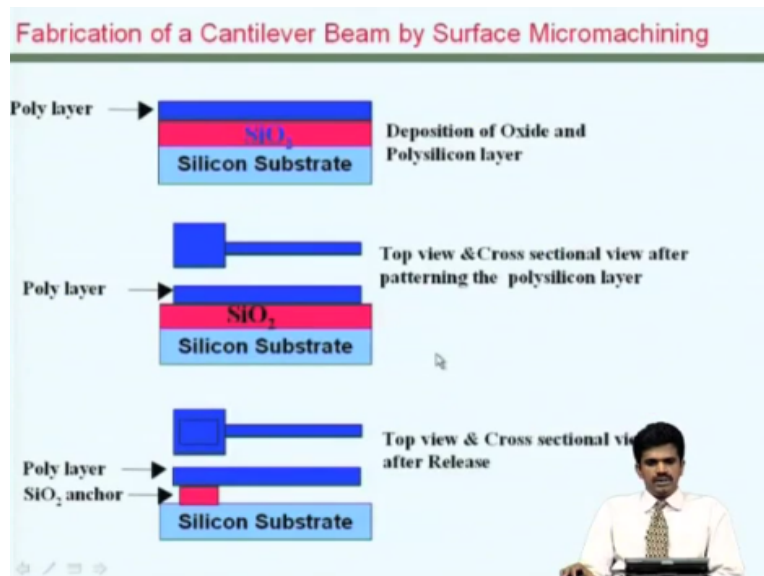


The diagrams illustrate two integration approaches: 'CMOS First' and 'MEMS First'. In 'CMOS First', the electronics are fabricated first, followed by the MEMS structures. In 'MEMS First', the MEMS structures are fabricated first, followed by the electronics. The wafer bonding schematic shows a cross-section of a wafer with layers labeled Cathode, Glass, and Silicon, connected to an Anode.



As in surface micro-machined structures, bulk micro-machine structures can also be integrated with electronics. This could be integrated on chip or even at the package level as multichip modules, but in micro-machining, you can only have cavities as deep as the wafer thickness. When we want really thicker geometries, we want to look at possibilities of bonding multiple wafers and processing them further.

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On the other hand, when thin microstructures are required, we look for surface micro-machining. In this example, cantilever structures are formed where poly silicon is used as a structural material and silicon dioxide can be used as the sacrificial material.

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Summary: Silicon Micromachining


- > **Surface micromachining**
 - > Surface micro machining (SM) build structures on the surface of the silicon
 - > SM involves
 - > Deposition of thin film of sacrificial & structural layer
 - > Removal of sacrificial layer to release the mechanical structure
 - > Micro structure fabricated using SM are usually planar structure
 - > Dimensions of the SM structures can be several orders of magnitude smaller than bulk machined structure
- > **Bulk micromachining**
 - > Allows selective removal of significant amounts of silicon from a substrate to form
 - > membranes on one side of the wafer
 - > A variety of holes
 - > Or other structures
 - > BM can be divided into two;
 - > **Wet etching**
 - > Liquid etchant (aqueous chemicals)
 - > **Dry etching**
 - > Vapor and plasma etchant

Compared to surface micro-machining, bulk micro-machining allows removal of significant amount of materials and hence larger structures are possible. In both surface and bulk micro-machining, dry and wet etching are utilized effectively. The dimensions of structures formed by surface micro-machining, can be several orders of magnitude smaller than in bulk material and but can have very large dimensions and very thin vertical dimensions.

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Comparison of Micromachining Techniques

> Bulk micromachining	> Surface micromachining
<ul style="list-style-type: none">> Emerged during 1960s> Used pressure sensors, Si valves> Used to realize structures within bulk of a single crystal Si wafer by selectively removing wafer material> Structures may have thickness range from sub-micron to full wafer thickness, and lateral dimensions as large as few mm> Key step is etching<ul style="list-style-type: none">> Wet isotropic> Wet anisotropic> Plasma isotropic> Reactive ion etching	<ul style="list-style-type: none">> Emerged during 1980s> Structures are mainly located on the surface of the Si wafer and consists of thin films> The dimensions of these structures are several orders of magnitude smaller than structures generated by bulk micromachining> Involves<ul style="list-style-type: none">> Deposition of sacrificial layer> Deposition and selective etching of structural layer(s)> Removal of sacrificial layer



As you could see from here, in surface micro-machining you are essentially adding a small component to the surface of the silicon wafer, whereas we dig into the wafer itself in the case of bulk micro-machining. Various components have been demonstrated using both these techniques and have become the main stay in building microsystems. So both surface and bulk micromachining techniques are important. Thank you very much.