Micro and Smart Systems
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Packaging of Microsystems
Lecture – 14

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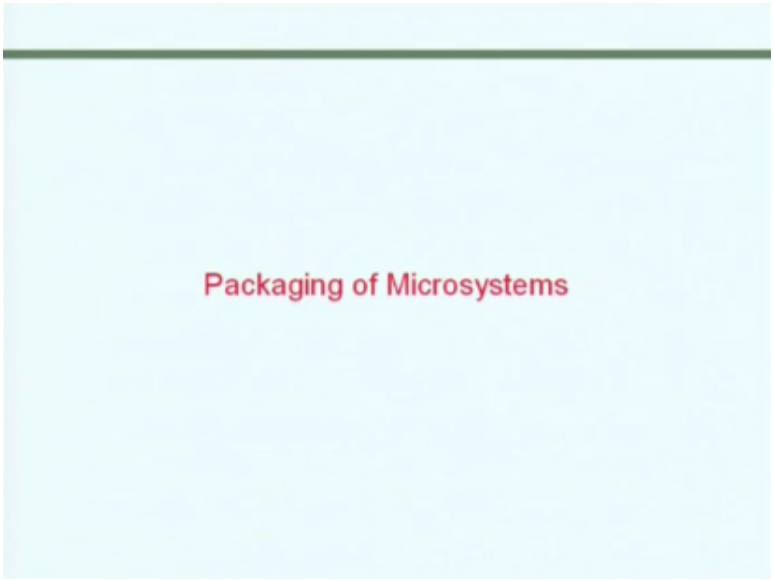

Today, I will talk to you about packaging of Microsystems.

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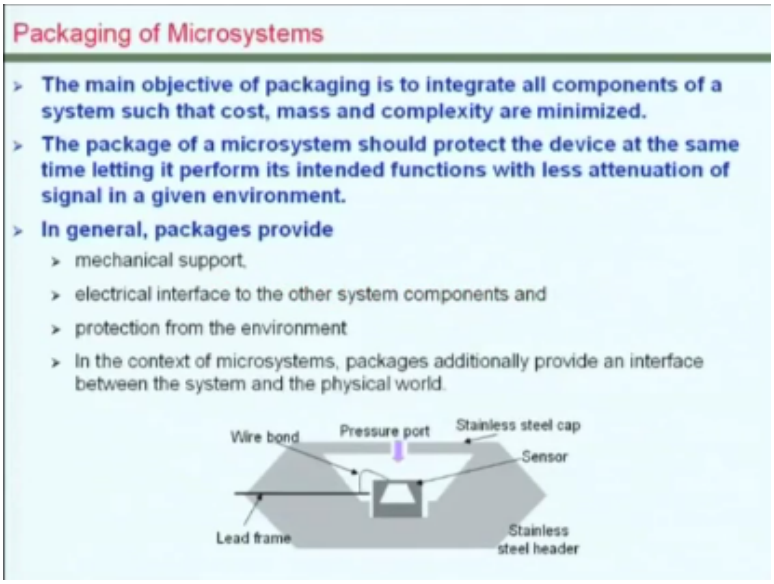

So, the objective here is to package the Microsystems made of various approaches that you

would have seen in previous lectures and how to put it in such a way that we can have the electrical interconnections as well as various fluidic interconnections that would be required for the function of the Microsystems and what are the general issues in doing it.

So, alike the case of microelectronic systems, the package for a Microsystem should protect the device at the same time letting it perform the internet functions by creating the passage or to interact with external vault. So, it should provide the mechanical support. It should provide the electrical interface and it should protect it from environment but at the same time once again it has to provide the interface with the physical world.

So, obviously there are various challenges involved in building such packages. We will see the approaches involved in building such packages and see how one can arrive at useful package to Microsystems.

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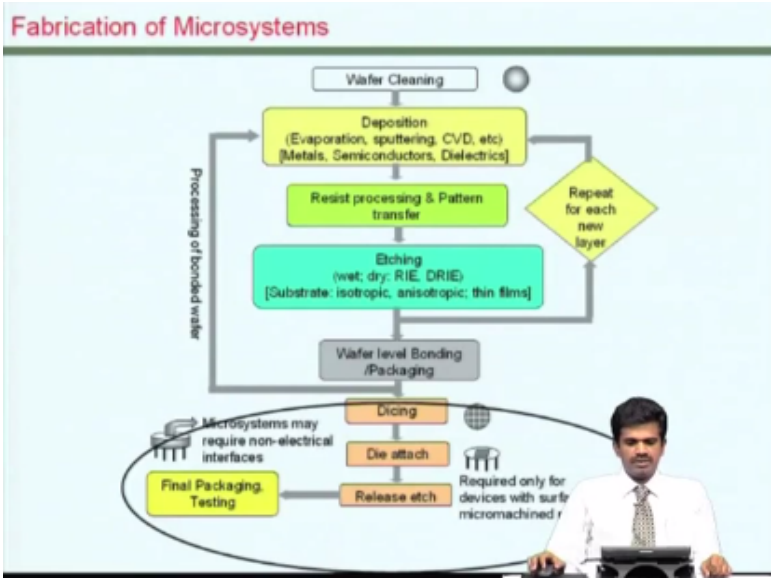

Microsystems by themselves are made using a series of process steps which I have discussed in some of the other lectures. In this lecture, I will be focusing on the steps in the lower end of this chain of events. As you will see, that by this series of process steps which will be reviewed now, we have a complete wafer or bonded wafer which may consist of a number of die.

These have to be separated, attached to somebody which has electrical interconnects as well as

possibly mechanical interconnects and then (()) (03:00) so that it is protected. In the context of Microsystems, there is a critical step known as Release Etch. We will talk about that also as we go by. To understand that we may want to quickly review the processes involved in the fabrication for these Microsystems.

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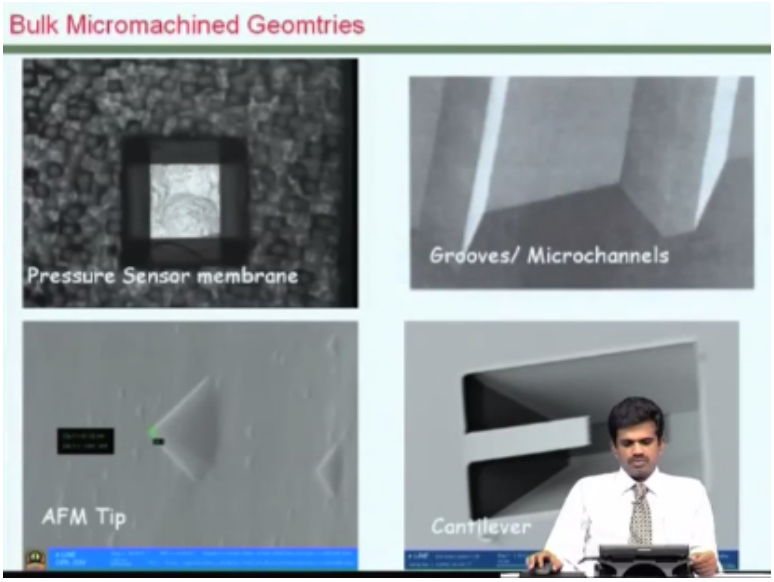

You would have seen from other lectures, we can build various components or parts of Microsystems using bulk micromachining. You can build pressure sensor membranes by removing materials from the substrate. You can build channels or grooves on the substrate and making use of anisotropic etching of silicon, we can have well-defined profiles for this. It is possible to built tip kind of geometry by etching on silicon.

We can also make use of interesting characteristics of anisotropic etching of silicon to build freestanding cantilevers on the surface of a silicon wafer.

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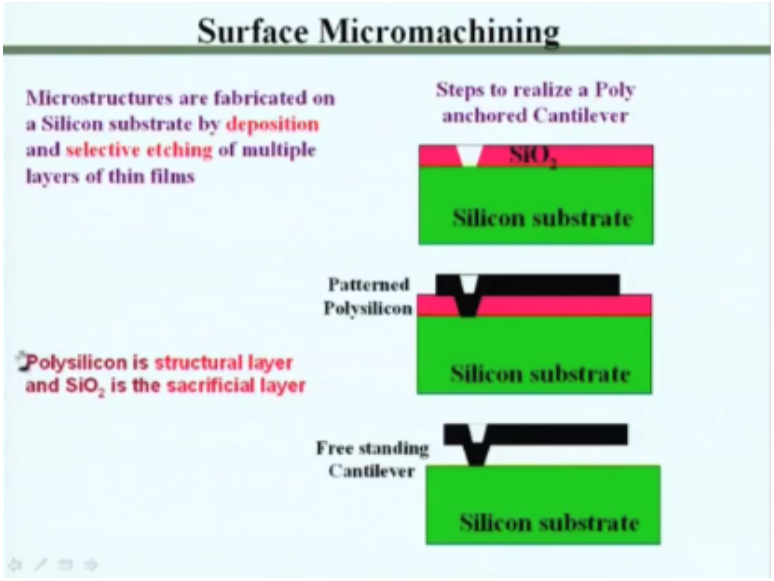

We have also seen that by choice of structural and sacrificial layer materials, we can build limited structures by using what is known as surface micromachining. In this case, we basically add to the surface of the substrate layers. For example, for the minimum, we will need to add one sacrificial layer which will eventually be removed and as structural layer which will be retained as the moving part in Microsystems.

By suitable choice of materials, one can build several useful microstructures by this approach.

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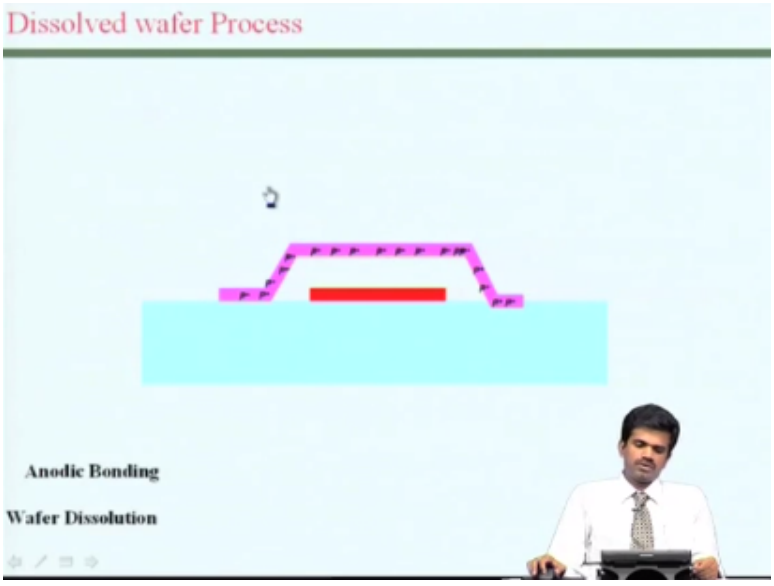

We have also seen about a process known as dissolve wafer process in which two parts of the same Microsystems are built at the wafer scale on two different wafers and these two wafers are

attached together by wafer bonding and then one of the wafers is removed by dissolving the silicon in this particular case and retaining a smaller portion of this which is a heavily adopt region of silicon which has different chemical characteristics than the regular silicon and therefore the structure would be remain attached to the glass substrate that you see here.

So, this approach can also be used for building micro structures on various substrates.

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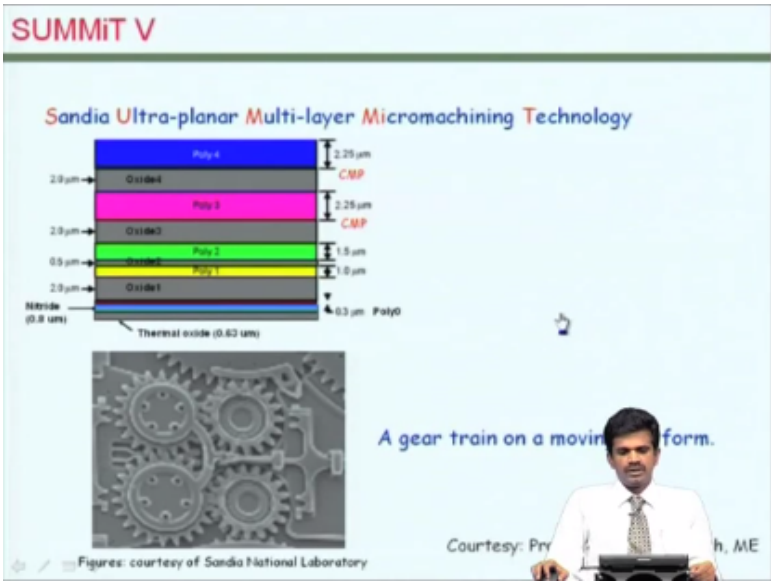

In another context, we also talked about extending the surface micromachining approach by using chemical mechanical polishing which can result in planar layers even after etching some of the layers in between. So, with such planar layers, one can go urgent into a large number of structural layers and complicated looking structures such as the gear chain developed by Sandia National Labs could be formed primarily because of the polishing method that is used.

In this case, you know we use both chemical and mechanical approaches of removal of the outside layer, so that this could be patterned relatively quickly and subsequent layers could be added and it brings in several advantages in building Microsystems.

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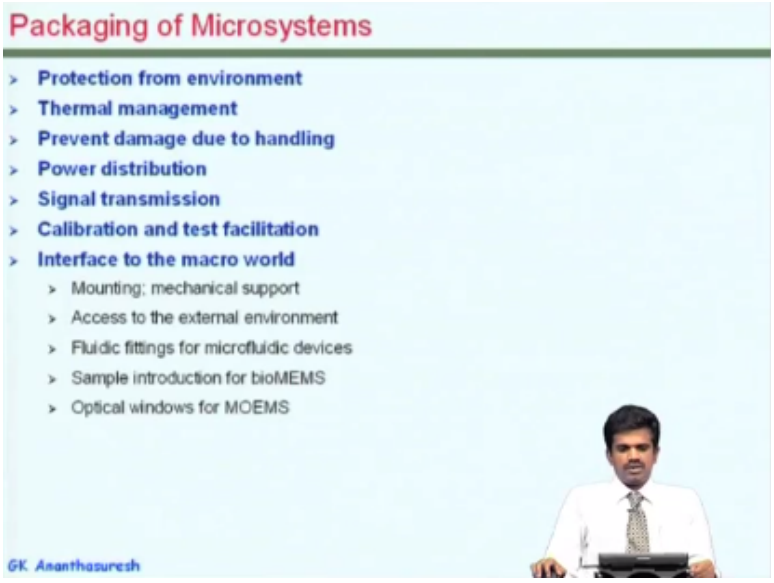

Coming back to packaging of such Microsystems which may have these fragile moving parts, one need to look at aspects of protection from environment, thermal management to dissipate the heat that is generated due to various aspects of the operation of the device. We need to look at the aspects of handling these dies and package devices, approaches for the distribution of power as well as signal and test and verification and more important than anything else interface with the macro world.

How this could be mounted on a mechanical support and how access could be provided for the external environment and how fluidic interconnections could be made and you know how this could be used in various specialised applications such as biosystems as well as optical systems.

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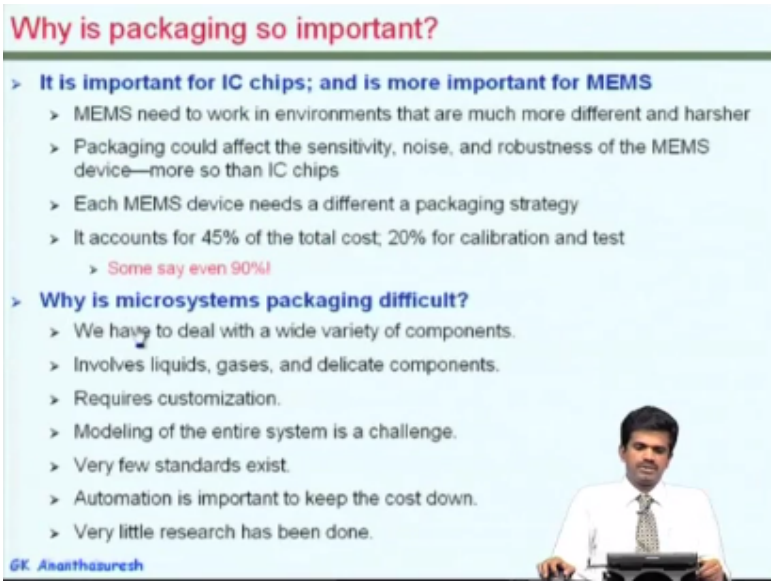

Packaging is a very important step in microelectronic systems. It even more so in the context of Microsystems because we have a number of these delicate parts added which are also mechanically moving. So, this have to work with different kinds of environment, unlike the case of microelectronic chips and therefore since the Microsystems that is being packaged is likely to be different and it may have different shapes or parts involved and different kinds of interfaces required, standardizing the packaging strategies for Microsystems is more difficult.

In the context of integrated circuits, you know typically the cost of the chip is substantially added by the packaging step itself. People say about 20% to 40% could be based on just the packaging step. In the context of Microsystems, there are additional complexities that we have talked about. So, obviously packaging is a very important step in building successful Microsystems that could be deployed. The challenge is that very few standards exist for building such packaging.

So, it has to go hand-in-hand with the design of the Microsystem itself. However, standardization and automation of the processes involved can potentially bring the cost down and as it stands, very little of research is done in the area of packaging of Microsystems.

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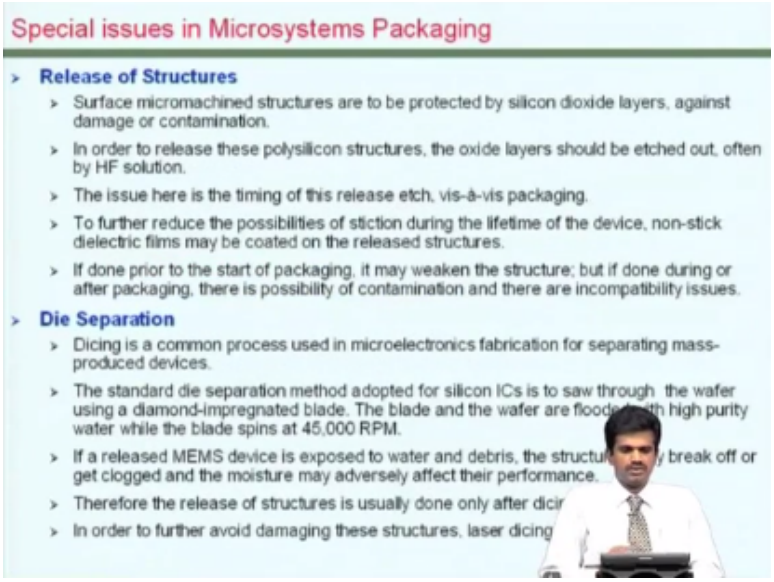

One key aspect in the packaging of Microsystems or developing the strategy for packaging Microsystems is the release of microstructures. If you recall in surface micro-machining, we have this fragile parts which would be formed by removing the sacrificial layer which in the example that I have shown was silicon dioxide which was supporting the polysilicon layer. So, when we release this polysilicon layer by which I mean remove this outside layer, it becomes a highly dedicate structure.

So, that limits and you know if you want to start for example dicing the wafer after it is being released run into problems because the vibrations caused during the dicing can make the structures displaced from the surface. So, most of the packaging steps are done before release of surface micro-machine parts. So, the die separation or dicing which is a common process used in microelectronics has to be timed, has to be performed before the last step for microfabrication.

So, although we have talked about it during the microfabrication, I have release those freestanding structures. In practice, this is done much later after the die are separated and as are attached to the package base. So, this essentially avoids damaging of structures during the dicing process.

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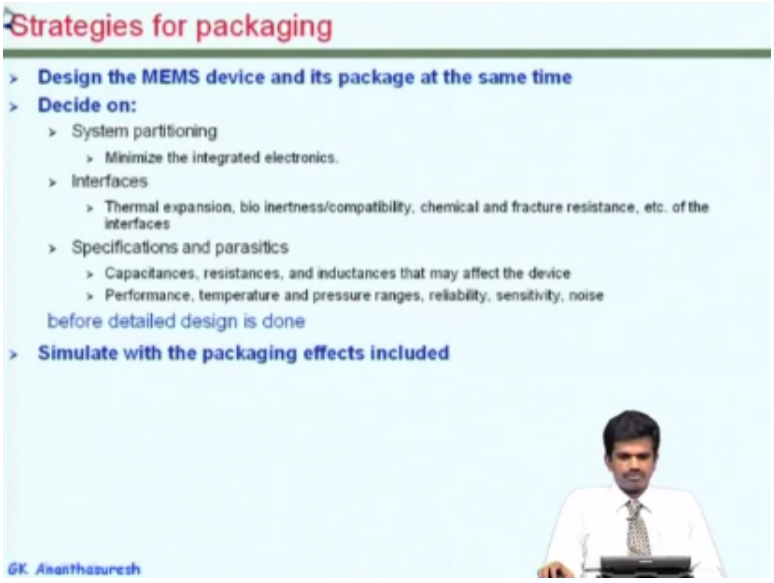

So, in the absence of clear-cut strategies or standard procedures, we think about the packaging while designing the Microsystems device itself. So, one needs to decide on the system partitioning, so as to minimize the electronics that would be going onto the chip. One need to look at the effects of that on the interfaces required through the package and things that could be embedded within the chip and therefore various specifications and parasitics will have to be looked at while designing the system by itself.

So, usually what is done is to simulate this entire environment including the packaging effects. Otherwise, the contributions from the package would remain as an uncertain parameter which could eventually affect the overall performance of the device being made.

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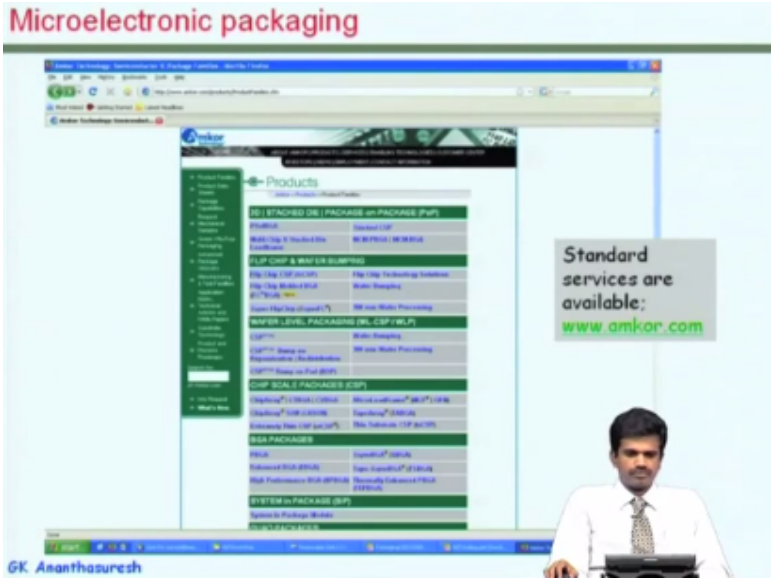

In microelectronics in contrast packaging is a relatively well-developed field and standard approaches and services are available from various vendors. Compared to Microsystems in microelectronics, we only have fewer functions for the package. It has to protect and it has to provide the electrical interface only apart from providing the mechanical support and thermal dissipation characteristics.

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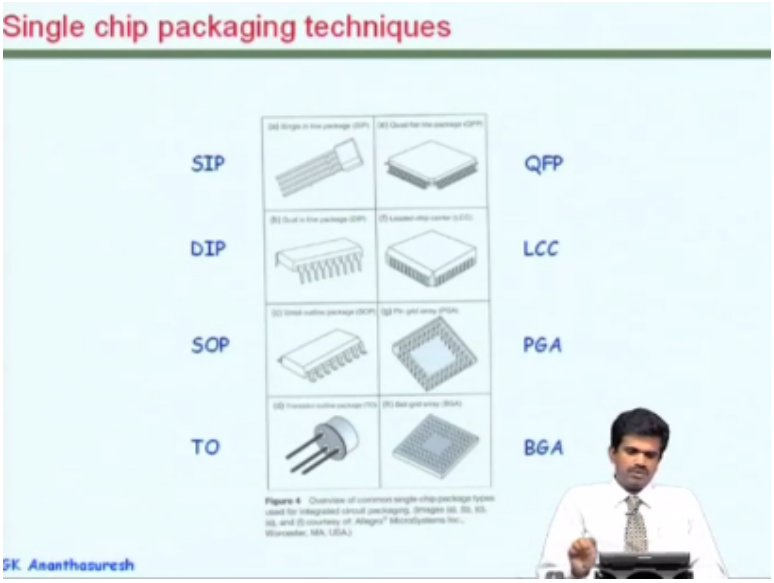

So, a number of standard packages are available for building micro electronic packages. These include approaches such as single in-line packaging, double in-line where you have two rows of legs. We have additional packaging approaches which could be extended for better performing chips. As you could see in some of the later generation packaging approaches such as ball grid

array or pin grid array.

We essentially can minimize the lengths of the leads and these could be attached directly onto the board. So, the uncertainties and parasitics caused by these later generation packages are much lower than some of the older conventions of packages that are there in microelectronics. So as you could see in many particular Microsystems, these could be extended or adopted to build Microsystem package.

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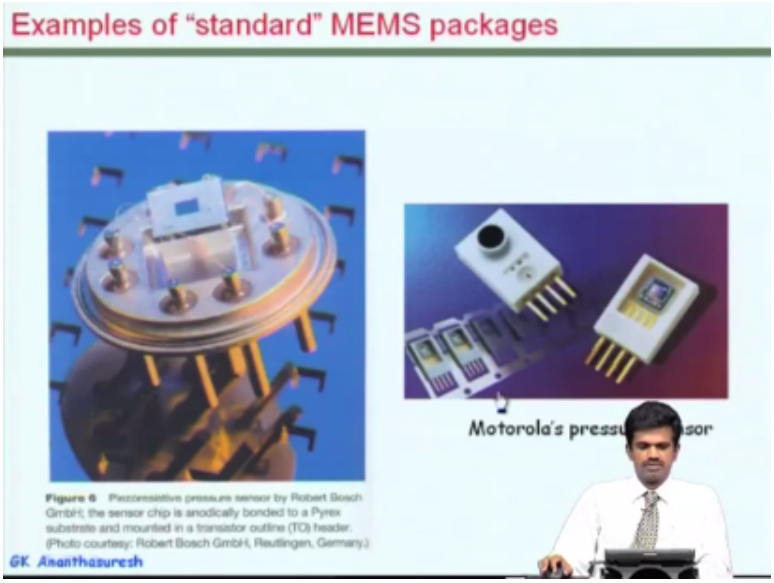

For example, a standard Microsystem package would look very similar to the transistor package that you have seen in the previous slide. So, we attach the die of the Microsystem onto a package base and do, as you see here, wire bonding and then cap this thing and provide additional interfaces on the cap and weld it together to the base and system is ready to use and more attractive packages are now available for several commercial Microsystems which are being deployed.

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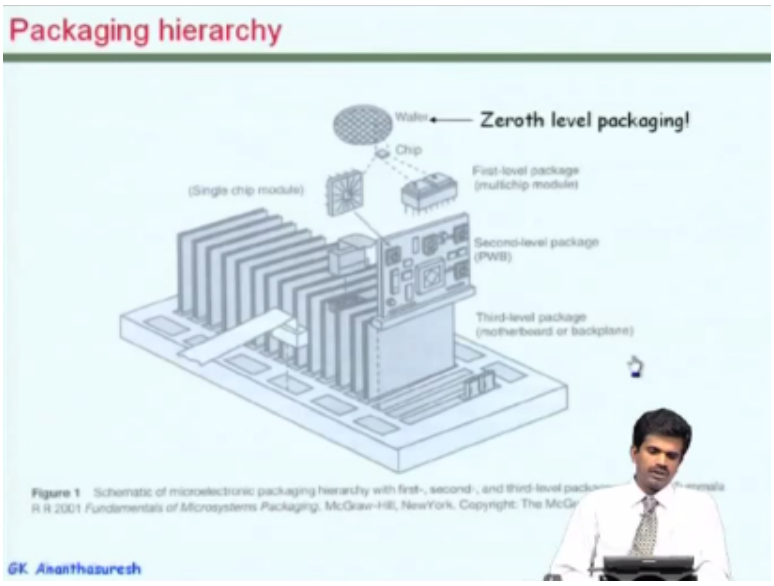

To look at the hierarchy of packaging, there are various possibilities for Microsystems. We start with this wafers. So it is possible as you will see to provide small amount of protection in many Microsystems by doing a zeroth level of packaging at the wafer level itself. We will how this can be done. Then, we make these into individual chips which are essentially attached to the package base which goes into subsystems and eventually into full-fledged systems,

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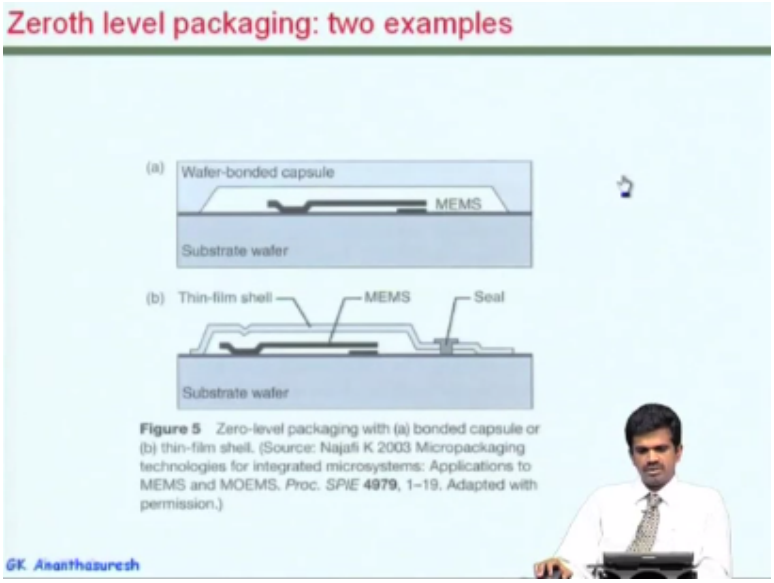

So, we will see some of these. So, what I meant by this zeroth level packaging is by adding another wafer on top of the primary support wafer. So, in doing so, one can actually protect the fragile parts of the Microsystem. So, the Microsystem is now capped entirely by a wafer and we can provide interfaces in this wafer by creating windows, etch halls in this wafer which can

essentially provide those interfaces.

So, it is possible to provide a primary level of support to the many of the Microsystems by doing some kind of capping by using the wafer bonding process that we have discussed in other context.

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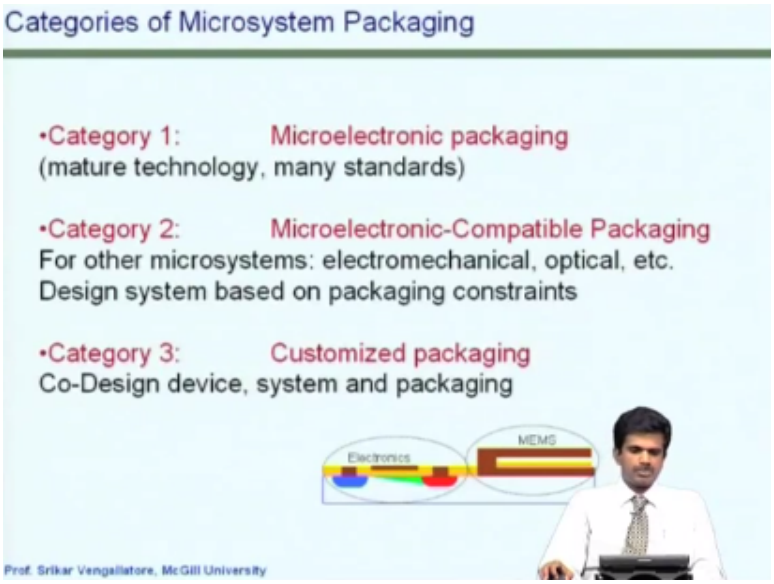

So, the Microsystem packages could be categorized into three types. One could be just in cases where you could just follow in microelectronics packaging. In some other cases, one can extend the microelectronic packages to provide these extra interfaces but still make use of electrical interfaces in the conventional microelectronic approaches, and the most difficult would be the customized packaging where we will definitely need to work together have the complete package system which would be designed along with the design of the Microsystem itself.

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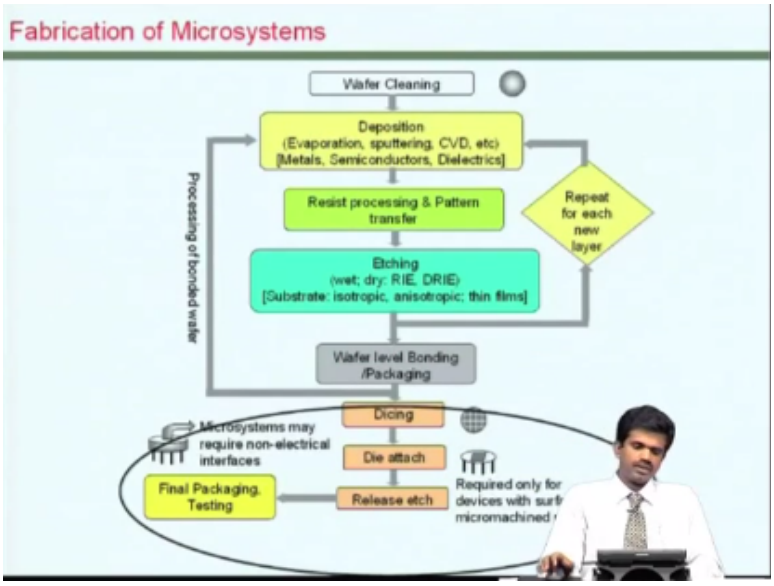

So, if we come back to this flow diagram, what we see is that you know we have this completely made number of dies on a single wafer which has to be eventually packaged with the external interfaces. So, we will see some of the criticalities involved in doing these steps from this wafer to the packaged device.

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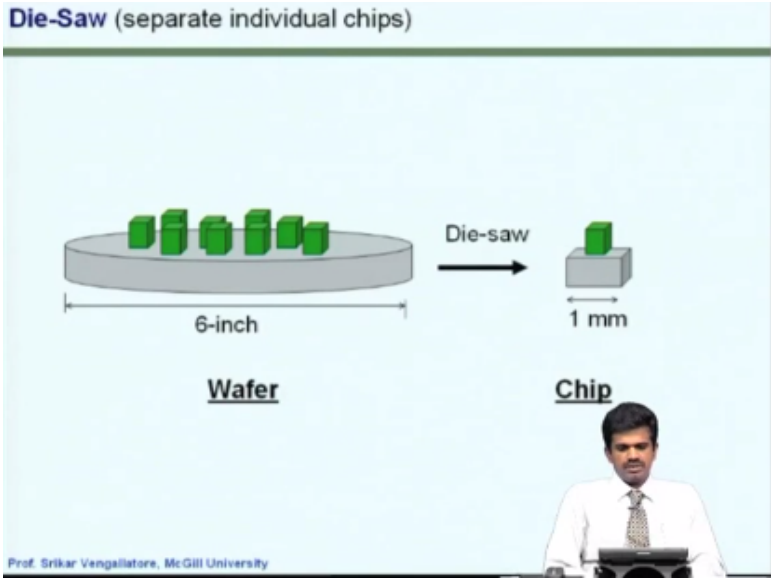

So, the first thing that is to be done is to essentially take out this individual dies from the 6-inch or 8-inch wafer that we would start with. So, this individual chips which may have open protected microstructures on it off the order of few mm are now taken out usually by using a die saw or a laser cutting machine. So, that gets us the individual chips.

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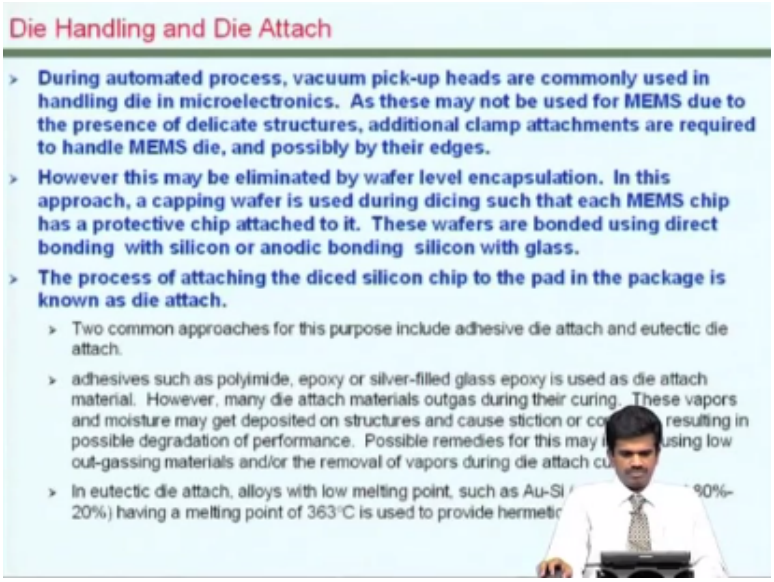

But there are several issues in the context of Microsystems. In a typical automated process in microelectronics, we can possibly use a vacuum pickup head for handling these dies but in Microsystem with these delicate parts, it is almost impossible to use a vacuum holding structure. So, that brings in a new dimension of issues. Obviously, this can be eliminated by the wafer level packaging approach. In that case as I have just mentioned, we cap the wafer before dicing, so that the chip itself is protected.

So, the process of attaching this diced silicon chip onto the package base is known as die attach. There are two common approaches; one is known as the adhesive die attach in which case we use an adhesive, polymeric or elastic material for this addition. In the other case, we use a gold layer which would be used to make this eutectic contact between the base and the silicon die. As I mentioned in another context, it requires a temperature of 363 degrees to provide the hermetic sealing of the package.

Adhesives could be polyimide, silver epoxy which is a conducting material or these could be used for sticking the die onto the package base.

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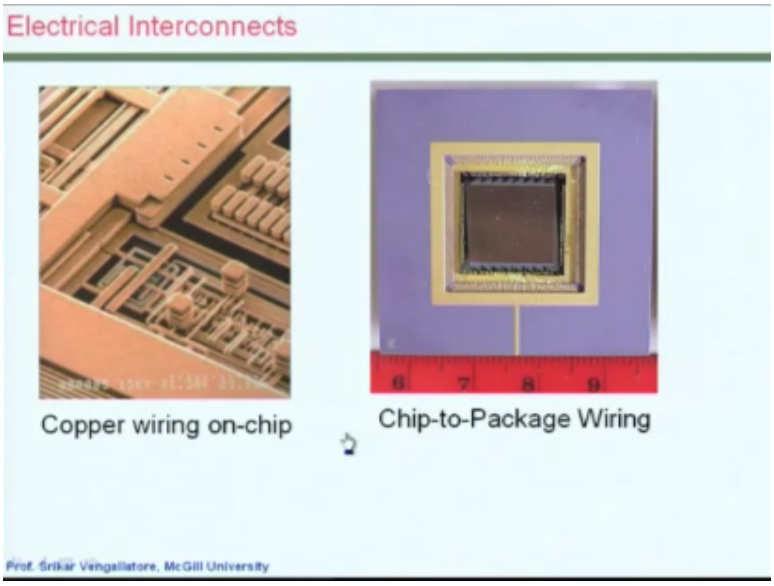

The next issue is to provide electrical interface. Within a chip, we can layout conductor patterns. When it comes to connecting the chip to the package, one need to look at the wiring and it is usually done by an approach known as wire bonding.

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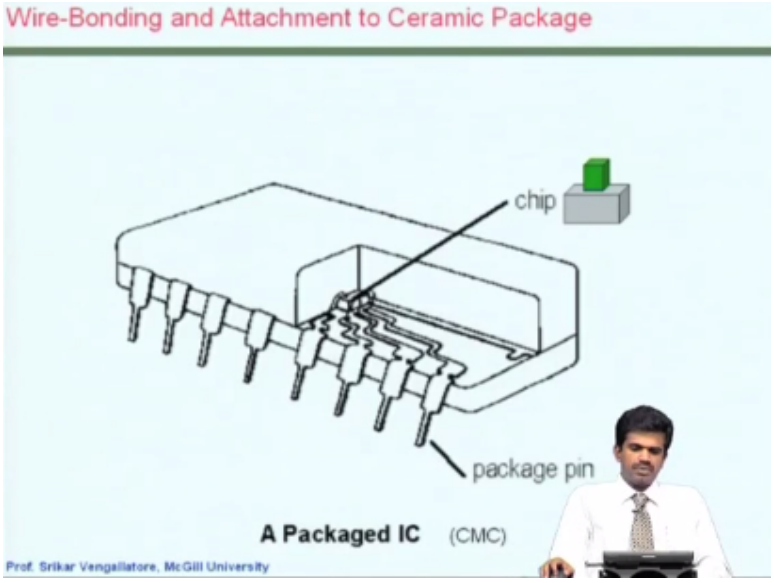

There are also issues in taking the leads through the package, so in many packages there could be conductor traces made out on the package base itself to reach out to the chip.

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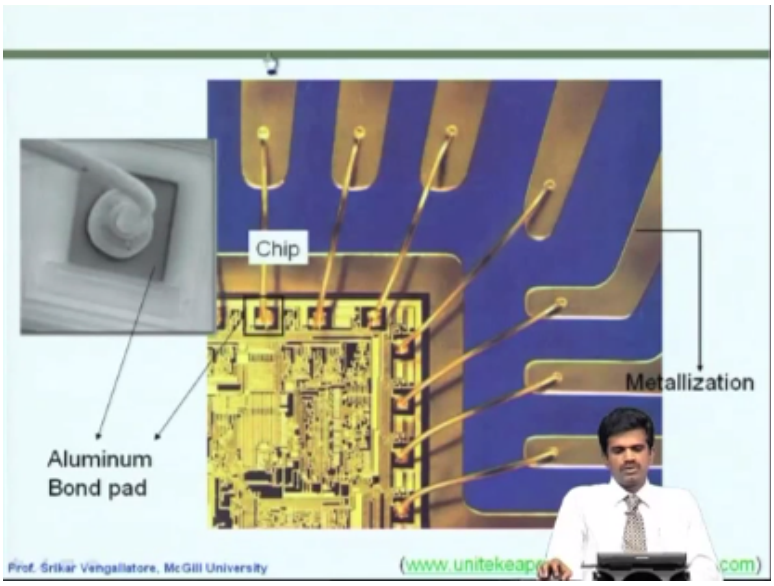

So, in wire bonding what is done is that from a pad on the chip to pad on the package, an electrical connection is made using aluminum or gold wires.

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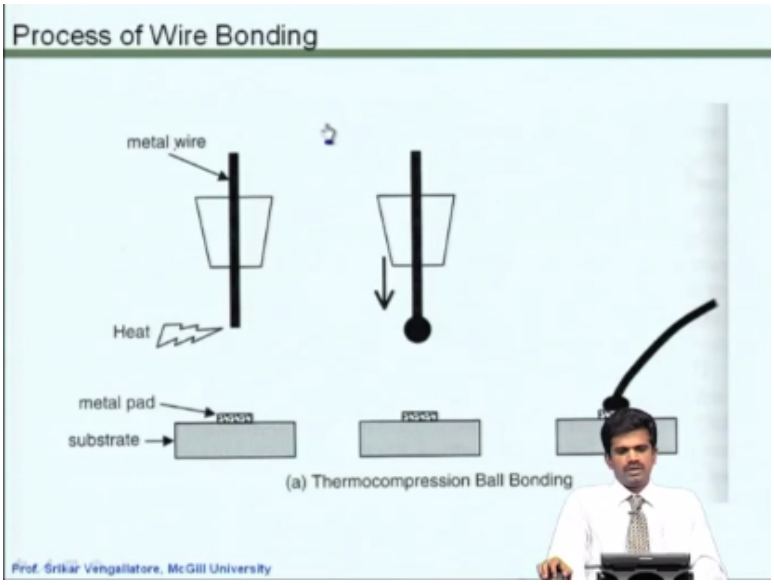

It essentially this very narrow gold wire which is of the order of 25 microns thick which could be first bonded onto the pad on the substrate or the die and subsequently it is attached to the package base. It requires temperature and ultrasonic energies and this can be done using wire bonding machines.

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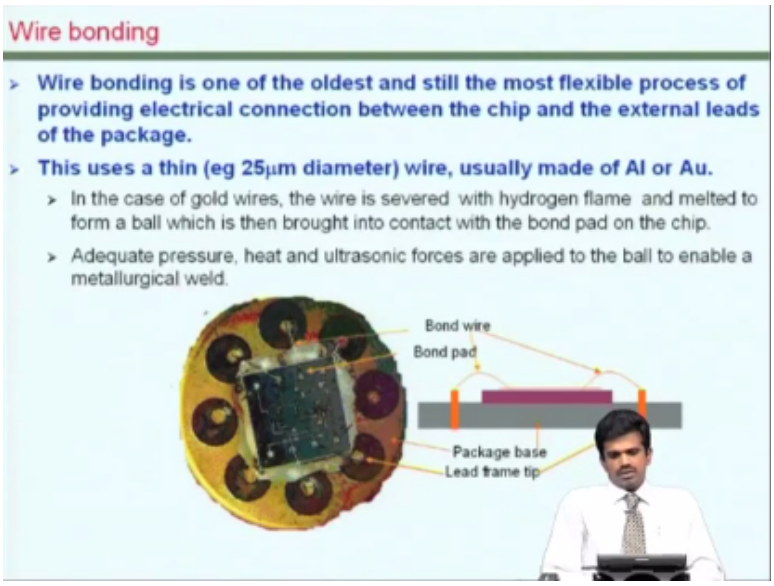

So, wire bonding is one of the oldest and most flexible approaches for providing electrical connection between the chip and the external leads of the package. As I mentioned, you could use either gold or aluminum wires and it also depends on the kind of pads that are there and by providing adequate pressure temperature and ultrasonic forces, the bond can be made to stay for longer duration for the operation of this device.

So, the thin wire essentially provides the connection between the package and the die.

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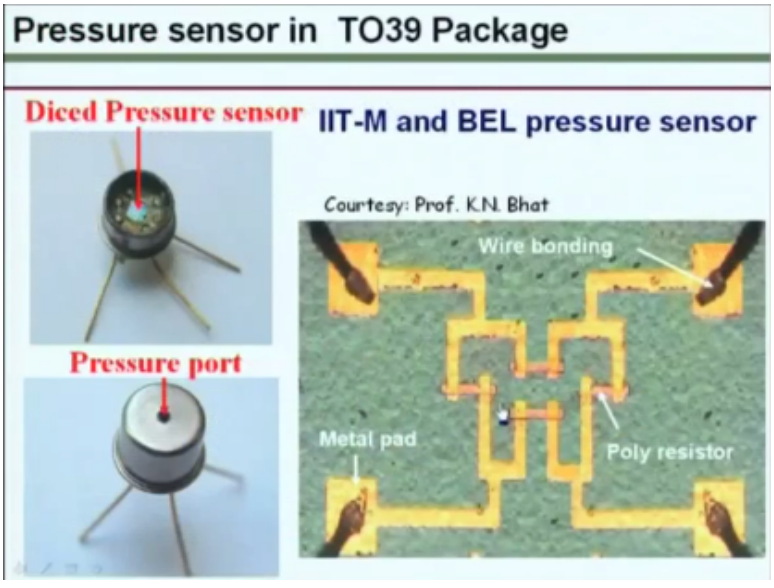

For example, in a pressure sensor, the next step would be to provide this fluidic interconnection. For that, one may need to modify and include a pressure port for example for a pressure sensor.

So, in a pressure sensor we have all these resistors, polyresistors on the diaphragm which is fabricated by microfabrication and which are bonded onto the base but to make this deflection to happen, we need to bring in the fluidic interface, that we will see later.

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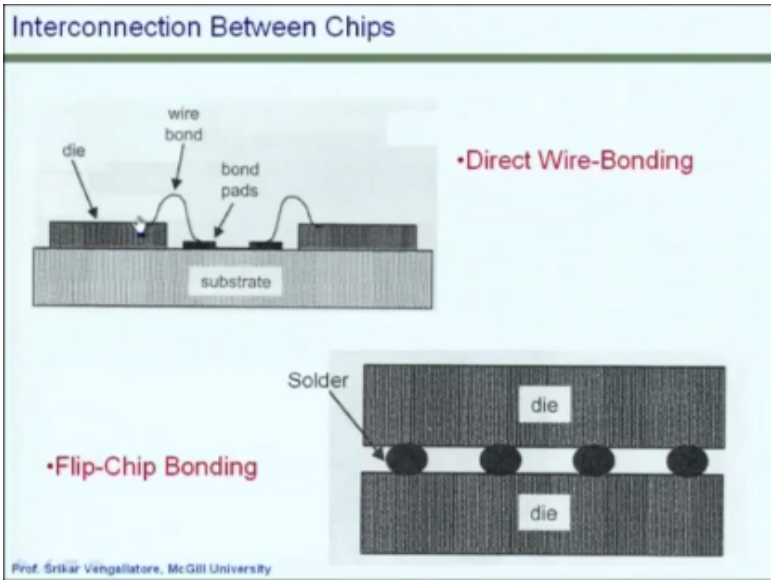

Apart from this direct wire bonding, there is another approach of providing electrical interconnection which is known as the flip chip bonding. In this case between dies or a die and substrate or the package base can be contacted by providing these balls in between which would be pressed together and heated.

So, in flip chip, we essentially have two layers of electronic or even MEMS chips or package bases which are essentially connected together rather than having this electrical wiring between them, we use this solder bumps which could be pressed and melted to make this perfect electrical contact.

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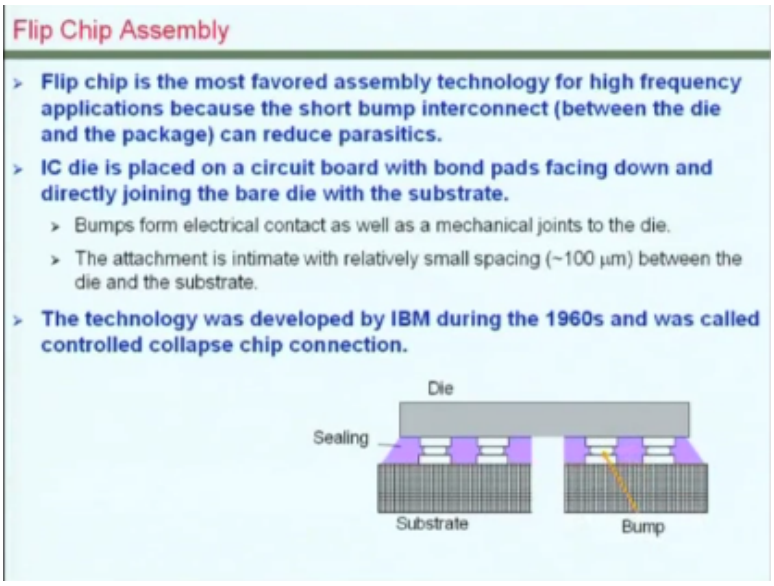

Obviously, this is far more favored assembly method especially for high-frequency and other approaches and the IC is placed on the board or even another die and one can actually design these in such a way that they are aligned together and ultimately the attachment is controlled properly and this technology is fairly match. This has been extended now for Microsystems.

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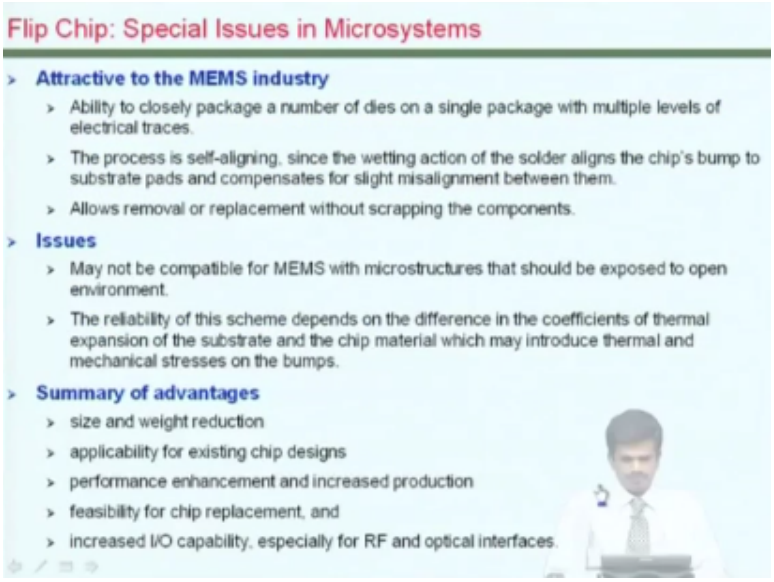

The main advantage is that it can provide closely packaged dies within a single package and we can go for multiple levels of electrical traces and this to a great extent is a self aligned process, so based on this waiting action of solder, the chips bumps would come in contact which would compensate for slight misalignment and you know the issue is that in cases where there are microstructures which are above the surface of the wafer, there could issues in contacting them

using the flip chip approach.

These schemes would depend on the thermal expansion coefficients of the substrate and the chip material and can introduce some issues based on that. So, the main advantage of flip chip approach of assembly is the reduced size and weight. It can be used in a variety of chip designs and can improve the performance while production and it is possible to include IO compatibility for various applications.

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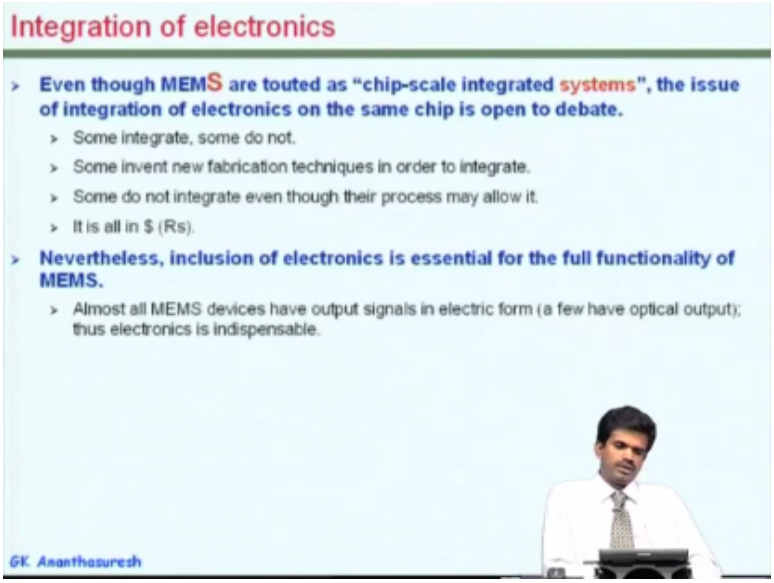

One of the key challengers in Microsystems is while providing integration with electronics. Even though MEMS is primarily talked off as a chip scale integrated mechanical systems integrated with electronics, there are various challenges in building these two together in the chip level. As we have eluded to in previous lectures, the sequence of process steps required for building electronics and for building Microsystems can lead to incompatibilities.

However, building these together smaller in single die would significantly reduce the overall cost. Hence the integration with electronics is exploited with full vigor for successful Microsystems.

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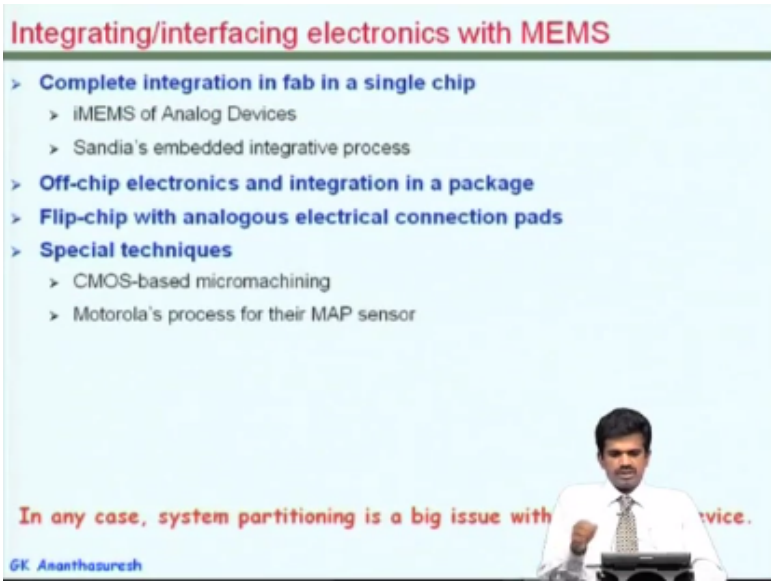

Several approaches are pursued for integrating electronics and Microsystems. We can talk about the iMEMS approach developed by analog devices. There is an integrated embedded approach developed from Sandia. There are several off chip electronics approaches and we have talked about this flip chip approach with these interconnections between different dies possible and there are several approaches in which we limit the micro-machining to see CMOS-based processes.

So, essentially the choice of the approach is based on the functionality and the fabrication complexity of the Microsystem itself.

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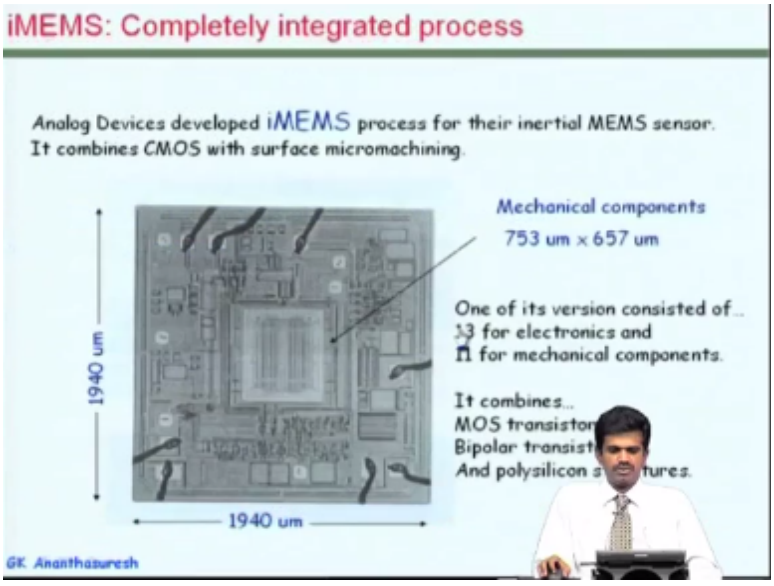

In the iMEMS approach, CMOS-based electronics and surface micro-machine components are built together and integrated in which most transistors or even bipolar transistors and polysilicon structures all integrated into a very small system of about 2 mm x 2 mm.

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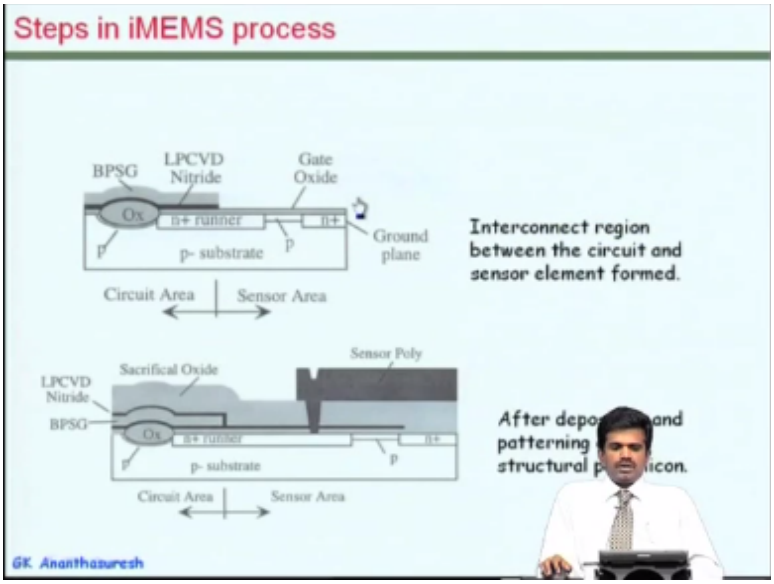

In this case at the die level itself, we will have both the sensor polysilicon part and the electronics part which will be sitting side by side but the key is that while processing this micro-structure, the electrical regions will be usually partially protected so that they will not be affected.

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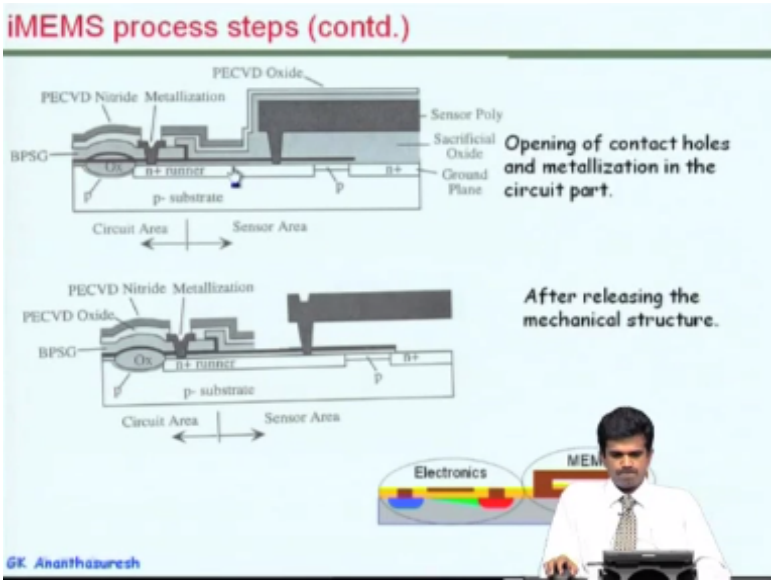

So, fairly complicated electronics and microstructures could be combined in the iMEMS process

and the freestanding microstructures can be obtained by releasing those from this (()) (36:38).

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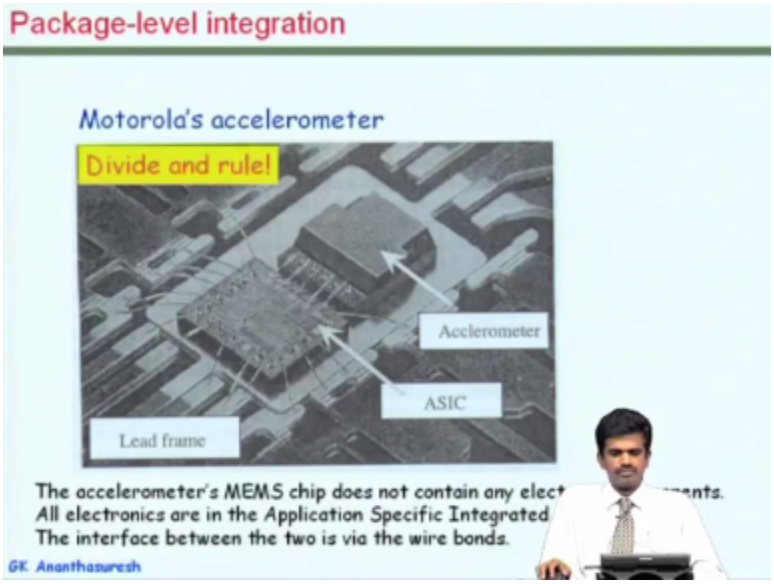

It is also possible as is done for the accelerometer to build some part on a mechanical die and another part in ASIC and then can provide the connections between them and then interface it with the external vault by using the interconnects on the lead frame of the package. So, in these two approaches as you have seen the totally different you know in the second case, these two are fabricated separately and put together.

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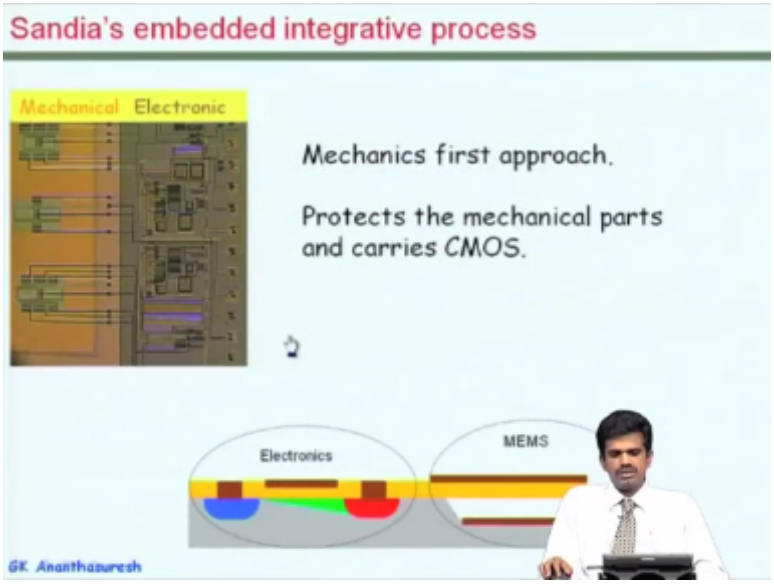

In Sandia's approach compared to the iMEMS approach, the mechanical part would be fabricated first and then the electronics part will be fabricated and ultimately these are integrated together in

package.

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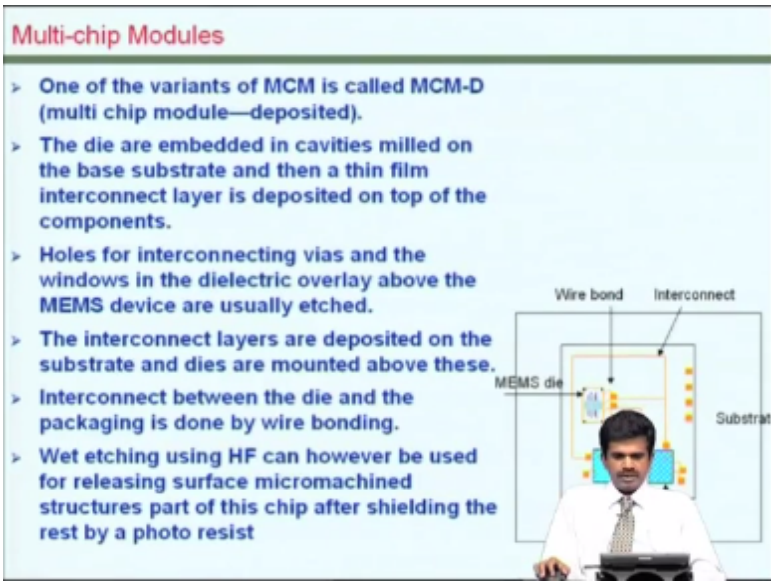

As I mentioned, when you have these multi-chip modules where we will have multiple dies, these could be connected together using interconnects on the package base and individually these are all connected using a wire bonding or flip chip-based approaches and we will have a common substrate to hold all of these together and then attach these onto the package base. So, these interconnect layers are actually deposited on the substrate and the dies are essentially amounted above this.

So, the interconnect between the die and package is usually done by wire bonding. So, the release etch is usually done after it is mounted on this package.

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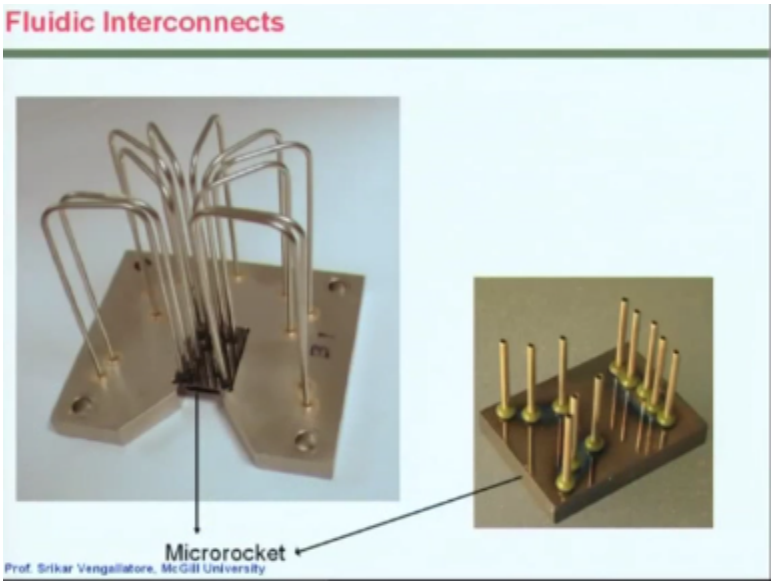

So, as I mentioned, the next issue is providing this known electrical interfaces and in most cases the fluidic contacts.

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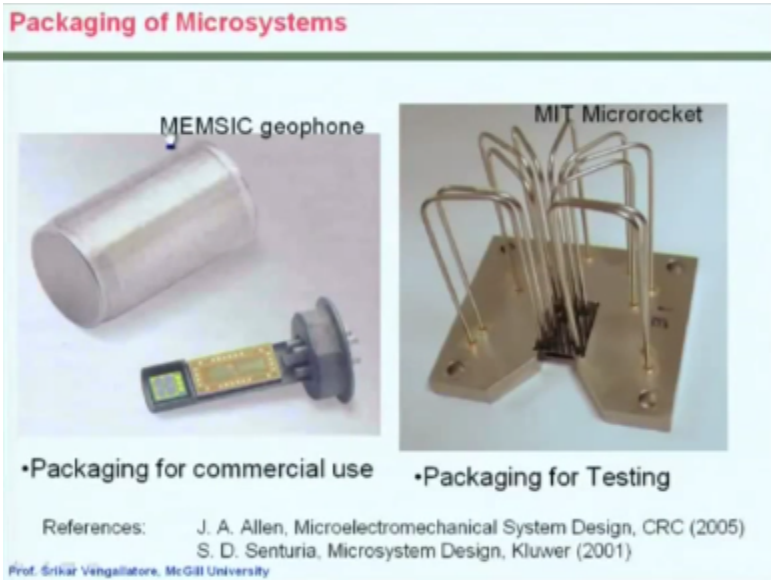

Microrockets have been used for this purpose to provide the non-electrical interfaces to various parts of the die and this whole thing can be packaged together and has been demonstrated by MIT.

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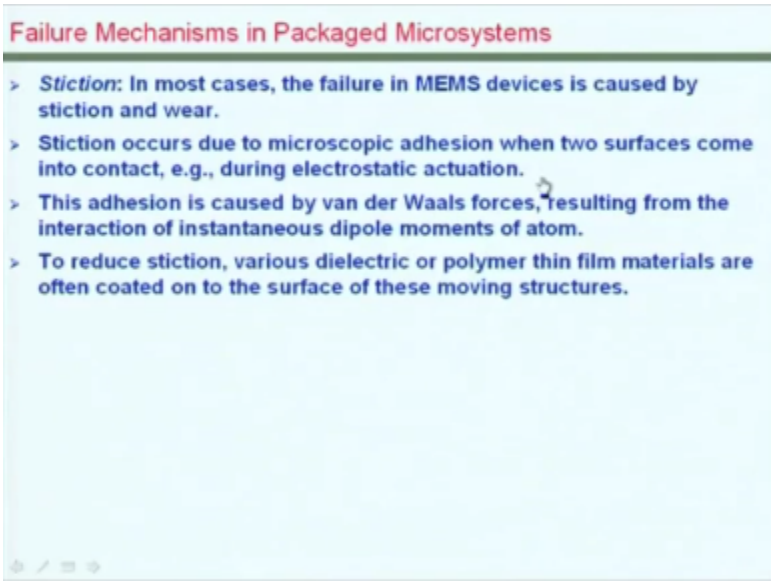

It is worthwhile to explore some of the failure mechanisms in the Microsystems in this context. Stiction is the most common failure mechanism due to in-surface micro-machined Microsystems. In records as I have mentioned earlier due to the microscopic addition when to plan our surfaces are put into contact. For example, during electrostatic actuation. In electrostatic actuation you may recall we have a beam which is pulled together by applying a potential.

So, when this beam touches the surface of a conductor beneath, if both of these are planar surfaces, these may adhere due to van der Waals forces and this can result in these sticking together. To some extent, this can be limited by using a dielectric layer above the conductor and there are various other approaches of minimizing stiction.

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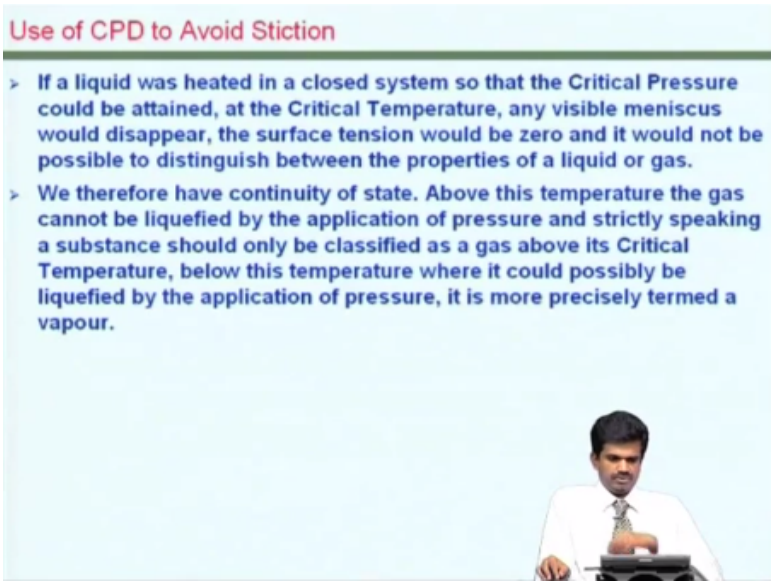

If you recall during the fabrication stage also, stiction is an issue in surface micro-machine devices. Critical point dryers could be used to avoid stiction in that context.

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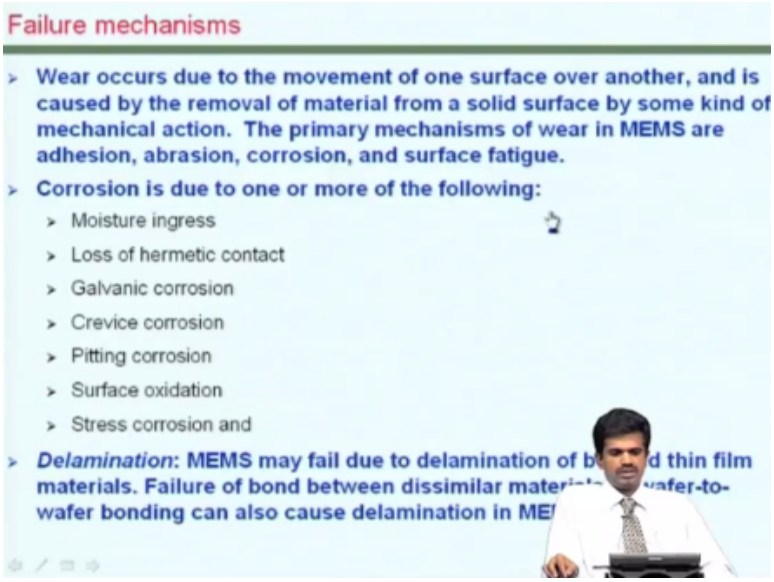

Other failure mechanisms would wear because it is a mechanical part that is moving which can result in marginal removal of materials from the solid surface due to this mechanical action. Another cause for failure could be corrosion which could be due to various reasons including moisture ingress. The loss of hermetic contract at the package due to galvanic corrosion when there are more than one matter is present, due to pitting or crevice, surface oxidation or stress-based corrosion.

In Microsystems, another possible reason for failure is delamination because we deal with several thin films of different materials and during some of the process steps, we expose these to extreme environmental conditions which can cause delamination of the layer.

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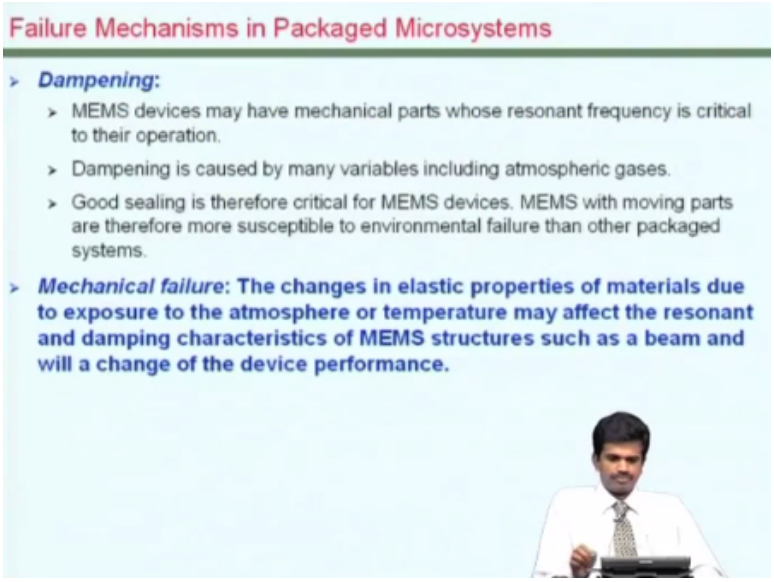

In packaged Microsystems, dampening is one of the issues for failure. For such a severe use of these mechanical parts, it can create issues. So, various mechanical failures can affect the performance of packaged Microsystems.

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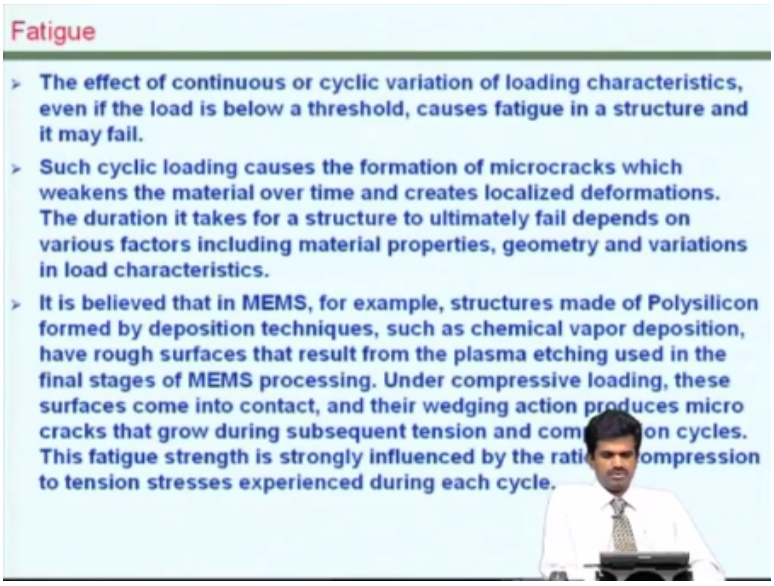

Fatigue is another long term contributor for the failure of Microsystems. Due to cyclic loading, micro-cracks may form on these microstructures which essentially aggravate over a period of

time and cause ultimately failure of this part. Many structures in Microsystems are made of polysilicon which are made by deposition of thin films.

These have rough surfaces and caused by etching and other process steps and when these are subjected to compressive loading, there could wedging action which could produce this micro contacts and that can affect the characteristics of the structures.

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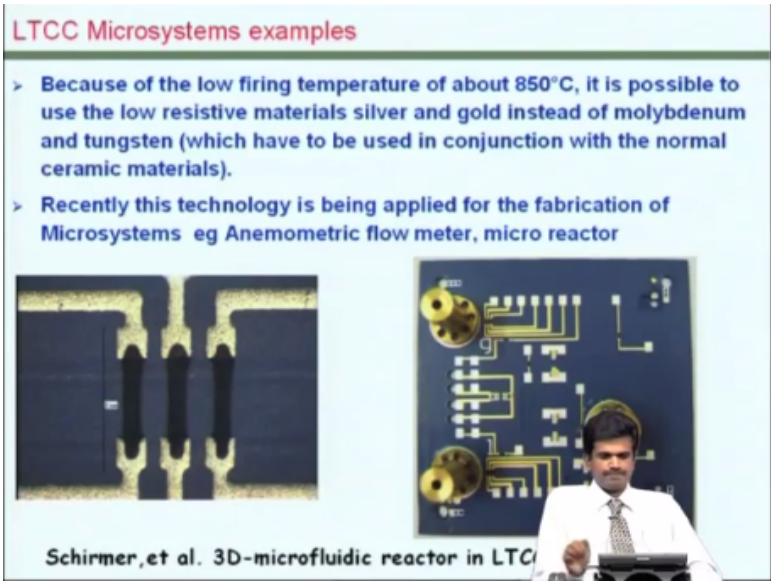

It is also worthwhile to look at some of the alternate approaches for packaging Microsystems. In another context we talked about self-packaged Microsystems using LTCC. The examples that we have discussed include an Anemometric flowmeter which is completely integrated by this multilayer low-temperature co-fired ceramic approach. As you see here it is also possible to prove non electrical interfaces to micro reactors and the like by the LTCC approach.

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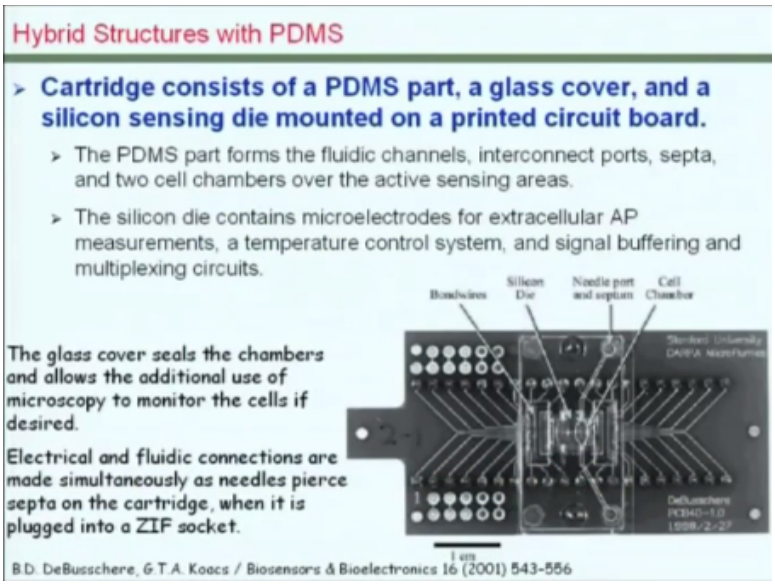

We have also talked about PDMS-based hybrid structures which are also self packaged systems. So, the PDMS-based open cavity is created with which will be attached to the electronics on a harder surface and could be used as cartridges for biological senses. So, as you see these self packaged approaches do not necessarily follow the Microsystem-based approaches and hence are designed completely have been issued.

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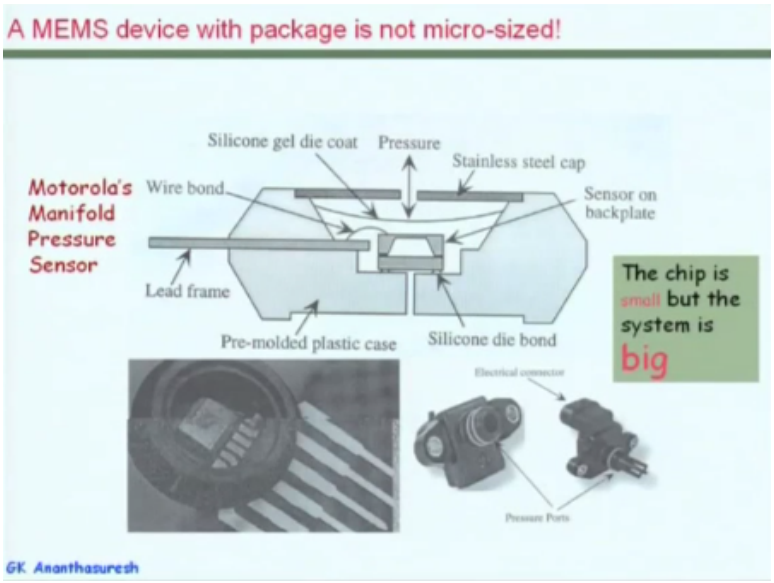

Coming back to Microsystem packages that are more general purpose, there are pressure sensor packages which would consist essentially of a mechanical metal enclosure with electrical lead frames which could be used for electrical interconnects and pressure ports which I have discussed previously. But an interesting thing to note at this stage is that the chip is small but the

packaged system is fairly large.

To some extent, this is caused by the complexities involved in the packaging itself, but the key to remember is that the packaged Microsystem is not at all micro-sized.

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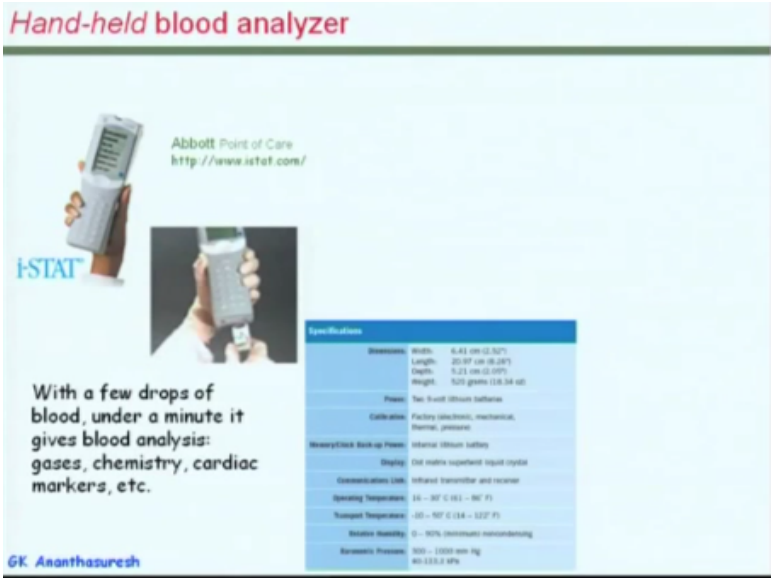

There are various other biosensors based on microfabrication approaches which would make use of these chips made of small parts but ultimately, the system by itself is relatively big.

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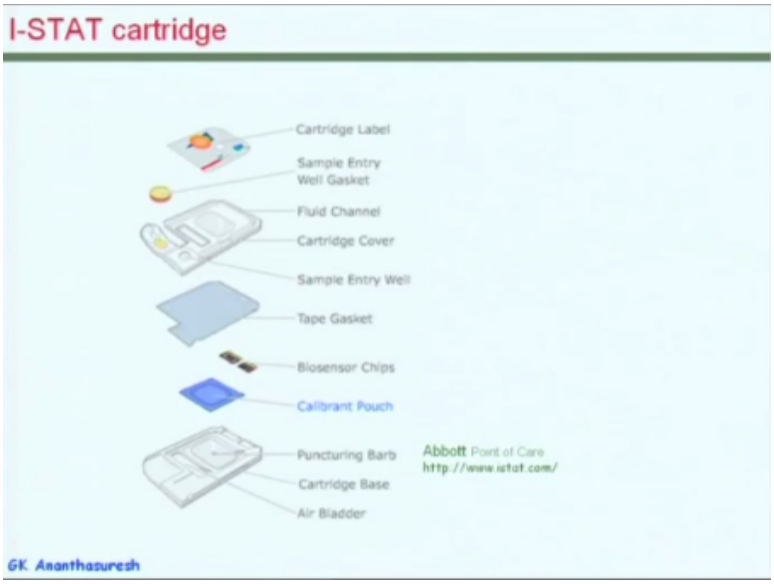

If you look at the cartridge that is going into some of those sensors as you see, the individual Microsystem parts are relatively small. Yet, the overall system is made to be big.

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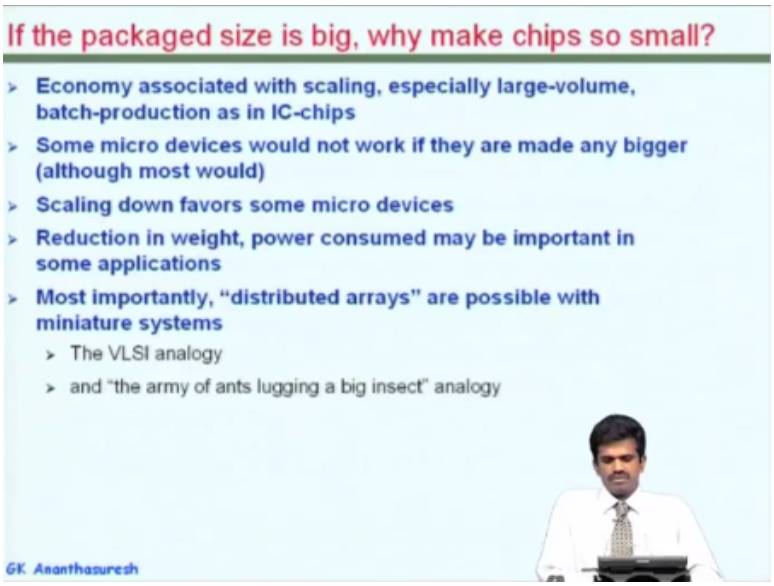

So, the natural question that may arise is that why do we struggle so much to build chips that are so small if the systems are large. We have talked about the reasons for these in some of the earlier lectures. There are several advantages associated with the large-volume batch-production in IC chips. The entire cost involved in producing these chips will get shared. There is really no point in buildings such chips in large area.

But more important to note that some of this micro devices, for example an electrostatic actuated device will not even work at larger-sized case. So, we essentially make use of the scaling advantages offered by the microfabrication in building some of those. So, scaling does favour apart from reducing the weight, the power consumption, etc. that comes naturally in making things smaller.

But more important than many of these, it is also possible to have a distributed array of miniaturized systems just as in VLSI for Microsystems. You can think about the analogy of ants which can possibly carry a large insect. So, when we have this distributed arrays, a lot of things can be done with these parts.

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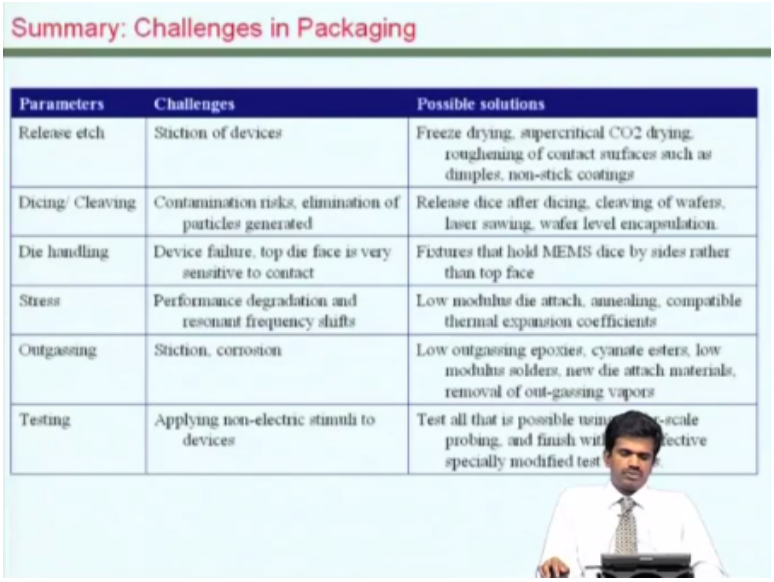

To summarise, some of the challenges involved in packaging of Microsystems include the release etch. If you recall it has associated issue of stiction. So, there are various approaches currently available to avoid stiction and you know the timing of release etch has to be performed after dicing and attaching this die onto this package space. So, during dicing, we have issues with microstructures being fragile and therefore we usually release the die after the dicing.

Die handling also we face some issues because of microstructures because we cannot hold them any longer with vacuum grips but alternate fixtures are required and can be made for this purpose. The stress in thin films or outgassing can also cause issues and there are ways of overcoming some of these by making use of alternative materials.

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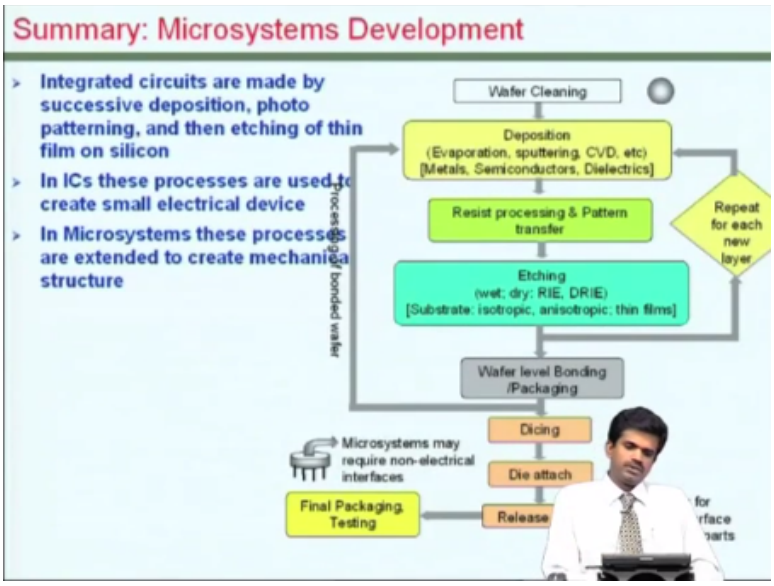

To summarise the development of Microsystems starting from the wafer to a packaged device is as you see in this flow diagram. We go through a series of deposition and pattern transfer and etching steps repeated a number of times to home form many Microsystems. In some cases, we include this additional step of wafer bonding to complete the process of fabricating Microsystems at the wafer level.

After this, the wafer is diced and these are attached to the package base and when surface micro-machine parts are involved, these will be released at this stage and will provide all the interconnects that are required to interface it with this external world.

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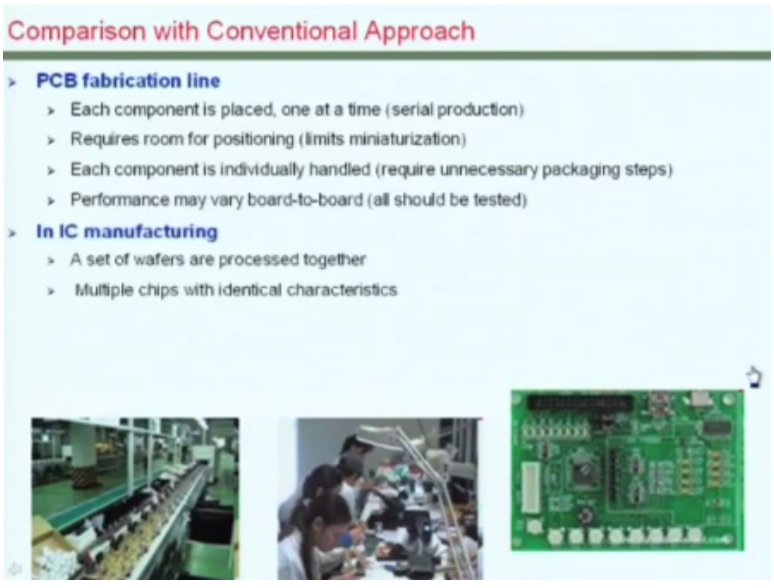

So, all these steps are equally critical in building Microsystems. If you recall, I started with comparing it with the conventional approaches of building part by part as you do in a conveyor belt approach. We attach part by part onto a printed circuit board in a conventional approach of building a system. So, an operator attach one component at a time. Compared to that the silicon fabrication approach that you saw in the previous slide is a batch approach in which a number of systems are built on the same wafer and these are integrated together.

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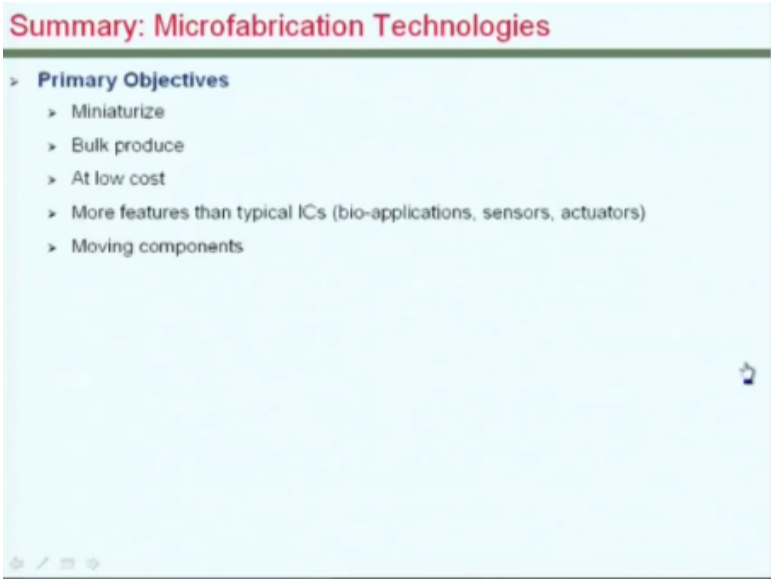

So you can see that the objectives in microfabrication ultimately are to miniaturise these systems and produce them in large number so that low overall coast for this individual systems. Several new features could be incorporated by bringing in new materials and new operating principles. As you have seen compared to integrated circuits, we can bring in moving parts by this microfabrication approaches.

In many Microsystems, we have this challenge of integrating electronics with the sensors or actuators and it is possible during the fabrication in some cases or during the packaging in many other cases. Ultimately what results in miniaturized Microsystems.

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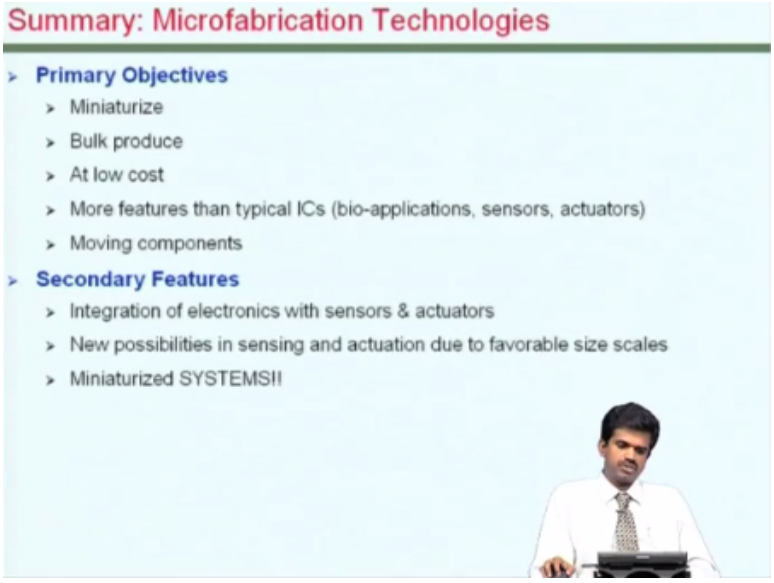

To probe further, I would like to suggest a recently published book on Microsystems which is authored by speakers of this lecture series. This book is currently available in India and an international edition is expected to be released in 2011. It has extended introduction of various sensing and actuation systems that are used in Microsystems. Various microfabrication technologies, modeling of solids and finite element methods and extended towards coupled electromechanical systems.

Electronics circuits that could be used in the context of Microsystems and how this could be integrated with Microsystems and packaged them together to come up with useful systems and several case studies are included. So, that could be an extension to this lecture series. So, with that, I wish to thank you for attending to this lecture. Thank you once again.