

**Micro and Smart Systems**  
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**Lecture - 07**  
**Microfabrication Technologies**

Good morning. My name is Prof. K.J. Vinoy, I will talk to you about Microfabrication Technologies, various aspects about it.

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**Microsystems**

- > **These are miniature devices or array of devices that usually have parts with electrical and mechanical operational principles**
  - > Sensors and actuators
  - > Energy conversion (electromechanical)
- > **Microelectromechanical Systems (MEMS) could mean:**
  - > Microsystems, Micromechanical systems, Micromachined Systems
- > **These are fabricated using extended IC Processing techniques (top-down/bottom-up processes)**

**They are...**  
smaller  
more functional  
faster  
less power-consuming  
and cheaper!

Let us start with microsystems you have seen in the previous lectures various aspects about these, these are essentially miniature devices or array of devices that usually have parts with electrical and sometimes mechanical and these operate with this electrical and mechanical operational principles. And there could be sensors, there could be actuators and in most of these there are some kind of an energy conversion which is usually electromechanical.

These are you know smaller and multifunctional devices and these compared to the conventional ones are faster and less power consuming and more importantly cheaper devices, and one of the very popular terminology for this is MEMS microelectromechanical systems and it could mean Microsystems, Micromechanical systems, Micromachined systems and all these terminologies are used in various parts of the world with somewhat similar meaning.

But we will try to stick to microsystems during these lectures. These are essentially fabricated using extended IC fabrication processing technologies and in fact with today's technology either a top-down or bottom-up approach could be possible to fabricate many of these. And we will see these fabrication approaches in today's and some of these subsequent lectures in this program.

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### Why Miniaturization?

- > Redundancy and arrays
- > Integration with electronics, simplifying systems (e.g., single point vs. multipoint measurement)
- > Taking advantage of scaling when scaling is working for us in the micro domain, e.g., faster devices, improved thermal management, etc.
- > Increased selectivity and sensitivity; Wider dynamic range
- > Cost/performance advantages
- > Exploitation of new effects through the breakdown of continuum theory in the micro domain
- > Minimizing of energy and materials consumption during manufacturing
- > Minimally invasive
- > Self-assembly and biomimetics with nanochemistry
- > More intelligent materials with structures at the nanoscale



First let us have a relook at why miniaturization is required in this particular context? One of the key is in terms of getting redundancy and so that you know when you have these arrays, this comes as an important feature point. Another important aspect is integration with electronics, so that when you build these mechanical parts or electromechanical parts this could be integrated with electronics required and that would simplify the system requirement point of view and enable a multi-point measurement.

The another requirement or another possibility that come up with this is miniaturization, with miniaturization is essentially scaling and you will see more details about this elsewhere in this program essentially with scaling with this kind of size scales we should not be able to make use of newer features and also get you know faster devices with improved performance from various aspects including thermal management.

And obviously when we make miniaturize devices there is a strong possibility that the selectivity, sensitivity, dynamic range and accuracy of measurements and all those things could

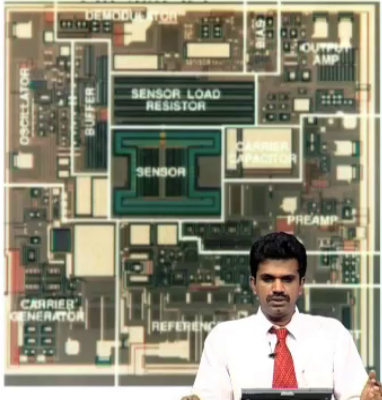
be improved by that, and we will we are likely to get cost over performance advantages because of miniaturization, we should be able to exploit new effects because of we know the size scales once again and you know less material consumption.

Because of the you know smaller volume consumed in fabricating these and in many instances you may have seen elsewhere these result in devices which are minimally invasive, it is also possible to fabricate many of these when they are small using approaches such as self-assembly and nanochemistry. More intelligent materials possible with that to build small structures at this nanoscale.

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**Three-axis integrated micro-accelerometer**

- > Mechanical sensing elements + electronic circuits for signal extraction, conditioning, and amplification
- > Examples:
  - > Sandia's three-axis accelerometer;
  - > Analog devices ADXL



The image shows a detailed view of a micro-accelerometer chip. The chip is rectangular and contains several distinct functional blocks, each labeled with text. These labels include: 'OSCILLATOR' on the left side, 'SENSOR LOAD RESISTOR' in the upper middle, 'SENSOR' in the center, 'CARRIER GENERATOR' at the bottom left, 'REFERENCE' at the bottom center, 'THRESHOLD' at the bottom right, and 'OUTPUT AMP' on the right side. The chip is mounted on a green printed circuit board (PCB). In the foreground, a man with dark hair, wearing a white shirt and a red tie, is partially visible, looking towards the camera.

One of the very popular examples of this is micro-accelerometer as you may have seen elsewhere, these have mechanical sensing elements and associated electronics you know signal conditioning circuits, amplification and you know event control circuits build in. And there are examples one of them is Analog devices ADXL device and this is one of the schematic of that which as you could see from there is sensor and a large number of you know components required in their electronics or ore integrated on board in this particular case.

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## Compared to Microelectronics

- > **Microsystems usually have**
  - > Moving parts...
  - > Capabilities to 'sense' the environment...
- > **Without the power to ACT it may not be possible to CONTROL!!!**



Compared to microelectronics as you could guess you know microsystems will have more of quite often moving parts and these should be able to sense from the environment, so there are several you know challenges in building systems based on this. You know in microelectronics you have everything we can build controls circuits, we can build you know signal conditioning circuits, amplifying circuits and also in microelectronics.

One key you know thing that is missing in this is that there is really there is nothing actually moving and without the power to act it may not be possible to control, let us say what is happening around you and this is a typical scenario in let us say you know a primary school classroom when the teacher does not have stick with him you know he may not be able to control the kids.

So the circuit that you are building if he does not have a block which can actually in a move in many situations when it is you know interacting with environment it is you know less let us say powerful, so we need to build circuits we need to build chips which have these moving parts and that is essentially the challenge in terms of microfabrication.

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## Microsystems vs. IC Technologies

- > **With IC technologies, we can**
  - > Miniaturize
  - > Bulk produce
  - > At low cost
- > **But Microsystems technology value adds IC technology by incorporating**
  - > More features (bio-applications, sensors, actuators)
  - > More fabrication processes
  - > Moving components
  - > Help ultra-miniaturize systems

Let us look at you know a comparison between what is usually done in IC fabrication technologies and let us evolve what is required for microsystems fabrication. In IC technologies we are essentially trying to miniaturize that is essentially the trend by bulk producing and all these have resulted in building chips at much lower cost.

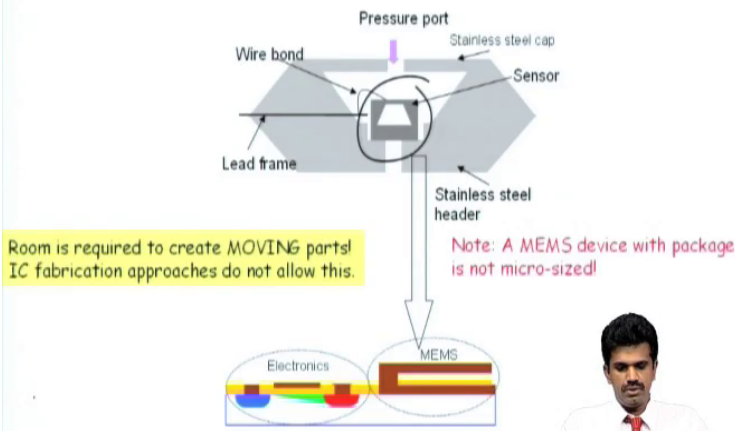
But in microsystems as I mentioned you need to build these additional features for various sensing and actuation applications and with moving components with obviously requiring you know additional fabrication processes, and in this way we should be able to miniaturize the entire system possibly within a package or even within a chip.

So in microfabrication technologies the objectives are essentially to like miniaturize and bulk produce so that it results in a low cost and we obviously want to build in all these extra features in to the chip and there could be secondary requirements such as integration new possibilities in terms of sensing and actuation you know various environmental quantities and thereby we can build overall miniaturized systems.

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## Fabrication Challenge

### A Packaged Pressure Sensor



One example another common example is pressure sensor, which essentially has a small chip in the middle which is actually you know package by this extra enclosure, so that you know the interface is possible and what is inside there could be you know based on the fabrication technologies that I have I will just talk during this lectures.

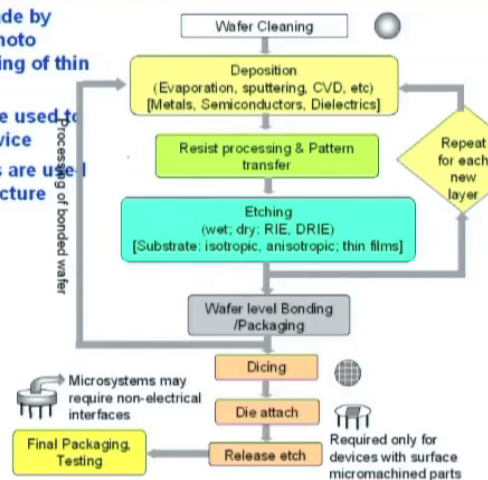
And you know if you really zoom it out we can see some electronics over there and also you know this microfabricated components which are required in sensing the quantity, it is you know one thing that we can notice at this stage is that although we talked about microsystems once it is packaged it is no more of that order it could be of the size the overall size could be of the order of millimetres or even you know centimetre for the overall packaged system.

But another key aspect that you should notice out of this is that unlike in ICs we need to integrate these moving components into these on the chip and that is really not possible the conventional IC fabrication approaches.

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## Microsystems Development

- > Integrated circuits are made by successive deposition, photo patterning, and then etching of thin film on silicon
- > In ICs these processes are used to create small electrical device
- > In MEMS these processes are used to create mechanical structure



Now for the microsystems development the flow that you follow is quite similar to what is done in IC fabrication. We start with clean wafer and do a series of steps such as deposition and patterning which are done repeatedly and then we do some sometimes we do wafer bonding and we also and that again can be followed multiple times, and ultimately after all these are done we dice them into individual chips and then attached the package and then package will do that.

In the lectures that follow we will essentially focus on the some of these coloured blocks, whereas the dicing, die attach and those steps will be discussed when we discuss Packaging of microsystems separately during this program. So in the key differences here are that we make use of the etching extensively in the fabrication of microsystems.

Whereas in microelectronics we you know quite often we will be requiring several doping or ion implantation kind of process steps at this stage and you know although we will still have this resist you know deposit and resist patterning steps cycled even in the IC fabrication. So these modifications are required and we will see how you know these minor looking modifications would can be exploited to result in moving components for building microsystems.

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## Comparison with Conventional Approach

- > **PCB fabrication line**
  - > Each component is placed, one at a time (serial production)
  - > Requires room for positioning (limits miniaturization)
  - > Each component is individually handled (require unnecessary packaging steps)
  - > Performance may vary board-to-board (all should be tested)
- > **In IC manufacturing**
  - > A set of wafers are processed together
  - > Multiple chips with identical characteristics



Let us at this stage let us also compare this fabrication approach to a more popular conventional approach. One example is building a printed circuit board, in a printed circuit if you have actually seen a fabrication line for a printed circuit board you know it is done by what is normally called a conveyor belt approach where on to a bare board each of these components are attached one after the other.

And you could also probably seen you know technicians lined up you know attaching components one by one, now in this case the key is that each of these components are attached you know sequentially and this require you know one room around it the space around them for so that these could be positioned on to this board and as you could see these are individually handled.

So you know they require lot of process, lot of steps and lot of time and lot of manpower or even mechanical power to build such a board and associated with that you know the challenge is the performance could vary from board to board and hence almost all the boards should be tested for reliability, whereas what you have seen in the previous slide we are essentially taking wafer at a time and inside that on the wafer you are building dozens of hundreds of chips.

So all of them are likely to be identical and actually in industries not just one wafer it is actually a set of wafers are processed simultaneously, so the variation between one chip to the next is



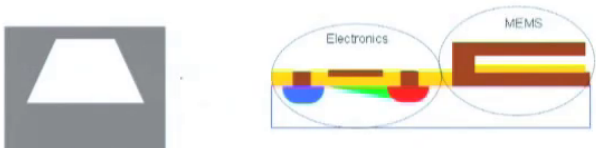
marginal, so the testing requirements would be minimal, the processing would be less complicated as compared to the conventional approach for system building.

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**Description of a typical fabrication process**

Shallow pits were etched into n-type substrates, and p-type deflection electrodes were diffused in the above pits, followed by fusion bonding of a second wafer above the first. The top wafer was then ground and polished down to a thickness of 6  $\mu\text{m}$ . A passivation layer was then formed on the top wafer and sensing piezoresistors were formed using ion implantation, after which contact holes for metallization to connect to the diffused deflection electrodes were etched. Bond pads and interconnect metallization were then deposited and patterned, followed by etching of the diaphragm from the back of the wafer. Finally, two slots were etched next to the beam to release it over the buried cavity.

(Petersen et al., 1991)



Now let us look at you know how the processes are arrange, which are the process that could be required in building a typical microsystem, what you see here is one of the oldest example of building reported for building a micro system in this particular case a pressure sensor. And if you read through the passage over here what we have is that if you see coloured is that a series of process steps many of these are you know are used in IC fabrication as such.

And some of these are you know little tweaked or little modified comparative what is required in IC fabrication. Diffusion is a process steps commonly used in IC fabrication in you know in terms of modifying the dopant level of different layers. Bonding is rarely used but it is also rarely used in IC fabrication but you know highly required in many microsystems.

Polishing steps are once again you know rarely used in microfabrication, we will see that some of these are very much required in building microsystems. Ion implantation once again is common in IC fabrication, metallization is common, deposition steps and patterning are also common in IC fabrication but you know what really is stands out here is that there is an etching step here which is required to you know for creating the diaphragm that is required in the case of a pressure sensor.

So we will see how some of these process steps are arranged and are performed to build microsystems such as this.

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### Important Useful Technologies

- > **Lithography and selective patterning**
  - > Photolithography
  - > Lift-off technique (lithography + metallization)
  - > Chemical/plasma etching
- > **Vacuum technology**
  - > Cleanliness, Transfer of materials without contamination
  - > Repeatable processing
- > **Plasma technology**
  - > Created in vacuum (with selected pure gases)
  - > Ion-bombardment to modify materials
  
  - > Selective etching
  - > Deposition
  
  - > Change surface chemistry
  - > Change surface morphology



It is also necessary to have a closer look at some of the technologies that are in world. Lithography is essentially the patterning technique that are followed in many ICs, nowadays there are more advanced techniques such as lift-off used in lithography and in patterning in ICs, and it is also possible to use either of these to pattern a smaller layer in microsystems.

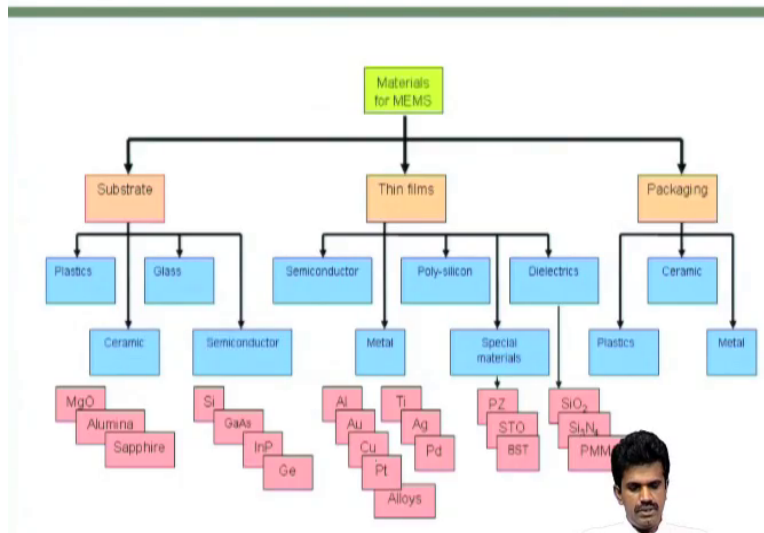
It is possible to use wet chemistry based or even a dry etch process steps to etch various layers in order to pattern them in building microsystems and which is very similar to that is there in IC fabrication. Another technologies that is used in building ICs as well as in microsystems is Vacuum technology, which provides cleanliness it provides environment in which materials could be transferred from one to another ensuring you know purity without contamination.

And this essentially held in realizing repeatable application processes. Another key process that is used in microfabrication as well as in IC fabrication is Plasma technology, this is required in many of the deposition processes and it is also used in many of the etching approaches, so essentially you know what we require is process technologies that would allow selective etching and deposition of different layers.

Sometimes it is also required to have you know work with chemistry so that the surface properties could be modified so that you know the adhesion between layers could be improved and also in terms of you know changing their morphology.

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## Materials for MEMS



A large number of materials could be used for the fabrication of MEMS and microsystems. We can start with a substrate which is essentially the support material and you know on which we are building these chips. In ICs we are always bound with the semiconductor substrates, but in mini-microsystem the substrate by itself is only a support material and hence need not necessarily the semiconductor.

So we can even think of glass or plastic substrates for building microsystems especially those did not require on chip integration with electronics, the fabrication of most let us say most of these microsystems we would require working with themselves as I mentioned depositing them and patterning them sequentially. And one of the finest steps in building microsystems is you know packaging the individual dice and various materials are used in packaging and which is similar to the case of integrated circuits.

Now if you look at individual materials that are used we can think we can look at various semiconductor materials for the substrate and as you could see from here base on that let says

where you will see that silicon by far is the most widely used material as a substrate material for microsystems as obviously in the case of integrated circuits, for various reasons as you will see later in this lecture.

All these you know metallic and non-metallic materials used as thin films in building microsystems, so let us now look at them in you know from a different perspectives.

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### Functions of Various Materials in Microsystems

- > **Substrates**
  - > Mechanical support
  - > IC compatibility
- > **Thin films**
  - > Structural
  - > Sacrificial
  - > Dielectric (polymeric/ceramic/silicon-based)
  - > Semiconductor (epi-layers)
  - > Conductor
- > **Usually thin film materials may have multiple functions**

The substrate materials are used as I mentioned primarily for the mechanical support, it is as I said when there is electronics to be integrated if it is a semiconductor substrate it provides the compatibility with the electronics that are there. Thin films are essentially required in building those structural members that could possibly be moving, thin films are required from the IC perspective are required from the dielectric properties, semiconductor properties and conducting properties.

So we have all these kinds of thin film materials and from the MEMS perspective from the microsystem perspective this could even be called structural materials, we will talk about these again a later. Thin film materials as you could see we can have multiple functions for example from the microsystems perspective there could be for a structural aspects, whereas from the electronic perspective this same thin films could be working as dielectrics again we will see them in action a little later.

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**Substrate Materials: Silicon**

- > **Silicon is used widely for mechanical sensor applications,**
  - > mechanical stability
  - > feasibility for integrating sensing and electronics
- > **Electrical Properties**
  - > Conductivity type, dopant
  - > Resistivity, Sheet resistance
- > **Wafer types**
  - > Prime Grade
  - > Reclaim Grade
  - > Test Grade
  - > SOI
- > **Crystal types**
  - > Covalently bonded structure
  - > Diamond cubic structure( same as carbon in diamond)
  - > belongs to zinc-blende classification.
  - > Silicon with 4 covalent bonds, coordinates itself tetrahedrally.
  - > These tetrahedrons make up diamond-cubic structure

As I mentioned the most popular substrate material is silicon, silicon has very good mechanical properties in addition to its electronic properties and because of that it is widely used, and obviously it is semiconductor material and hence integrating electronics is easier if we use silicon as a substrate material. Suppose if you know that its electrical properties could be changed by adding dopants and with which you can even change the resistance or the surface resistivity of that.

You get various types of silicon wafers and you could choose these based on the requirement, the silicon wafer you know usually also the type grade also decides the cost of the wafer. It is also possible at this stage to get a wafer called SOI wafer Silicon-on-Insulator wafers which are essential processed wafers and are used widely this is for many microsystems requirement.

Silicon is a crystalline material this has basically atoms arranged in a particular order and this order is essentially repeated all over the crystalline wafer that is available to us that we can purchase commercially. It belongs to what is called zinc-blende classification of crystal structure. In silicon as you may know has you know 4 electrons in the outer band and hence has 4 covalent bonds and these essentially help in terms of arranging these atoms tetrahedrally within this crystal.

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## Miller Indices

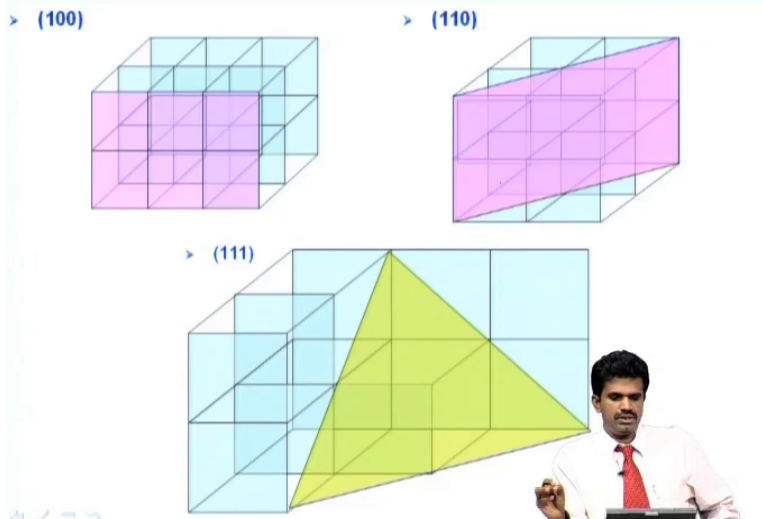
- To identify a plane or a direction a set of integers  $h, k, l$  called **Miller indices** are used.
- Conventions in notation to identify
  - $[\ ]$  a specific direction;  $\langle \rangle$  a family of equivalent directions
  - $( )$  a specific plane;  $\{ \}$  a family of equivalent planes
- Directions  $[1\ 0\ 0]$   $[0\ 1\ 0]$   $[0\ 0\ 1]$  are all crystallographically equivalent and form the group  $\langle 1\ 0\ 0 \rangle$  direction
- A bar above an index is equivalent to a minus sign.

Let us now look at how crystalline geometries could be studied in you know especially in the context of this silicon one of the approaches for that is based on what is called Miller Indices and this is done basically by identifying a plane or a direction and it is this Miller Indices are used for this purpose. The some conventions used in this, basically if you use square bracket it specifies a particular direction and if you round brackets it specifies the plane.

And if use angle bracket it means essentially a family of equivalent directions I will talk about it a little later. Similarly, if you use braces it indicates a family of equivalent planes, for example what could be termed as  $[1\ 0\ 0]$   $[0\ 1\ 0]$  or  $[0\ 0\ 1]$  are all crystallographically equivalent we will see what are these, and these could actually be represented with a  $\langle 1\ 0\ 0 \rangle$  with an angle bracket. You will see that a bar placed above this index is used to indicate a minus sign in specifying the crystal direction.

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## Understanding the Crystallography of Silicon



First let us see what is some of these crystal directions that are commonly used, assume that you have a co-ordinate axes  $x$ ,  $y$ ,  $z$  axes defined and as you could see from the figure on the left a plane which is parallel to any of those axes could be in fact what is called a 100 plane, a plane which is diagonal to 2 of those axes and parallel to one is typically called a 110 plane, and a plane which is not parallel to any one of those axes is you could see from the third figure here is a 111 plane and let us see a little bit more what these are based on the definition Miller Indices.

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### Miller Indices

- > **To determine Miller indices of a plane,**
  - > take the intercepts of that plane with the axes and
  - > express these intercepts as multiples of the basis vectors  $a_1$ ,  $a_2$ ,  $a_3$ .
  - > Reciprocals of these intercepts are taken to avoid infinities,
  - > multiplied by LCM to convert it to integer. This removes common factors.
- > **Example -1**
  - > A plane intersects the crystallographic axes at  $(2,0,0)$ ,  $(0,4,0)$ ,  $(0,0,4)$ .
  - > Step 1:  $(1/2, 1/4, 1/4)$ ; multiply by 4 to express as smallest integers.
  - > Step 2:  $(2, 1, 1)$  are the Miller indices. This is a  $(211)$  plane.

$$\left. \begin{array}{l} (1, 0, 0) \\ (0, 1, 0) \\ (0, 0, 1) \end{array} \right\}$$



What do you normally do to define Miller Indices is to find out the intercepts of the plane with the coordinate  $x$ ,  $y$ ,  $z$  axes and let us say that  $a_1$ ,  $a_2$ ,  $a_3$  are these intercepts. We take the



reciprocals of these number essentially to avoid infinities and then find the LCM and then you know multiply with this LCM to get the Miller Indices for the particular plane.

For example, if you have a plane which is intercepting with 2, 4 and 4 with respect to the x, y, z axes you can choose the numbers 2, 4 and 4 from this example and in the first step we could write 1/2 because we need to take the reciprocals, so we take (1/2, 1/4 and 1/4) and the LCM is essentially 4, so we multiply by 4 and we get the Miller Indices has (211). So this is essentially a plane that is intercepting with these points of and the co-ordinate axes is called a (211) plane.

So similarly, when it is intercepting with only you know let us say x axis at point (1, 0, 0) and if it is parallel to x and z axis we can work out in the process steps that are discussed here and we can find out that it is one of those planes that you saw in the first example in the previous slide. It is also possible that you know any even if it is intercepting with (0, 1, 0) or (0, 0, 1) with respect to the x y z axes it is you know these are whole parallel to one of those axes.

So when atoms are arranged in a cubic fashion it does not matter whether it is parallel to the x axis or y axis or z axis, hence all these are you know essentially identical in this particular context and that is why in the previous slide we have seen on the crystallographically identified and we collectively called them a (1, 0, 0) or similarly, in other cases.

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### Miller Indices- Example

> A plane intercepts x,y,z axes at 2,3,4 respectively.

- > Points of interception: (2,0,0); (0,3,0); (0,0,4) ✓
- > Equation of this plane is  $x/2+y/3+z/4=1$

> Reciprocals: (1/2, 1/3, 1/4) ✓

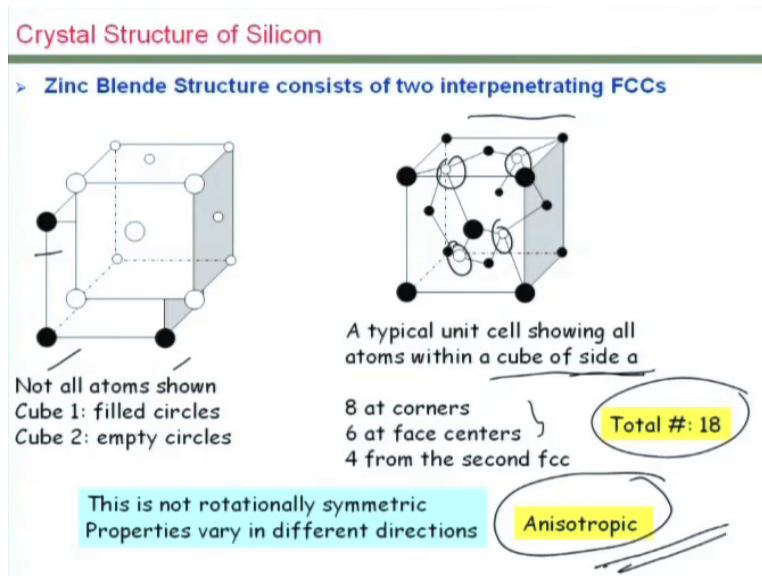
> LCM 12 ✓

> Multiply with LCM

> Resulting: (6,4,3) ✓

So here is one more example let us say that we intercept at point 2, 3, 4 and we can work out, we can find the intercept points and we can find the reciprocals and find the LCM and we can find that the resulting Miller Indices are like this. So going back it is possible that you know the surface of the wafer is aligned with any one of these planes when you purchase them, and hence the wafers this different types are there.

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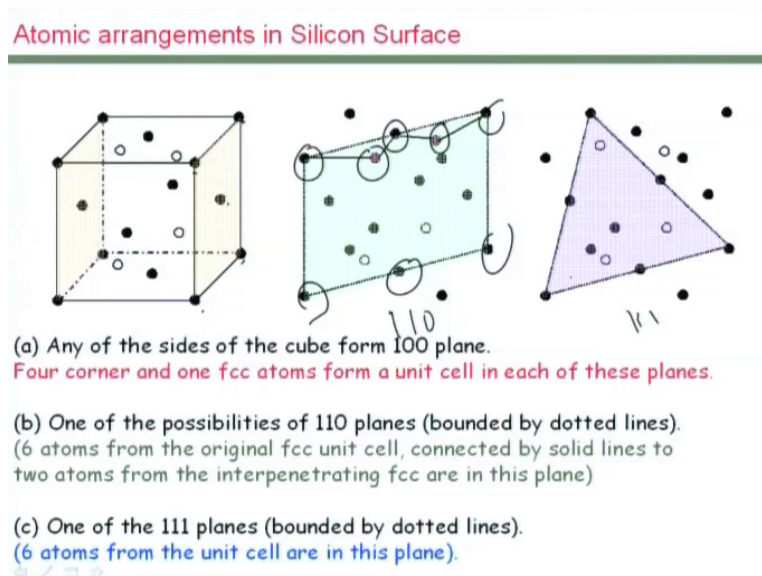
Now why is it that we have all these different types of wafers and what makes difference as I mentioned in the case of silicon is essentially a zinc-blende structure which is consisting of 2 cubic lattices which are essentially interpenetrating FCCs. So in the example in the schematic here the 3 atoms from one of the cubic is marked with this black darkened circles and some of the atoms from the second interpenetrating FCC are marked with this hollow circles over here.

So if you actually look at one unit cell with side  $a$  you will see that there are all these 8 atoms coming from the from the corners of the cubic cell, there are 6 atoms at its FCC so essentially this set belong to one full cubic cell, and then there are these additional 4 atoms shown with this hollow circles over here which are coming from the second interpenetrating lattice. So all together in a cell a cube of side  $a$  we can have 18 atoms in the case of silicon.

And now if you try to slice these crystals along let us say the (100) plane or (110) plane obviously the atoms on the surface could be different as you could see it is not rotationally

symmetric, hence the properties of silicon could be different and it is also different when you approach in different directions. So the chemical properties, the surface properties of silicon wafers could be different based on the crystal directions.

And hence in many cases you will see that the silicon properties are anisotropic in fact in building many microsystems we make use of this anisotropic in building microsystems.



So here is the example what I said if you take 100 wafer and if you see surface atoms you will see that anyone surface you will have these different atoms coming from the surface belonging to these lattices and there are essentially 5 atoms in 1-unit cell, whereas if you see 100 sorry 110 surface you will see that all these atoms are on the surface of a 100 wafer.

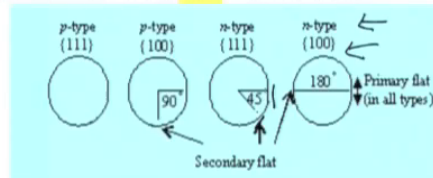
And similarly, in the case of 111 wafer you will see that there are these 6 atoms on the surface belonging to 1 unit cell, all the other atoms are essentially within below the unit cell and these are essentially linked to it and these are strongly bounded as you could see from here, the surface of the 111 has it very strongly bounded to the atoms inside and hence it displays them and you will see that again as I mentioned that these properties are made use of in processing the silicon wafers conveniently for building microsystems.

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## Identification of Various Silicon Wafers

### > Location of primary and secondary flats

#### > Convention followed for small diameter wafers



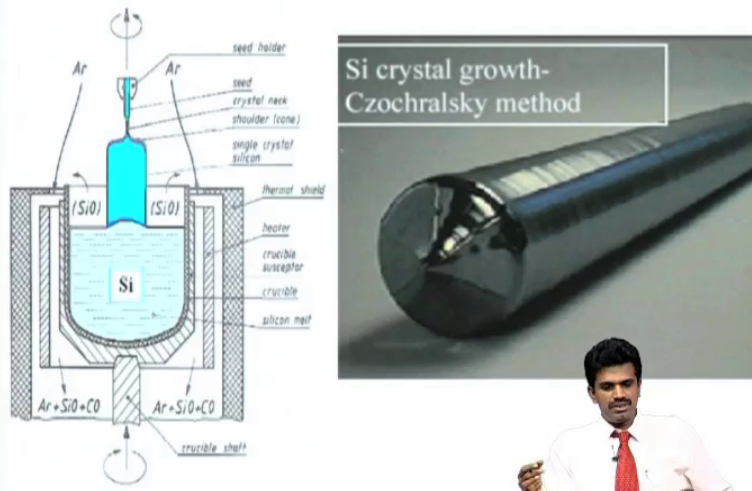
Wafer Diameter	100(4")	125(5")	150(6")
<b>Parameters</b>			
Primary flat (mm)	30 to 35	40 to 45	55 to 60
Secondary flat (mm)	16 to 20	25 to 30	35 to 40
Bow (mm)	60	70	60
Total thickness variation (μm)	50	65	50
Surface variation	(100) or (111)	(100) or (111)	(100) or (111)

For the identifying the silicon wafers with different crystal orientations and different doping types in some convention is followed. This is essentially true for wafers with small diameter which are typically used in university labs, for larger wafers which are used in you know industrial foundries these conventions are not typically follow. And as you could see that what we have is essentially these 2 flats.

So it is although we normally indicate wafer with full circles it is not show this up to small you know flat edges which is slightly difficult to see from the images here, but still you know with different dimensions and different relative location and that are essentially used in identifying the type of the wafer when you have one with you.

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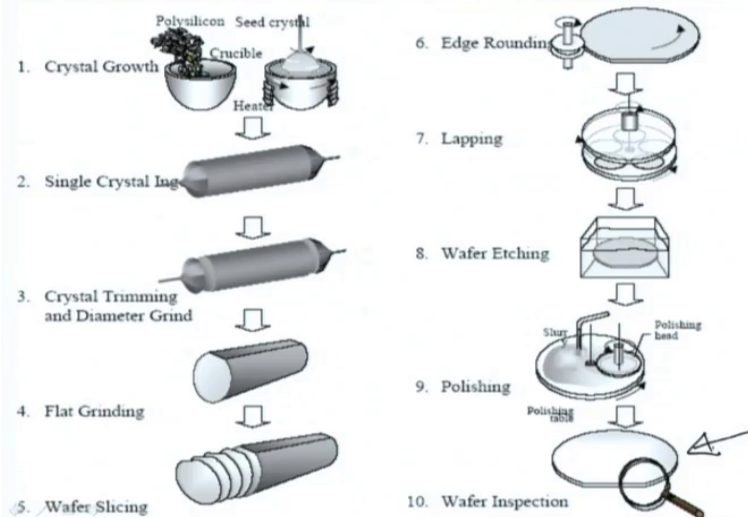
## Czochralski Crystal Growth Process



The fabrication of silicon wafer although we hardly follow those in university lab, you almost always buy the silicon wafer from the vendors but still it is interesting to see how you can get that silicon wafer out of silicon.

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## Silicon Wafers



So we you know have a series of process steps essentially you know fallout to build a single crystal which is fashioned you almost like a cylinder, and essentially run through a series of steps further to final year result in a completely flat wafer. So it is essentially by melting the silicon or which is essentially a high purity sand that you get silicon as a source material, and it is absolutely critical that at this stage itself the crystal orientation of the silicon is defined.

And further on it is essentially shaped, it is made into the flats that I indicated or engraved on it, and further it is sliced into this individual wafers and polished to mirror finish as you probably of seen some of there and then you know inspected and provided us for processing those for building various microsystems and you know ICs.

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### Useful Characteristics of Silicon

Sensory	Mechanical
Piezo resistivity	Better yield strength
Thermal property	Lower density
Optical property	Better hardness

- **Silicon is the most widely used substrate for microsystems**
- **Yet Silicon is NOT usually used in some cases:**
  - For very large device size
  - Low production volume
  - When electronics in not needed or cannot be integrated



Apart from the mechanical and the electrical properties that we have what we know in the case of silicon, it also has some very interesting properties which could be exploited in the context of microsystems, it exhibits an essential property called Piezo resistivity. That is you know by applying a stress the resistance could be varied, it has very good thermal characteristic, it also has some optical properties you must be familiar with photodiodes and other devices need of silicon.

So because of some of these additional features many more microsystems could be built on silicon then that are possible in other substrate materials, hence silicon is the most widely used substrate materials in microsystems, yet silicon is not the only material there are instances when you really need to build a large area device and then you know silicon is probably not the best suited material.

And it is also you know instances when the production volume is not large enough to go through the process steps that I have you know briefly indicated previously, and then also cases where

electronics need not be integrated on chip, so in such cases the non-silicon materials could be used for building microsystems.

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**Other substrate materials...**

- > **Gallium Arsenide**
  - > Second most common semiconductor
  - > Disadvantages
    - > Does not form sufficient quality native oxide;
    - > Thermally unstable above 600°C due to As evaporation;
    - > Mechanically fragile
- > **Other options**
  - > Glass, Fused Quartz, Fused Silica

**Performance of various substrates (for general MEMS / IC applications)**

Substrate	Cost	Metallization	Machinability
Ceramic	medium	fair	poor
Plastic	low	poor	fair
Silicon	high	good	very good
Glass	low	good	poor

One of the other popular substrate material again a semiconductor material is gallium arsenide, it has you know particular advantages especially for building radio frequency and some optical devices, it also has some disadvantages you know especially in terms of building you know thin films on it and also processing at high temperatures you know building truly mechanical components. There are of option such as glass and even plastics that could be used for building microsystems.

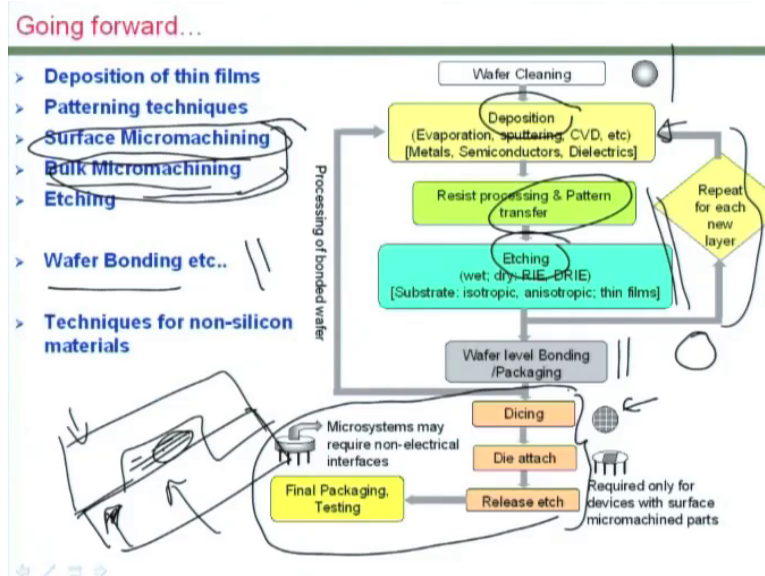
So we could you know at a higher level we could compare the performance of this substrate materials, as you could imagine a plastic or glass based substrate material will have very low cost compared to silicon. Ceramic material cost although it is indicated as medium here it could actually you know range from you know medium to in fact extremely high based on the quality of the ceramic material that we want to choose.

Metallization properties are typically good for silicon and glass usually it is you know little difficult to deposit metals on to a plastic but it is still possible. Machinability as you could imagine machinability is essentially the processing to shape different structural parts out of the



substrate material and as you could imagine it is very good in the case of silicon, and you know some of the ceramic materials it is very difficult to build such you know mechanical parts.

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So going forward in the subsequent lectures what we will see is that how silicon and other substrate materials that you have seen could be started with and how some of these process steps could be done to build really what are called this moving components and you know so that we can build microsystems. Let me give you a brief overview of how these are done.

We essentially want a film or a part of the substrate which could be left in such a way that it is allowed to move or there is some room to move, so what we need to do is that we need to extensive you know patterning and etching steps, so that this room can be created, the space beneath can be created on the substrate or on the thin film material that you have actually deposited by tweaking the process.

And this is usually done conventionally by 2 of these approaches indicated here, this is essentially a series of process steps that you see over here organized in such a way that either a thin film or the substrate by itself is processed to create this 3 dimensional space around it, so that it could be (()) (48:33).

In surface micromachining as the name indicates what we are trying to is that we are trying to machine in a conventional sense, trying to chemically process strictly speaking the thin film so that it has some room beneath it, think about it, how can we have a room or a space beneath a thin film, a thin film has to be attached to the surface of the substrate. The question is how can we create room beneath it, and that is essentially what the beauty of the approach that you will see later.

What we are trying to do there is that we first deposit a dummy material thin film and then at the film that you really want to retain and selectively remove the film underneath the so that the dummy material that I mentioned so that we will be able to leave the second material the structural material that we added.

So as you could see it is very critical that we work with the chemistry of these materials we understand how some of these materials react to you know chemicals and we identify suitable chemicals so that you know it only attached let us say the dummy materials as I indicated here, and note the structural material that we would want to add. So by having these 2 thin films in addition to the substrate material we can work on what is called the surface micromachining.

So in surface micromachining what we are doing, what we will try to do is to build a free standing thin film above the substrate. In bulk micromachining on the other hand we tried to dig into the substrate material itself and create room there, for example earlier I talked about a pressure sensor where there was a cavity below a diaphragm membrane.

To create such large cavities it is not enough that we work a thin film, we probably need several tens of micrometre depth cavities and it is really not possible to build thin films as thick, so what is done there is to basically you know try to remove the substrate material and by etching and you know so that we can create that large cavity the deep cavity below a thin diaphragm.

It is usually so again it is not possible to you know work on the bulk of the substrate material without creating a hole from the open area, and obviously you know it is not possible essentially to create a cavity like this working from the top side you will have to work from the back side, so

you know in the case of microsystems usually one would require what are called you know double sided polished wafers.

So that we can process partly from this side and partly from the back side, so you know what we get here is you know then with bulk micromachining approach that I am indicated what we get here is an open cavity. Now to create a closed cavity we may want to do steps such as you know adding a separate wafer bonding back side and that is done by what is called wafer bonding approach.

So in wafer bonding what is done is that before the individual dice are separated while the full wafer is being handled, you are essentially adding multiple at least 2 different wafers together, in such a way that we can have this kind of closed cavities, so building closed cavities is possible with you know what is called is wafer bonding approaches.

So in subsequent lectures we will talk about various approaches for deposition and we will see how patterns transfer is performed on to this deposited, we will see various approaches for etching, and we will see how these are you know organized in such a way that you know we can have freestanding films or freestanding substrate parts by surface micromachining or bulk micromachining.

And then we will also see how you know wafer bonding approaches could be used in building in a closed cavity kind of devices which involved closed cavities or really thick devices possibly even consisting of different substrate materials. And as I indicated the steps that are listed towards the end which are dicing, die attach and you know releasing and all those things.

And packaging with respect to electronics will be discussed later in this program and where we will see some examples in which you know devices made microsystems made out of the process steps here are actually attached various you know the packaging solutions currently available so that it can actually be used for real life applications. So I thank you at this stage and I will come back to you with more details of the process steps that are here. Thank you.