CMOS Analog VLSI Design
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Lecture – 05
Basic of MOS Amplifier (part-1)

We were looking for MOS amplifiers and we are still rush to model PMOS transistor last time I do some figures.

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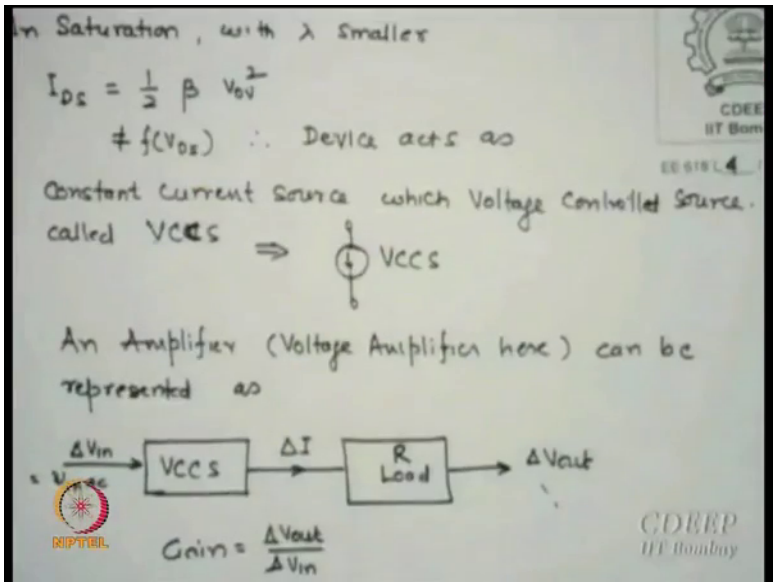

One of them; I said that in saturation the ideas which is the drain to source current is equal to half VOV square half beta VOV square and we show as if it is not a function of VDS and we later showed that it is a function of VDS through a lambda term; however, if you look at this expression you can see it is like a voltage control current source. So, typical amplifier has a schematic diagram one can if you wish to say I put of input ac which is essentially delta input delta changing a wave I pass through VCCS that is VGS minus VT is what we are now looking into which converts into change in current because this is the current.

And this current is then passing through a node which gives the output voltage V out. So, essentially a typical amplifier which we are going to use will have a current source which is a function of input and then it goes through a load going in a output voltage and the change in output voltage means ac voltage. So, ac voltage by ac input is essentially the

gain that is what an amplifier is likely to do. So, the essential part therefore, was to get this expression correctly and also we will like to see whether the load which we always talked about is that really resistive load or there is something else which we can do we will see little later that typically in the case of integrated circuits there is no register as such is employed.

Because of the area it will take, we will show you how much it make and therefore, you know transistor itself as the resistor or equivalent current source. So, we will see; that means, we need to create a current references or current sources that is one of the activity of this course. So, we will see how to create a good current source what is the property of a good current source the impedance across it should be infinite ideal current source. So, how good we reach their how good and that is one is important point and that is the design because other why is you can create anything and you will say there is a good current source, but the output impedance across that should be as high as possible preferably infinite.

But infinite is a number which is unknown. So, maybe say hundreds of mega ohms that is the big number. So, you say that is good enough. So, this is the basic idea which we are following and we continue to follow now there is some issue which may appear now we always thought transistor behaves in a very interesting nice simple way, but it does not unfortunately particularly if there is a short channel device it will being inverse even make a long channel.

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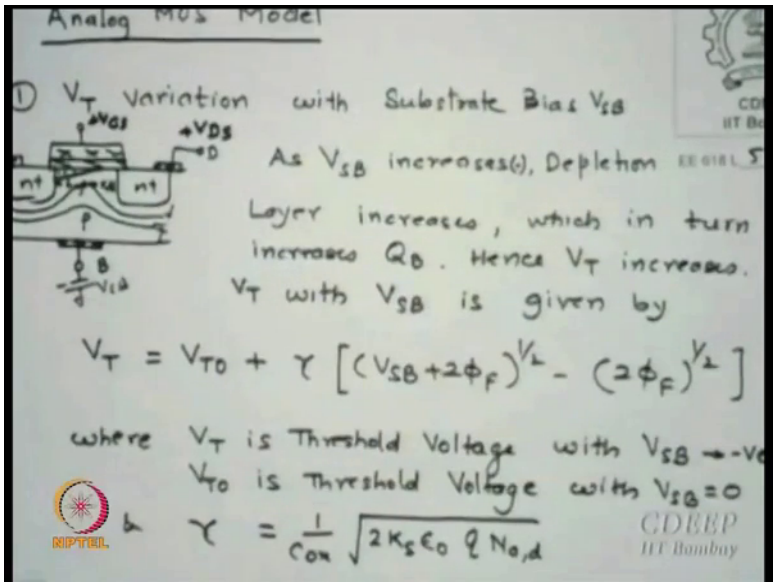

We would like to now see; what is the equivalent circuit of a MOS transistor which I can employ in circuit designs.

So, I figure it out there are many other issues which I have yet now discussed and one of the issue which I start with is I shown threshold was constant on real life this threshold is not really so much constant as I think. So, and it has been figured out that if I apply a substrate bias negative substrate bias what will happen you can see from here this is source to 100 drain is plus VDS for a MOS transit to work plus VGS which is exceeding VT. So, if I apply minus bias to source substrate junction.

So, one can see there are already a depletion layer even at 0 bias, if you applied reverse bias it will further enhance, on the drain side it already had a larger depletion because of VDS was positive with minus VSB, it will be VSB plus VDS. So, it will be additional reverse bias now available at the drained a substrate junction. So, the depletion layer will be even enhanced there. Now 2 things which is available one is of course, there is a extra depletion charge in the channel; is that clear? There is an extra depletion charge before VGS there is a extra depletion charge which is available to you; there is another issue which we will look into later since the depletion layer changes what changes in the normal diode; the depletion layer thickness is related to what.

Student: (Refer Time: 05:17)

Capacitance epsilon s by xd. So, larger the Xd capacitance will come down. So, there is some issue which we have to take care in circuit design when we say if you have a VSB the capacitance also it is a function of VSB now looking at that part later since the bulk charges in the channel area is increasing we know the expression which we are written for VT which has a term qv by Cox phi m s 2 phi F Cox by Cox minus qb by Cox that time the bulk charges were essentially because of the VGS that is what we said EAX is very large and whatever depletion is occurring essentially because of VGS.

But now you have created additional source for depletion charge which means now VT will become higher because already there is a. So, you have to first remove that to get into a inversion layer is that clear now this essentially means that the new VT with additional minus VSB sitting there will be VT 0 0 bias VT which is normally we were considering gamma times; now what is this is the difference; I am adding this is the original plus how much additional VT contribution will come because of the additional charge available to you. So, what is the now the surface potential VSB plus 2 phi F because earlier it was only 2 phi F; now there is a minus VSB on that that is plus for reverse. So, VSB plus 2 phi F is the potential now.

So, psi s is now becoming VSB plus 2 phi F to the power half under root expression we know minus without this; that means, without the VSB. So, this additional this terms multiplied by q; gamma which essentially is the part of this Xd expression which we wrote there qv expression which we wrote there one upon Cox twice ks epsilon naught qna and d means why about aid is Na for P n channel device nd for P channel device. So, one word one can say.

This is the small query for those who are very keen about devices is Na should be higher than nd for n channel and P channels Na nd will be equal for P channel n channels all n channel nas will be different from P channel nds what is your criteria do you think something about as the numbers; which one should have different dopings; for example, I may give a hint that Na nd will not be equal. So, which should be higher and which should be lower.

Student: (Refer Time: 08:13) Na (Refer Time: 08:15)

Na.

Student: Higher.

Higher for n channel compared to nd because we have wrote a P channel expression all terms were negative. So, I do not want Vd to be very large negative for P channel. So, actually for reduce nds VT will go down if I increase Na that compensation term will be increasing. So, a VT will increase actually positively and a all circuit designs preferably and not necessarily V VT that is threshold of n channel is kept as much same as P channel, but in analog this may not be a criteria in digital CMOS; this is general criteria because of the swing to be equal we always put VTN equal to VTP in digital, but in analog that is not a compulsion in many times I will not do that so, in which case my 2 devices will have different dopings.

So, that I can adjust my VTS independently is that point clear. So, this VT now has enhanced compared to its 0 bias case and that should be taken care because if that is. So, we will like to see of course, this expression.

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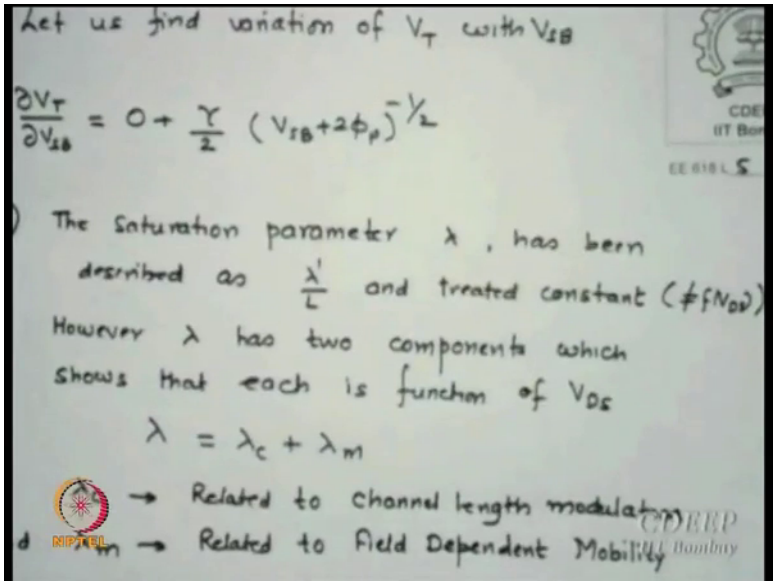

We will use later I just want to show that may vary the threshold variation is VSB which is gamma by 2 VSB plus 2 phi F to the power just differentiate. So, we see change in threshold voltage with subset bias; obviously, here is a minus value plus gamma by 2 VSB plus 2 phi F to the power minus half that half will come and minus will appear due to differential.

So, this is one issue which in analog people have to worry now this question may be asked in normal technologies which we use you just write down, then I will come do not re-write read this, just go up to this, we will come back to the second issue little few minutes.

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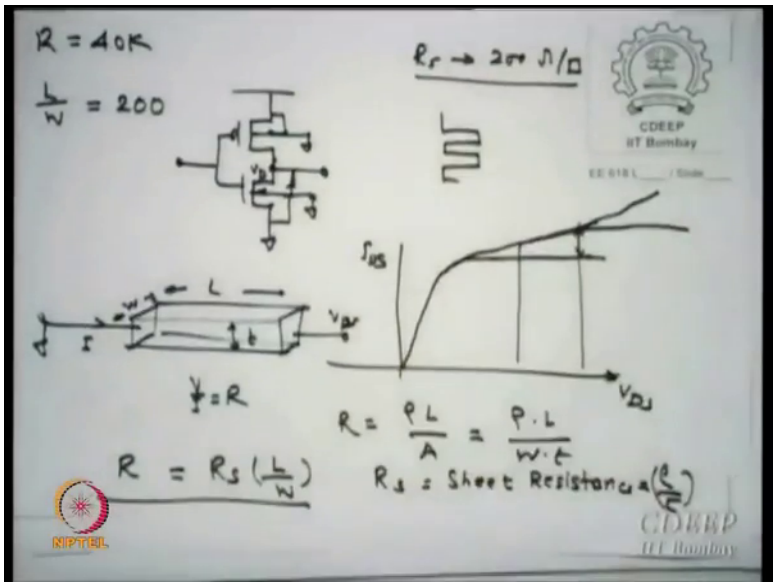

So, if I am showing this in normal I will come back to this figure again in normal CMOS which is what digital inverter are using this is the P channel device this is the n channel device what I see there that the bulk for P channel and bulk for n channel are normally connected to sources sorry normally connected to sources.

But in most circuits these days because we want to control VT through bias what we do either we leave this separate or at best we ground them; is that clear, now if we ground because that is what control we need. So, if we ground it now you can see the any potential whenever current pass thorough this n channel there will be a potential drop here the center point which is the output point will have a voltage VDS of the lower transistor this voltage here whatever is the VD of the lower transistor is actually VS; VD of the upper transistor also is that clear.

That means there is a substrate bias between gains had to be ground because the bulk is grounded. So, even if you are not really putting any VSB or VDB there is a built in substrate bias is created which means the threshold of these 2 transistor will vary even without doing anything is that clear. So, now, one must worry that in real technologies

where I am not actually connecting source and bulk together this issue will be of relevance because in that case only, then I know I can control VT and now I start doing I just ground it or may times I do not even ground it I actually leave it open put a bias whatever I want there in those cases there will be built in VSBS or VDBS available which will modify the VTL and this is another issue which one has to worry about in analog design now because this is self bias as we call by automatically itself.

Student: Sir.

Yes.

Student: (Refer Time: 12:29).

Actually this VSB is the only not only on the source side is also in the VDB side depletion layer is on the both side the; a value which I am really using in the average value is that correct the depletion values there on the both sides. So, VT on the drain side is not same as VT on the source side the general calculation is triangular average this is the game we play in area of a triangle in half this into this. So, same we concept we use we say average stage, but essentially equivalently saying it is increasing with self we appearing there; earlier, it was not there why it was not there because always substrate and gate were ground connected.

Once they are connected there is no of course, upper side is still will be there by at least there is 0 change in that. So, that average will go down. So, that change will not be. So, stronger now both changes can actually hurt you is that clear and this hurting you is VT will now enhance and what is the problem with VT enhancers.

Student: Current.

Current goes down and all that we are looking later, we says the trans conductance is essentially function of current larger the current larger in trans conductance. So, gain false if V; VT increases is that correct of course, one advantage you may say oh power goes down because the current has gone down.

But then, if we shall see later essentially gm goes down and bandwidth also will go down. So, essentially what will happen that all that analog was looking for probably may not be attainable just by not doing anything you may actually land in the situation which

is not meeting your spec reason that you did not take care of VT variations in analytical sense many a times we do not do this because it becomes you know non-linear equations keeps solving them difficult. So, we take some average value and substitute that as a constant and use it, but in spice you can only it, it can solve anything in given time and therefore, it will always be able to take care of point by point VT variation take averages of a whatever they wish to it. So, we do not have to worry too much ourselves now, but earlier this was a big issue for us we never cared that VT is varying too much the reason probably was also the gammas then was very small.

Now, with the increased dopings, the gammas are becoming stronger and that as pushed VT variations lower technologies more problems so.

Student: What do you mean by (Refer Time: 15:05).

It does not know because it is a P substrate n substrate. So, upper is it is always reverse biased.

Student: (Refer Time: 15:06).

P plus is yeah, I agree, but there the what potential that diode even if it conducts what you are saying is true is offset by this VGS value because now they are showing some bias value equivalently putting minus there that and you need a minus value to appear. So, it will compensate for that as if this bulk will go to higher potential and which essentially will offset the upper voltage VGS value for that equivalently saying 0 here, 1 here, 1 here, 0 minus there that is the way the voltage will look into we will come back to your issue is very interesting.

So, this is one issue which we are now taken in models.

Now, we have to take care this second issue of interest is very very very important; we say that saturation parameter lambda we said last time that it is lambda dash by L and we describes in lambda dash value which is under root up to n substrate or something equivalently this not actually numerically and numerically its, but it is not dimensionally correct. So, we may have to put constants which will give dimensions for that.

Now, this essentially we are trying to say once we declare lambda there then we say its constant it does not vary with VDS what we say we are taken care of variations through

lambda saturation, but we say that itself is constant is that point clear in nowadays derivation of this we say there is a lambda there is a slope on the id VDS, but that slope is constant that is our assumption that is if I change the VDS, then lambda does not change, but in reality that does not occur lambda does change with this now what you why it is called we will see this later.

There are 2 parts in lambdas in reality one because of that is what we call as channel length modulation which is lambdas from where actually this lambda dash by L appeared. In fact, and the second term is called lambda m which essentially is related to mobility we if we see our current expressions for the MOS transistor ids is proportional to nu deriving this all expressions we took nu out in the integral out I when I calculate ids VDS characteristics I removed nu I took it constant, but in reality nu varies with the electric field nu varies with many other, but at least for us immediate worries of the electric field.

And says nu varies with the electric field where applying now larger voltages larger fields because channel length is reducing and voltage is not scaling down. So, they are fields which are not small enough now long channel this issue was not very strong why channel length for 1 micron, 5 micron, 3 micron, even 0.8 microns fields were 3 volt; 3.3 volt. Now voltage is only 1.2 volt or a 1.5 volt and the channel length has gone to 65 nanometers; 500 nanometers. So, you can see how much fields are suddenly boosted up.

Now, these fields will be affecting because mobility is essentially the connected to how much drag it sees when it moves in the solid state or semiconductor essentially if the field is higher it will get retarding because it will accelerated it will likely it will impends next electron immediately and therefore, it will scatter faster and therefore, it will reach relatively late at the other end on an average this is called drag mobility reduces as the field increases now this issue also. Now, therefore, lambda m should also be a part of lambda and therefore, this new lambda must be now derived.

The first one; let us see the lambda c part if you see a expression of transistor or rather it is your figure of transistor.

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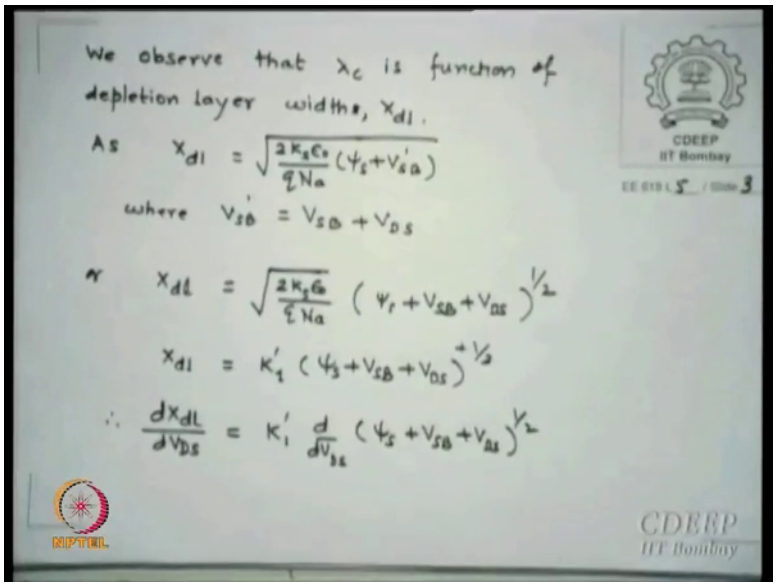

Just a minute; I was put it again that is side, but just you can see from here as I increase VDS which is larger than VGS minus right. Now let us say VSB is not there VSB is 0 even if it is there does not matter, but VGS minus VT is much smaller compared to VDS and if you keep in at this point when VGS minus VT is VDS, we say, it is forged or channel it does not exists at the corner drain as you increase VDS further the channel pinch of point shift towards source is that correct.

But in a transistor if you look at this transistor the actual channel length we say it from source to drain which is channel length L once the pinch of point moves away the effective channel length is not L now because channel is existing only L minus the depletion layer here is that correct total length is L, but the depletion layer rest is depletion layer is the actual effective channel length is reduced is that correct if this channel length is reduced. So, I must now take care that this channel length reduction must appear in my expression because actual L is not l, but it is a L effective which is L minus Xd is that correct and Xd is now function of VDS which means now even the channel length is the function of VDS is that clear L effective is L minus Xdl; Xdl is a function of VDS larger the VDS larger is Xd therefore, smaller is the L effective.

Which means if I see the expression W by L and now I replace it by L effective larger the VDS I create L effective goes down means current increases is that correct that slope which you say is visible to you is essentially as VDS increases L dash starts L effective

starts reducing; so, essentially current starts increasing from low value of VDS to higher value of VDS and that is why in our transistor characteristics we did observe on an output characteristics ids VDS for any VGS initially its linear then we expected theoretically something like this, but what we got is this.

Because as VDS increase the effective channel length reduced, but that also influences the lambda itself and that is the interesting part this is one effect which is obvious this is called channel length modulation why it is modulation because channel length get modulated by VDS change by VDS. So, as VDS increases Xd increases root of VDS, but it increases. So, L effective is L minus Xd and therefore, effectively effect channel length goes down as increase VDS and therefore, you keep seeing slopes. So, this slope. So, first thing is a saturated. So, it is no more really saturated.

Now, ideally what do you expect to happen we want something happen this side because that will give me what we will see I delta id ratio and we say it is a infinite value kind. So, that happens I say were fantastic for a current source if I want r 0 I want infinite. So, I would prefer saturation to a constant current, but now this is not a constant current how much it goes away is a very important issue for me is that clear and in this is what essentially related to lambda. So, we look into of course, I derived in a big way, but you need not you; you can also write down I normally solve all expressions.

So, we observe that lambda c is a function of depletion layer width Xdl which is twice ks epsilon qna psi s plus V now this VSB dash is nothing, but VSB plus VDS because if there is a VSB in depletion layer is further getting enhanced from the substrate bias side. So, the net substrate bias we can say is equivalently saying VSB plus V VDS if I substitute now in my Xdl expression I say psi s plus VSB plus VDS. So, larger value of this will appear and; obviously, larger the VDS or larger the VSB even if it is root Xdl will enhance Xdl will enhance I did some calculations further I just put this as a constant I then differentiated I want to see how depletion layer changes VDS from this expression.

So, I differentiated this expression I got k one this oh sorry yes right now it is d by DVDs. So, this will become minus half as the is that clear I am trying to figure out what is the variation of slope of Xd verses VDS because I have figured out that the current which is Xd increasing is essentially; we how do we actually put it into expression in our

ids VDI 1, it was lambda VDS we put some lambda parameter. Now I want to see this lambda which you thought is a is itself is the function of VDS then as you increase VDS the slope may change and a slope changes then you have more worries where do you bias your device is that point clear what I am saying.

Let us say for some reason I do not know whether let us say it is something like this; that means, biasing here or biasing here will have a different r 0s which means different gains is that correct. So, the worry is very very very relevant because I am my ultimate aim is what I want to get a at least the minimum gain specified and minimum bandwidth specified I must reach there if a put it affects me somewhere why of course, you can say you change the bias point yes, but in circuits once you design if you change bias point many other things will change. So, you may you keep somewhere over here then you see how much tolerant toleration you tolerable things you get if not then of course, you will have to modify your bias point itself this is all the issues are actually tackled.

So, I did this differential you can do yourself final expression.

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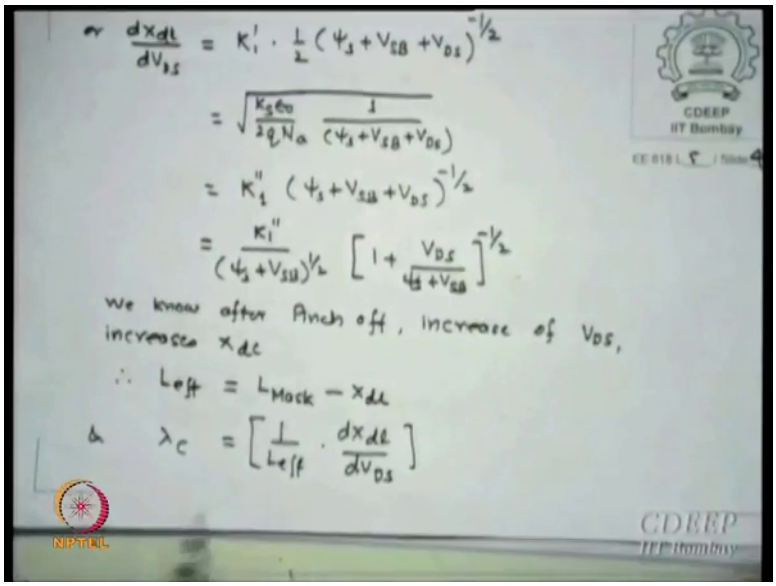

You can write this can give me a after differentiating it I Xdl verses VDS k one prime this other constants are took care it is psi s plus VSB to the power half one plus VDS upon psi s plus VSB to the power half we know after pinch off increase of VDS increase Xdl. So, the L effective L mask that is the actual channel length we keep minus the depletion layer and then we defined the channel length we entered lambda as one upon L

effective dX dl by dV Ds is that now clear say if this is a function of VDS lambda is a function of VDS is that point clear.

Since dXd by dX dl by dV Ds is positive is a is a value which is varying since this is a different VDS will have different this lambda will also vary with VDS I did this calculations further just moved down this L mask please remember when I design a chip I have to give some dimensions for transistor. So, source to the drain distance we call its channel length that is only mask which prints; however, in real life because the depletion the effective channel length is not same as what I thought as channel length ok.

Now, this is function of one upon L effective please remember this also is a function of VDS and there is a also function. So, there is some plus minus by some is increasing more some is decreasing and therefore, there will be at every VDS lambda c is not really a constant quantity which I assume lambda constant many circuits this works without just thinking you put it and you know god is on your side. So, it works, but many a times that days will come and then you find your circuit is not behaving. So, what do you the best person you keep quicking one method is [FL] at the end of the day what happens that it may take million years possibility to actually reach to the value or sometimes in a first hit.

So, there is a probability I mean event of event probability is not known please remember if I put a dice hundred times I have no real worries someday half you say fifty percent head and tail, but in a time frame there is no probability when this event will occur is not known this can happen now or maybe after any number of years. So, time event is very difficult to predict. So, when you say oh it has a very low probability agree it one in million, but that one in million may occur now, then what do you do. So, for a worst case designer we must know what can happen worst, then I say I will take care of this is that issue why designers look into all those issues because for them that worst case is what he is designing for heavers may not fall, but may fall may not means may fall and that may maybe today and that is where the worries are very strong in designs.

So, is that clear when I teach a course on analog circuit second year I keep telling nothing happens this is how it happens this is how you can derive, but when I start designing I realize that my circuit is not performing as I thought as my analysis give me I thought it should give me gain so much bandwidth. So, much it did not then I start going

back and say what went wrong I actually followed the professor he said this is how you should the analysis is like this, but it is not working; the working part probably is the deeper issues which we that time hardly tell because we thought that that the concept part we should tell.

But here is not just the concept here is something an issue which is real life things may not work at all, but as I say I am telling god is great most cases it works because you last year this is you will pick up what values you chose. So, if you had got it you will also get it this is how it works [FL]. So, that is how it works, but essentially it is a trick which may work. So, some what is what is the designers expertise you should have therefore, experience if you has (Refer Time: 30:35) chips anyone thing know very well what those wrong when ok.

So, he takes care of that that is why I keep saying analog designers have to be experience design because you must have seen many failures you know what goes wrong. So, then he had a thumb rule [FL] that is what exactly therefore, you take more of a art rather than science because that art is assuming you have enough science in you that is why you figured out this is how empirical it is working, but to get that empirical relations you must understand why this is occurring like this is what all that I am trying to hit.

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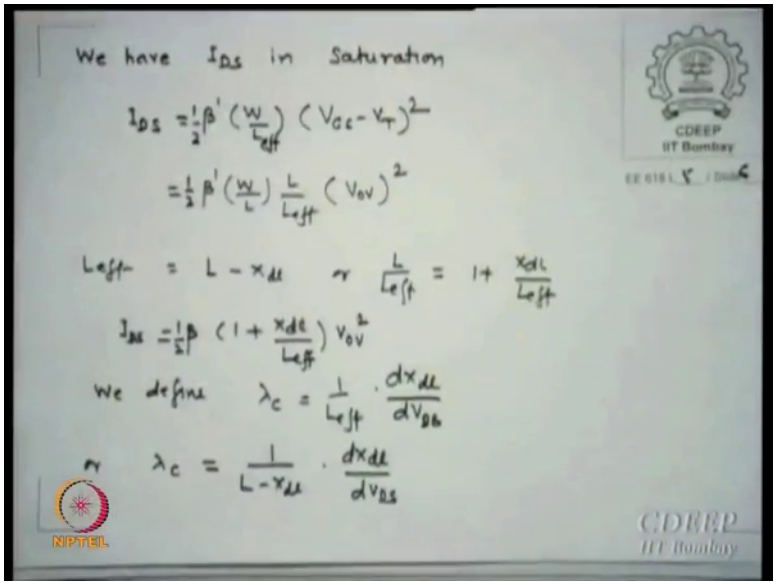

So, you look at the ids characteristics once again half beta dash WL effective this is what I said. So, L effective is L minus Xdl which is if I modify this I substitute and I see this

lambda c which is something like this is now a function of VDS through xds Xdl and also a function through dX dl by this, I do not want to expand all of it though if you wish I can show you the kind of expression which I derived seems to be very funny this is the expression just note down we all nothing great this is ids is some original expression I now can you think I did some mischief here also that lambda part is really taken care through this L effective part is that use I did not put one plus lambda way, but I am taking care through L effective that issue.

So, if I solve this, I just put x minus this as this form I get this expression and once you get this expression you do not have to write you write down my final expression I only took trying to write down all of it. So, lambda c is L minus Xdl upon this and I hope you have written down.

Student: (Refer Time: 32:33).

I have got both expression every expression I have derived Xdl I have derived dX dl by dv I have derived I just now substituted with this is that just substitute and if I substitute is that ok.

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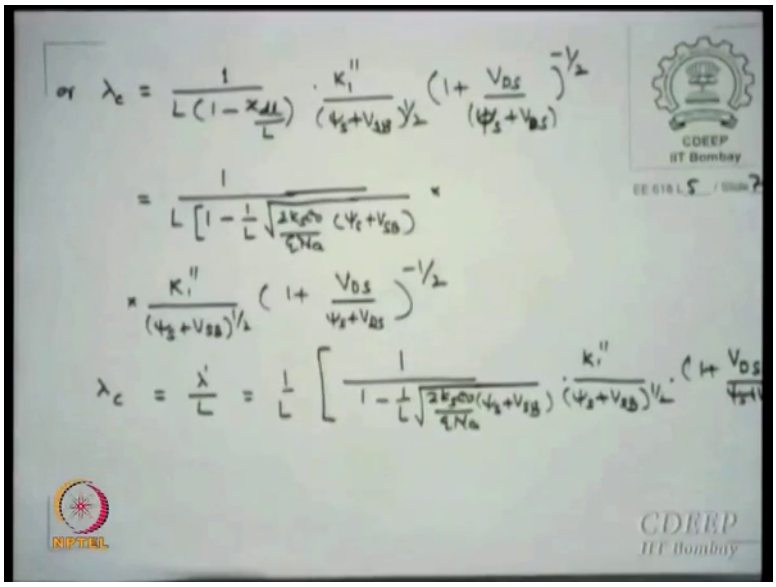

The lambda c, I will come back to it lambda c or in any lambda will this is not this anyway you are not going to solve by the spice this is only to show how spice will take care of many such issues lambda c we said lambda dash by L is that correct.

So, I actually converted into that lambda dash by L kind of expression by substituting this is L effective kind this is my dX dl by dV Ds just substituting and you expand this and this is the kind of expression you get it what is this expression this is that lambda dash time which I said lambda dash by L and thus lambda dash is a function of VSB function of VDS and therefore, lambda is not a constant quantity is that clear to you lambda is not a constant. So, you may note down, then I will show you the second part of lambda.

So, you can see from here lot much yeah expressions appear. So, now, this issues clear that one plus lambda VDS lambda is going to constant though as I say in all of our analytical designs we will assume some value and get away, but reality must be in your mind that in real circuit sometimes bias circuit is not performing partially maybe your r 0 is not getting what you are thought. So, what is the solution you use VSB at additional feature for you your VDS VSB you actually play with VSB then and adjust that value. So, that you get r 0 of your choice is that clear to you this is what I am saying design additional VSB is in your hand.

Now, earlier we never degrade; now we have a control I play with it you get what r 0, I was looking for this is the trick which I thought you should know why people actually go and bias it there now there are issues further do we need constantly bias we may not. So, there might be some feedback somewhere which says when I want and when I do not want. So, that removal of VSB also should be possible. So, that is more complications is that all of you this second issue in the lambda was related to lambda n.

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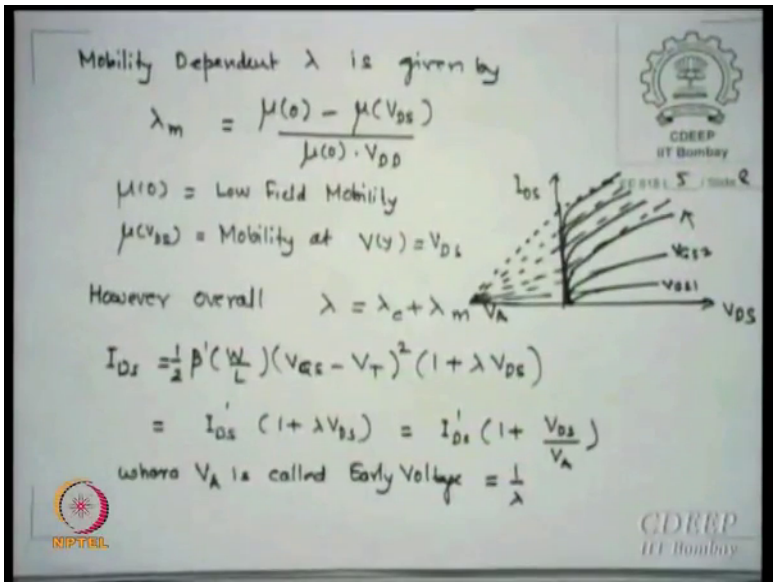

Which is I also mobility dependent we do not go into too detail because it is much more interesting from a device point of view how mobility varies why it varies you just take it from me that this is the expression which is mu 0 minus mu VDS upon mu 0 VDD; this is called the lambda parameter with mobility variations where mu 0 is the low field mobility and mu radius is the mobility at the applied bias.

So, if I now assume that lambda c is varying for a given bias point for a given VSB; I still assume lambda is lambda c plus lambda m is still constant which may not be true, but ok and if I use this expression this is the expression which I got earlier to show that is what the model I why I showed you now fully model because in real life model and in the an analytical model what is different we have shown this constant which was not there in beta dash we assume constant which was not.

So, when spice does it; it does not mean if you are giving some physics to it; it actually start solving and then your value of ids is not same as what you thought analytically is that, but why do you need analytically then because which value to start the simulation and. So, initial guess [FL] non-linear equation [FL] guess collect [FL]; so, there is no possibility of you reaching the solution because it is a linear divergence you have already cause effect 0 function.

So, in summation it is very essential for a non-linear system to know initial guess and guess very closely correct analytical solutions to give that guess actually at the end

something cad will work, but where it otherwise it will take some like for example, Intel Pentium four chip the latest version actually took in the first time they did six months of simulation on that so many transistors. So, many this hardcode problem was you know lot of good computer scientists were there to do parallel everything and it took six month to finally, get through because they wanted full test for that they did.

Now, they do not know now they know how much is important how much that much simulation is enough for furthers designs is that. So, some analytical thinking is an essential part in analog designs. So, if I use this expression as it is this is the expression without VDS and this is the expression with VDS and if I plot for different VGS ids characteristics at least the lower side of the ids VDS from the new side if I extrapolate them down to minus VDS axis this is for n channel device for P channel it is the opposite. So, actually there it will come third quadrant this is in the first quadrant this; this curve will be in the third quadrant and this pa will be positive there because that this will be the either is a please remember it is minus VGS minus ids for P channel plus ids plus VDS for n channel. So, just take it to the third quadrant and you will find that is for P channels.

So, if you see this expression now if you see this equation all of them somehow meet at a fixed value of pa is that correct the slope is one plus lambda VDS; VDS terms are taking this is. So, I figured out that if I take this as a VA; this is equivalent say your lambda must be one upon VA because then only it (Refer Time: 38:53), if you say assume lambda is constant and at this point yes ahead VDS it may not be. So, this is called early voltage this is called early voltage. So, many a times instead of specifying lambda they may specify you early voltage which is essentially is giving you a lambda indirectly or one upon VA is lambda.

So, many problems when I give you our intention in a otherwise I say early voltage is so much. So, that essentially is giving you the slope characteristic how do you calculate you can see if this is the current and let us say this voltage is very large compared to this let us say this is fifty volt this is a 0.5 volt or something. So, assume that is smaller. So, this is fifty volt divided by this much current is the resistance is that correct. So, what is r 0 this divided by the bias current which you put is roughly r 0 for it for you is that correct. So, that is the analytically this will be how much r 0, I am getting I can see directly from this expression itself or this curve itself.

I repeat VA is called early voltage the word has taken from base pnp; sorry is the bipolar transistor when the base gets punched the depletion layer from base collector junction goes to emitter junction short circuit equivalent occurs and at that time you say there is no transit time all carriers can go. So, that is the point at which we say points through has occurred.

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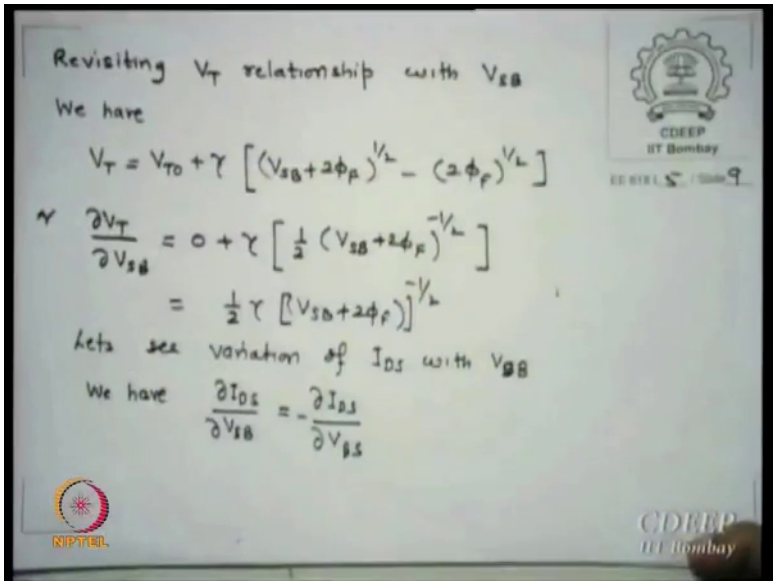

Let us revisit the VT expression once again we are also interested to know delta VT is this expression and we will like to see if VT varies how ids varies because if you say VGS minus VT and VT varies then I must know what ids varies with a substrate bias because if VSB changes VT ids will also change with VT VSB.

So, I want more relationship between ids and substrate bias because these are all issues analytically I may brush aside, but in real life they must be taken care in solutions is that the issues which I am raising are all first order issues there are many second order effects which I am not talking about there are many many issues right now, but at least the what dominant issues must be brought for the designer because this must be understood that why your specs sometimes do not meet reason we are not taking care of many of such smaller variations you thought smaller, but they are no more smaller.

So, I want to know relationship between this also in many books in many times I also this VSB and VBS is interchanged, but taking it is a only a minus sometimes you write bulk to source bulk bias sometimes you write source to bulb bias if it is. So, just change a

sign because source is grounded. So, the VSB should be minus, but I can issue this grounded and plus VSI can create equivalently. So, which way I will look at the bulk and which or which way I look at the bias is a only your choice I say VBS you may say VSB. So, the bias is same do whichever you look.

So, this sign has to be taken care whenever sometimes in some books you may see like VSB some other books they write VBS and then they do not show you sign the sign has been taken care through opposite polarity here. So, please take it because this; the 2 or 3 books which are suggested they all are not a gain with same nomenclatures. So, I thought in case some of you will read the book hopefully in that case if you have an issue, then you can get rid of ok.

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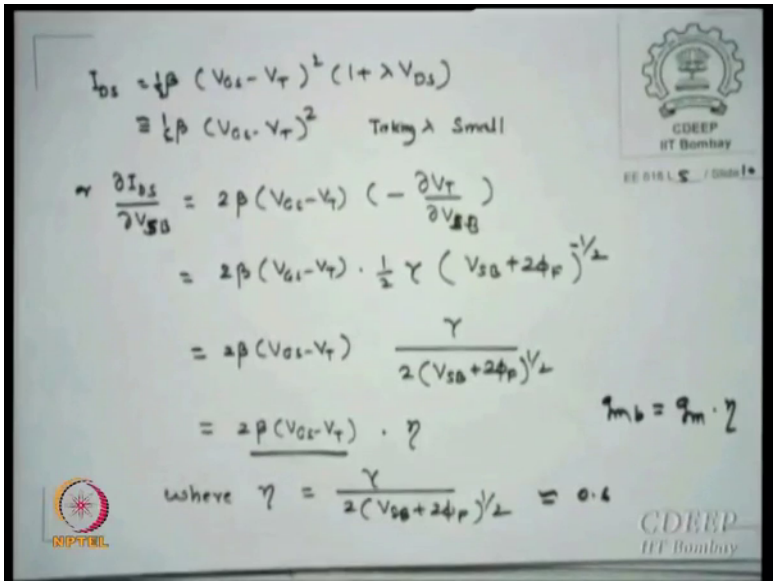

I did this please take it, this is very important and this is needed in a immediately for us why I brought this please take it this expression is going to be used in might actually equivalent circuit that is why I thought I should show you immediately.

So, I right ids is beta VGS one plus this. So, we got half part somewhere I think I missed there differentiate this and of course, then 2 also will go just check it I think there is a some quickly I did it this terms constantly check for this. So, I differentiate this I have already calculated this earlier delta VT by delta VSB which last expression I have shown you substitute here and I get maybe this too many integer beta times VGS minus just

check it by there were 2 edges the take from I just saw it few minutes say in one hour I ago some.

So, it is beta times VGS minus VT plus this constant gamma upon 2 VSB plus 2 phi F to the power half I think that 2 has been taken care by me some I have just shown taken, but just think of it this is a constant for a given VSB gamma is already only a function of Cox and it dopings, this is only a function of doping. So, eta is some constant you have and what beta represents what is the etas importance it takes care of what VT variation with substrate bias you are worried about no that is substrate bias indirectly also appears VT is going to be affected.

So, what we do is this of course, we can equivalent to saying that eta this is of course, we will see little sort of ga; this eta is gained by this expression and typically this is point six typically eta has a value of typically does not need actually you may have to solve for a given values, but around 0.6 is the value I will prove little later that this term is gm. So, this delta ids by delta VSD what name I can give you it is also gm, but with ball by substrate size of gmb trans-conductance with for the substrate bias is equal to gm times eta this is gm, but [FL].

So, we say not only there is one gm going on with you, but there is an additional gm is created if there is a substrate bias and which is not small 0.6 means if they are in parallel gm sources, then it is one point six gm equivalently I am going to get equivalent current source. So, you thought it is smaller where it is now higher that is why I say VSB is now my parameter of control I said look I can now start playing games on it is that clear that is why I showed you first time may be I am telling you that why VSB became so, relevant both in digital and in analog because now the technologies allow you to do many other things.

So, this gmb is another parameter of new designs which you must take care if you have a MOS amplifier.

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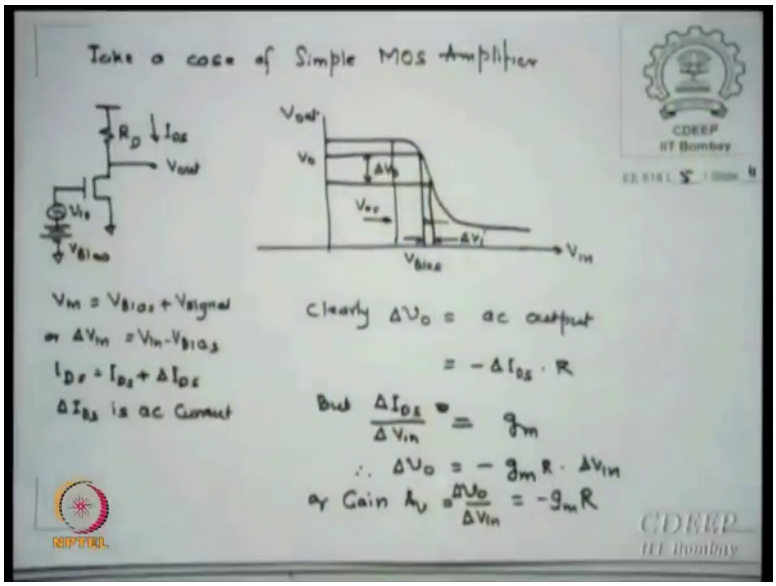

And right now this node is rd I start looking like that the input V in is V bias plus V signal. So, change in delta V in which is signal is V in minus V bias we always define small id capital Ds is equal to small ids which is the ac current of variant current time varying and this is dc this is how small signal values are expanded delta ids is the ac current. So, if I bias this is my MOS vi for an amplifier VA vi characteristics.

And let us say I bias at one V bias that is on the V in side I fixed the bias VGS whatever I fixed here and then correspondingly I know some V 0, I am go going to get because of the transfer; however, if you see delta ids by delta V in that is delta ids by ac this, it is a small ids a small VGS which is nothing, but the trans-conductance. So, now, I see delta V 0 change in if I there is a small change in bias to base there is a change in V 0 from here to here that delta V 0 is minus gm times r into this is the current I delta ids into r delta ids is the ac current r is the voltage drop across this.

So, this is the why minus is that is apart from here it is actually if you say total value VDS minus Id rd is this, but dc for ac valuation dc goes away from minus Ir is the output ac voltage this occurs because of what the transistor always gives you 180 degree out of phase currents out of phase to the input 180 minus can be thought as j square j is 90 degree j square means 180 degree. So, it actually gives you opposite polarity whatever is the input side and that is something one this is what the principle of inverter was in and

digital same way here is any difference you call now is it is out of phase 180 degree out of phase this is very very relevant in all analog designs how much phase you create ok.

So, gain function from this delta IDS by delta is gm. So, we are substitute here delta V 0 by delta VGS is minus gm R and this is essentially the gain of a amplifier sorry this is rd. So, please change with rd wherever I have done it; however, as I said to you in real life rd may not be the one which I am going to use. In fact, because the resistance just for the heck of it for those who think otherwise if you do not note it down then I will just show you why I never like to use actual resistors in silicon though I can create I will show you what I can create, but in some circuits even in analog you have forced to use resistances which are which block of the circuit normally we will use this anyone and heard of it the [FL] second year [FL] the band of reference when I create fixed vg bias that time there will be R requirement because you have I one temperature positive temperature coefficient something transistors give negative temperature coefficients.

So, I need compensations. So, I actually want positive temperature coefficient material R is. So, I actually going to there to compensates. So, think of it R is not completely out of picture, but in most circuits we will not like to use R for this region typically semiconductor bar if you use it and this is the current path I ground this I apply VDS or V. So, V is equal to. So, current I is entered. So, V by I is r, but if I if the shade I intentionally chosen R can be always written as rho L by a; this is my length this is my t and this is my W. So, this I rho is called resistivity of the material.

So, rho L W into t. So, that is called R is equal to rs L by W where rs is called sheet resistance or sheet resistivity either of them which is rho by t for a given technology generally this available because they are going to put separately whatever processes we have for making CMOS only those dopings will be available to you words substrate n plus P plus that was the only areas available this value is normally given by the word which is called sheet resistance or sheet resistivity is always technology dependent what process you are doing and the highest rs which I can get in a normal technology normal I can create which is ohm per square its defined as a ohm per square 2 hundred ohm per square that is best I can get of course, other materials can give mega ohms and mega ohm per square.

But silicon process technology for CMOS will not allow you a region which is better than 2 hundred ohm per square if I want a 40 k resister R from this expression how much will be L by W the highest I have 2 hundred ohm per square how much it is 2 hundred this L by W is call aspect ratio is that correct aspect ratio L is 200 times the width length is. So, much and width is so much any join person will tell you that if the aspect ratio that the accuracy in making that it is like goes away now I cannot hold on that one micron line or 2 hundred micron is more difficult by drawing outside that even if I print otherwise that probably means if let us say W is half a micron or a given technology half micron technology this is hundred microns.

So, in a transistor may require a 0.5 by 0.5 micron area and your resister is requiring 200 into 0.5 area or 8 resister [FL]. So, transistor [FL] resister [FL] chip size [FL]. So, [FL] one cannot use resistors because it will just take away our area of course, you can build this if you can increase this Ro Rs 2000, 2000, 5000 poly resistors people use sometimes in dram srams, then there is a special technology additional many if you messed yes R can be reduced and will link to its ratio.

So, in most technologies what we will do is we will use transistor itself as the resister you can see from here after id VDS means current voltage slope of delta V by delta I is a resistor. So, there is a small register here there is a large resistor here. So, you keep your transistor is either in this region or in this region. So, we either get this resister or we get this resister you change this to in the W bias because ids is in your hand W bias. So, change the size and you get different Rs; is that correct. So, in a analog circuit proof (Refer Time: 55:13) transistors will be used as resistors we will never be used as I mean there is no additional such huge of course, one to say some area what do you do anyone no.

So, how do I do it spiral it or member it something like this. So, [FL] perimeter adjust [FL], but area [FL]. So, you can adjust bit of perimeters. So, is that issue why R s or never. So, in all though in circuit classes second year earlier [FL] which you say in R are there because its it does not matter how do I create, but I just want to put the numbers there, but in ICS the first thing we will do is we will get rid of this actual resister [FL] now the problem with this most cases when I put some transistors there I must guarantee that that R does not change ok.

And if that changes in (Refer Time: 56:11) and that is where the design start that that R is not really the constant I thought if varies is then how much varies. So, can I take care of my design so much we have, ok, this is the issues which designers look for no.

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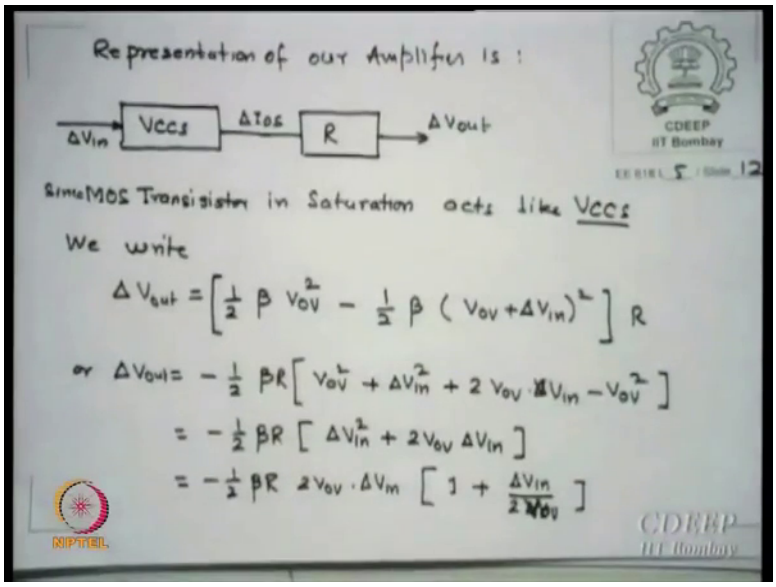

I have to use same expression again think for times to show you some other way of looking the same thing I have that same VCCS ids kind of amplifies shown I rewrite the expression delta V out which is ac. In fact, half beta VOV square right, now I am leaving alpha minus half alpha lambda half beta VOV plus delta V in VGS minus VT minus a plus V small this square call yeah this here I have used R.

So, I expand I expand squares do you know your terms if they are there VOV square and this will go away and I get delta VOV square plus 2 VOV delta V this VOV-VOV cancels. So, I get minus R beta 2 VOV delta V in into one plus just adjust the terms there is nothing big going on and I just take out some terms leave some terms inside just take VOV V in out. So, I get 1 plus I am taking this whole expression out. So, 1 plus delta V in upon 2 VOV.

Now, this expression can be further modified have you written down please note down I repeat what did I do ac is nothing, but total minus this is with signal this is without ac signal this subtraction is only did with a ac signal I am now going to their another gm expression which is very relevant and that is what designers should look at that is why I brought this expressions for you expand this VOV square delta V in square plus 2 VOV

minus I put signs. So, this minus VOV cancels square cancels. So, this I take this term out. So, I get this is that ok is that everyone minus half beta R 2 VOV delta V in 1 plus delta V in by 2 VOV same expression.

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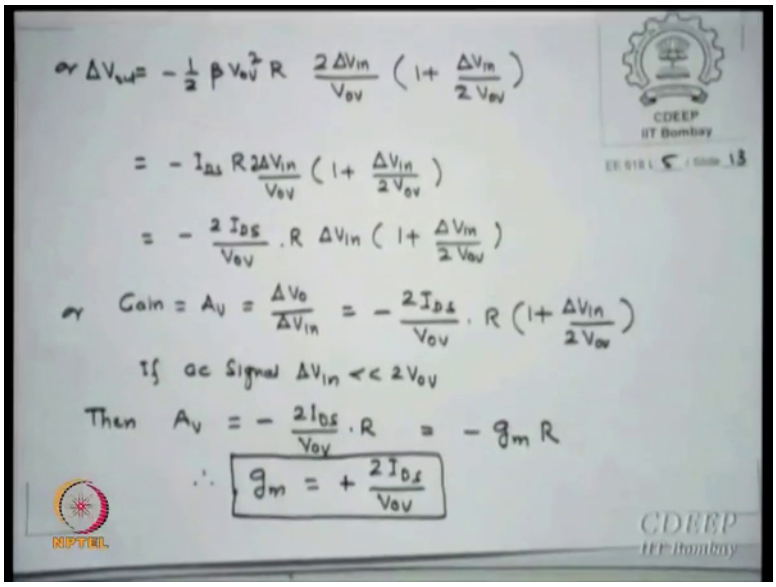

Just adjust it; what is this half VOV square half beta VOV square is what do you seen only of ids without signal that is what VOV square we started with.

So, this is ids delta V in R by VOV plus delta V in by 2 VOV this becomes 2 ids by VOV is that clear 2 ids by VOV the reminder term is R delta V into this is that only reorganizing the terms nothing great I am doing I am just reorganizing because and then I am looking for the delta ids I mean ids is that VOV term at the end. So, I get 2 ids by VOV as R, yes, delta V in is delta V in 1 plus delta V in by 2 VOV, now what is the gain I defined ac voltage by ac current or change in output voltage by change in input voltage which from this expression becomes minus 2 ids by VOV times R into one delta V in by 2 VOV is that clear.

If you say it is the small signal ac signal delta V in is much smaller than VOV because what is VOV capital VGS minus VT VGS is the bias value volts; what will be signals millivolts. So, you can see there as long as that is the condition I am putting what is small signal V in must be very small compared to VOV is that correct then it is small signal in that case this term can be neglected. So, I get minus 2 ids by VOV into r, but I know av I just derived at minus gm times R which means the gm is 2 ids by VOV is that

correct this is an expression which I will use this is one way of looking at the design using I this is my parameter I want to adjust gm I will adjust gm through 2 ids by VOV ratio is that correct I am going to adjust my gm through ratio neither ids nor VOV I can do either and do this.

But what I am now giving you I take the ratio. So, now, I have a larger game to play I changed sufficiently both someway. So, that I get a ratio and to adjust to this I have adjust W bias. So, that this ratio is different by individual is different, but ratio is what I am looking for this is called ids by VOV designs this is different from VOV designs or we do not be used to always design using VGS minus VT now I am introducing a new way say let us look design based on ratios of ids to VOV just do not look for VOV alone I show you there are 3 possibilities which can one of them is based and this is much more powerful tool in actual designs.

We can always design bias dependent here is a ratio of. So, gm dependence is what because gm why I look into this kind of game because at the end of the day what is my important parameter for gain gm. So, I say you want these gains. So, you want this gm. So, let us go back and look; what can I do for this. So, I am now looking more from the analog side gm control [FL]. So, what should I control as long as I adjust the ratio I need because then the issues started power will come everything else will come.

So, I will see to it that all this adjust to this I do not say this should be telling something I may say 100 and something I may say 5 and something I have a ratio to adjust is that clear as long as that ratio I adjust I get my gm. So, this is essentially I want some very new method, but this is little better techniques of designing a chip rather than the normal VGS VT minus method which we will show you that is also possible initially we may solve using those methods, but then I say now convert on this you have a variety of solutions.

Now, before I go to the next gain function I have not yet talked about that word again, but let me be very clear on that.

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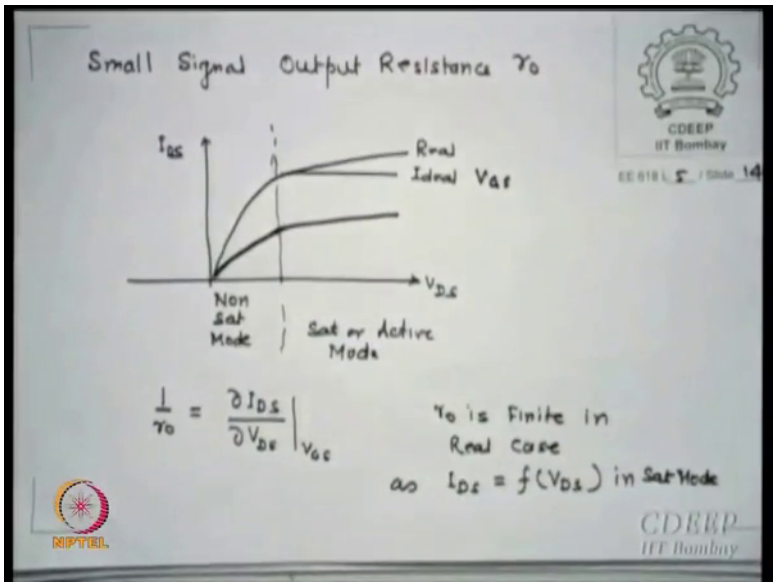

If you see yeah ids VDS characteristics in saturation this is my ideal this is my real the slope as I said may not be constant so, but for a one VDS I may say it is one value now I may find r 0 as delta ids by delta VDS slope of this characteristics r 0 is finite in real case because there is a slope and ids is a function of VDS inside that is what one plus lambda VDS term we derived ok.

So, if I do this there are few things which you should remember and that is why I am showing over this; this is a simple characteristics for r 0, please remember, we will never go in this region which is the linear region y; y will never operate our amplifier here.

Student: there is no (Refer Time: 64:22).

There is no game there, there is no gms there actually. So, do not we will always operate in saturation region and please remember there the actual value of input availability is very very small because it sharply falls V 0 V in. So, the gain is only available in a very small V in rangers ok is that expression clear r 0 is nothing, but one upon r 0 is delta ids at any VGS this is one VGS value some different VGS this will be different because if you have a characteristics somewhere here this node may not be parallel exactly and therefore, they may have different r 0s is that.

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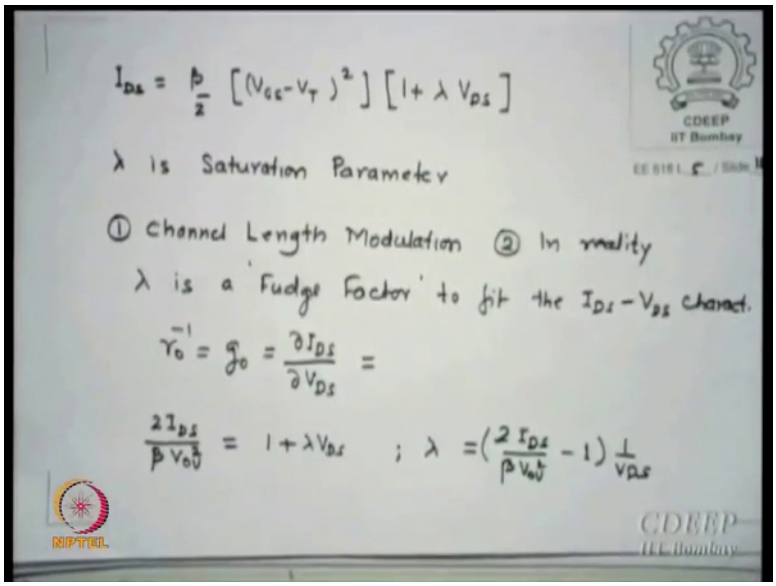

So, if I write this expression IDS again as I wrote earlier beta by 2 VGS minus VT one plus lambda VDS lambda we all now know what it is. So, you must take from V now. So, called channel length and mobility modulation we do in reality lambda is a fudge factor what is fudge factor means it is a fitting function which fits to the curve expression of r why they want a expression I know it may vary. So, I figured it out off how may how it will vary in real life what will be there for having found ids VDS characteristic for different VGS that bias points I am actually fit a curve there and get a r 0 there and that is the end of it.

Whether fits into my physics or not irrespective, but that value is available to me, I will use that therefore, it is some kind of a fit function which I am going to use in their life. So, please remember the theory etcetera is fantastic to understand, but in real life we always use this as a fudge factor fit now if we know. So, one can see lambda is some way related from this expression to 2 ids beta vo q upon VDS and if I differentiate delta ids by delta VDS please remember this is the expression which I am going to use where lambda is given by this I just come back and show you the same expression which are derived earlier have you written down r 0 is just there is nothing to write only thing is statement I am making is the it is a fit function rather than the real physics behind in real life.

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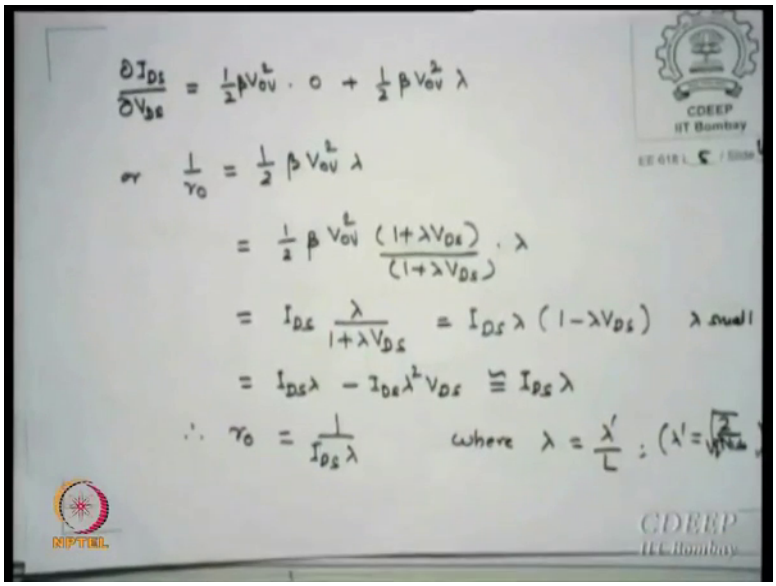

If I differentiate this r 0 is coming something like this and if I fit correctly I get expression ids lambda one minus lambda VDS if I expand if it is roughly equal to and if lambda is smaller lambda square is even smaller. So, it is ids lambda. So, in all expression what do I do is r 0 is one upon ids lambda. So, if I am specified lambda or VA I have knowledge of my r 0 is that correct how do I get r 0 either I will be specified lambda value or I will specify early voltage which is being the same and then if I know my bias current ids then I know my r 0.

This is with all these conditions. So, in accuracy is partly built up, but this is the first trial for this system. So, that is good enough value for your evaluations. So, I always started analytically saying that r 0s ids upon lambda they I say I have shown you so much physics how much it varies and why it will varies yes ours modeling in spice should take care, but analytically this is a good enough expression for us is that difference clear to you why I show you both side because you should not say that this is always correct it is not correct, but this is good enough for analytical solutions. So, first guess how much value gains will be.

Let us say if you designed with all this in accuracies your gain gets 9900 in real life it may gain 8500 time, but you say it should be more than 8000. So, it does not matter whether I reach 9000 or 8500. So, how much inaccuracy I can build and is still tolerable for me is all that designers should know if that happens he say thank you. So, this is the

game is that class clear that it is not the value which matters; it is the value bound matters and as long as we remain in the bound your design missed it work.

Sometimes it may call over design sometime may be under underachievement its, but its works.

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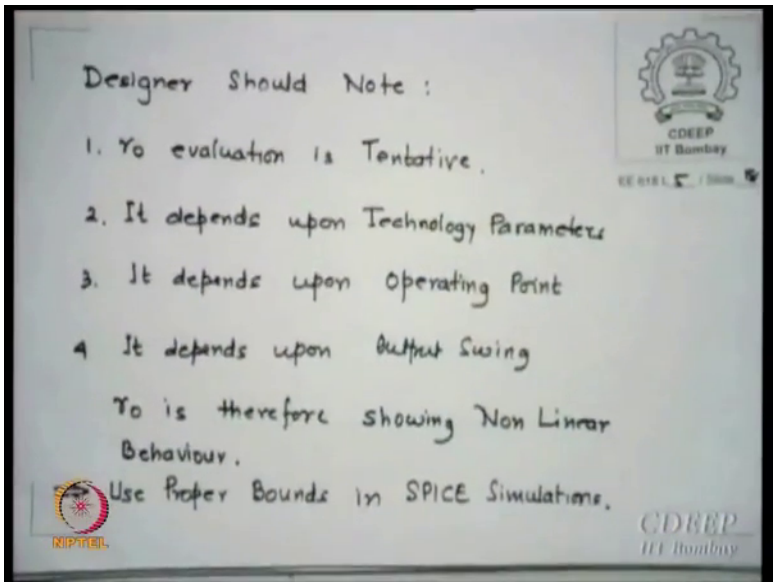

So, for a designer should note the following this is my as a designer help you write down as a designer you must move this for a r 0; r 0 evaluation is tentative it depends on technology parameters it depends on the operating point it depends on output source because whether that VDS is other or this side is and how much is signal r 0, therefore, showing non-linear behaviors I gave some hints on that I will show you what I mean by this swings use proper bounds in spice is that clear. So, that is the marker.

So, what is you should do use proper bounds there is nothing called correctness I will just show you this part non-linear how it works just let me finish few minutes that is the last of it although just.

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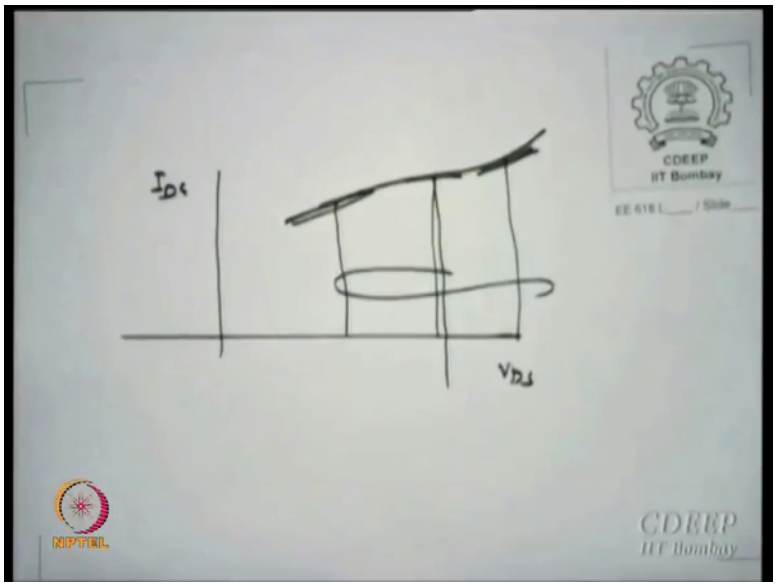

Now, said r 0 may actually maybe I should draw a fresh figure a different VDS something like this, this is my IDS VDS. So, depends on if you are biasing here biasing here or biasing here slopes here slopes here slopes here are not same is that correct.

Even if you bias here and if your swing is something like this large swings even when you are hitting different r 0s. So, there is a non-linearity built in your r 0 itself and in their life therefore, it should be taken care that which value you are using which is sufficiently ok sufficiently. So, please take care r 0 is not clearly a I just a lambda is not a constant. So, his r 0 is not a constant quantity. So, where do you bias how much swings you give that may decide the variation in r 0 and therefore, the gains will vary every other bandwidth will vary correspondingly see you tomorrow that is Wednesday next.