Analog Circuits
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Lecture – 12
Frequency Response of Amplifier

Okay, we were looking last time about the frequency respond and we are gone through a typical circuit of must amplifier and we are found out that if I use full analysis of Kirchhoff's law that is node analysis then I can find both poles and 0 same time but many of times as I said 0 is normally far away from the gain-bandwidth product that is unit again bandwidth.

So it may not be very important and therefore that may say we may only poles and if these are the only ways one among them may be our layer than the other and the one which appears earlier that is at lower frequency is called the bonded point or essentially the point which is the dominant Pole, okay.

That is what we discussed last time, well of course there are many amplifiers you can go into the book and you can look into the book, common source, common drain, common gate, common emitter and all sorts of amplifiers please look into them we are given a theory how to solve. Any such circuit can always be solved using the standard procedures. I will just give another method which is a very popular method in engineers which is we discussed in some way earlier but little more detailed circuit.

I may show you today it is called 0 value time constant analysis to find dominant pole. So we can actually find out dominant pole with no great difficulty. We can just do some analysis and we say okay here is the bandwidth, because we are not interested in gain bandwidth unit again midpoint but we are more interested the bandwidth.

Where the gain starts falling ok and that point is the dominant pole so our assumption is the other pole is at least away maybe one order by frequency or even 2 orders if it is 2 orders it is 40 DB below so a that gain has no value when if within ten times it is even 20 DB down which is large enough in fact.

So essentially what we are saying that we will be very keen to know which is the dominant pole and our assumption to start with is that the dominant pole exists, okay. In reality if you do not want to agree with this then you do full analysis and you will get all poles and 0s.

Wherever you wish you can find out which of the dominant which is the most correct and what absolutely proper method but as I keep saying not every proper method has to be used every time because there is sometimes short of time of doing analysis that is the quickness to give results products have to be released and on basis of experience people know this will have a dominant okay.

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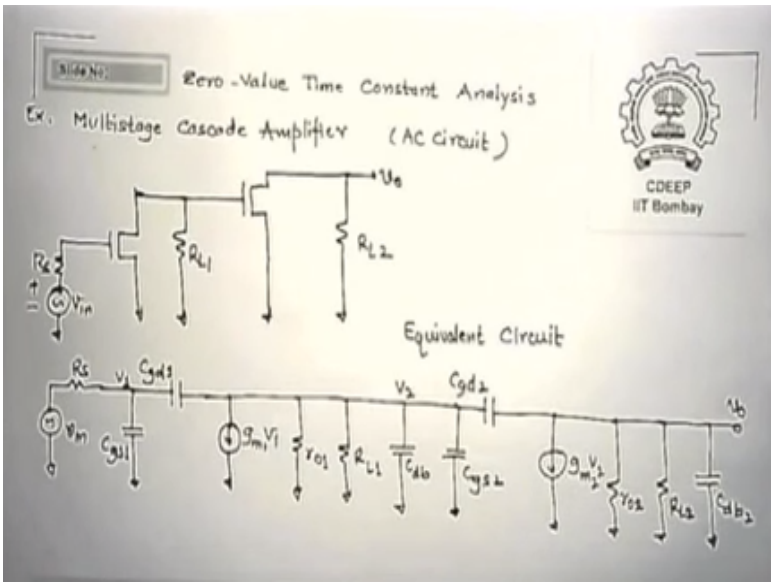

So I am not saying this method is always valid depends on the values of GMR's and everything given it may not be the dominant which we think but assuring there is. I have taken an example which is intentionally multistage amplifier that it is, it is a cascade at 2 stages of a MOSS amplifier. There is a first stage and there you are now the stage what are not shown here essentially is the DC biasing part in this okay.

That may exist, RG may exist and supply has to be RG1, RG2 kind. Right now in the AC equivalent circuits have been AC circuit has been shown. We also want to neglect CC1, CC2 and

CS bypass RE I pass are a circuit so there is why we are neglecting that because right now we are shown that they are not the part of the external circuit.

This is a simple analysis to show how to get it in real life they may be CC1 here there may be CC2 here everywhere things will appear as they should. So if I have this circuit look at it the first circuit can be represented by equivalently on this, then series resistance may be I call it signal.

If you wish I do not know where what I call it but R signal then whether they are CGS1 CGD1 then this current source at the output GMB1 B1 is the voltage here which is VGs actually, champing that is order 1 and R1 which is the load provided to you then there is a drain to bulk voltage CDB and this is this point so this is my V2 somewhere here.

We will be my V1 so V2 is now going to be the input of the next stage. Okay, so this is my input there is a CGS2 which is for the gate to source capacitance of the second stage Cgd2 which is the gate to drain would say capacitance between this V2 and the output then there is a equivalent current source which is gm2V2 sorry yeah gm2V2 and shunted by RO2 RL2 and CDB2.

This is 1equivalent this is the other equivalent. This is 1, this is the other, 2 stage. What is the advantage of 2 stage amplifier per se. Why should we use 2 stages let us say, I want to gain of 100 so one possibility is that I will make gain of 100 and one single amplifier the other possibility is I may do 1010 or 25 kind of thing maybe 520 or 25 also the decision.

I will leave it to you to find out if you cannot next time I will tell you if you have a cascaded stages there is a method in which first stage gain should be higher or lower than the second stage it should not be equal that is definite. Whether the first stage should have a higher gain than the next stage or vice versa on what basis we decide that. One up to 100, okay.

I can make 10 10, 5 10, 5 20, 25, 30, 35 kind of thing many combinations I can try 4 25, 25 4 so how do I make a choice that the first stage should have a higher gain compared to second or first stage should have much lower gain compared to the second stage this is something which you

must find I do not think every book would are given but I think Sandra Smith has discussed it somewhere find it out if not I will tell you.

Why we choose one over the other. So is this equivalent circuit clear this is the first stage equivalent circuit, this much and this is the second stage equivalent circuit which is given for this. What is then missed here CC1, CS and CC2 and we shall separately handle down because we figured out those capacitance values are very high and therefore they will actually act like a short circuit at high frequencies, okay.

Because I am looking for a dominant Pole ahead so we are expecting that these will be short circuited at most those frequencies, however at low frequencies they may dominate and we will look into them, well, what they do when they are present, okay. So this is that clear what I am trying to do is to solve a 2 stage amplifier mass amplifier and my assumption.

I repeat CC1 CC2 CS everything is much smaller and therefore neglected at high frequency and also RS is bypassed at that frequency because CS will be short circuited so the bias resistance in the source also will get bypassed at high frequency so know where that RS is taken care though in real DC there will be a RS sitting there is that clear shunted by CS but at the high frequency others will get shorted, okay.

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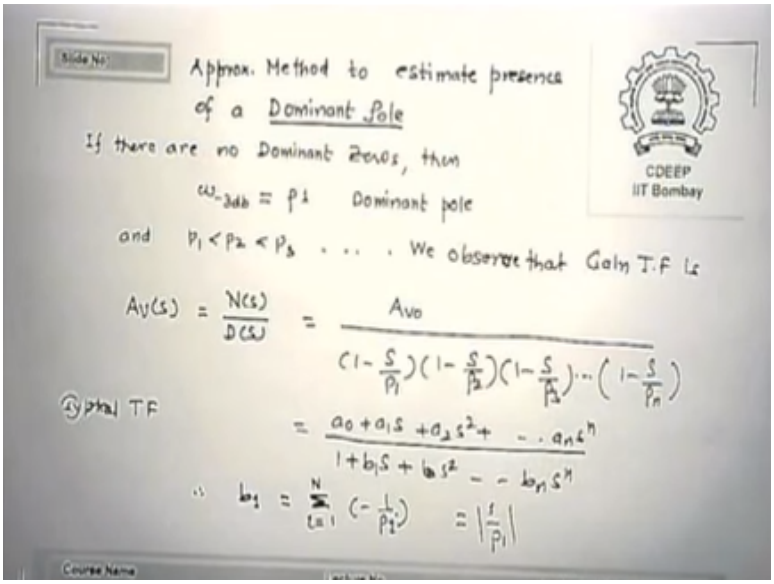

Having said so I as I said this is an approximate method to estimate presence of a dominant pole and please do not believe that every time this is true but in most cases 99% is symmetry so he may try once a while, may fail once a while. About redemption again is there are no dominant 0 okay, that means 0 does not exist prior to the dominant pole if that occurs the gain will start rising somewhere so our assumption right now is 0 is far away.

So we say, a dominant pole which is at the 3 DB point where the gain falls by 3DB is our dominant pole p1 and again we assume that for the transfer function of the gain p1 should be less than p2 less than P3 if there are n poles. What we are saying is dominant pole is p1 next maybe p2 p3 and so on and so forth, okay. Any transfer function of gain can be represented as numerator divided by denominator NS/DS and typically.

This actually it should come here a 0+A1S+A2S2 … AnSn upon 1+B1S+B2S square BNSN this is, first look at this, then I explain this. If there are no 0s in this as we discussed, which are dominant the numerator part. I just miss it, I say they are none coming from the numerator. What numerator will give me 0 and I say 0s are far away.

So I am not concerned about only a 0 term will remain but that is a DC value or that is a fixed value so that will go into the gain DC gain part itself, okay. Is that correct this other terms I am neglecting a1s a2s2 is why I neglect because my assumption is 0s are far away, okay. Part of it and the poles of my query ok is that ok this is my assumption ok and if they are assumption the numerator is only a 0 for example.

So equivalently say in a normal gain voltage gain function it can be written as some DC gain divided by 1 mile which includes some p1p2 value also in the product because then you take it out that P1 P2 will also come outside. Is that where this S-P1 is actually appearing so P1 is outside but right now I kept like this, so anything constant is taken care in AV0 so 1-S/P1 1-S/2/2 so on and so forth.

So our assumption is if there is a dominant pole which strands are also negligible in the denominator SS square SQ will be negligible. We said S is first one will come from S and we

said that is the dominant pole so we say the next terms are so far expanded so in the first 2 terms it will be 1+S times SS square a1S+b1 SS square.

So we say ok S square terms does not exist only the first term B1S is only dominating term is that clear. If I take into this bullet let us say all others are much higher even with this 1-something 1SS squared terms ok so which means essentially what I am going to get is something like this 1 upon P1+P2 if I make product of this but this essentially I already said P1 is smaller than P2.

So even I say I can neglect this. I only say that the coefficient is essentially related to S/B1 only is that, that is what I say the coefficient B1 here is nothing but sum of all such PS if you take more than that and since I's are only one here, so it is 1 upon dominant pole is 1 upon P1 so how do we get this, by only observation of this transfer function I realize that this terms can be neglected except 0 here also.

Other terms can be neglected so only term which will give me dominant code will be related to B1 therefore that is how we can evaluate. This is the trick I am going to use now how do I get this P value? This is my next question, first is we figured out that all that I have to calculate to get P1, I must somehow that P1 is related to what in normal case we are discussed B1 it is nothing but related to other than time constants.

So there are more than 1 capacitors which are coming into picture, we must calculate both occurring due to all such capacitances and the notes associated with them, and then sum all of them one by like this ok and if I get that 1 upon tau average which we are going to do I will get my poles here.

Example for that, before we go, this this is something which we will discuss in feedback once again but just to give you the S function which you keep drawing everywhere it essentially has 2 parts it is a complex function Sigma which is the real part and J Omega is the canary part a plane which replace them as Sigma J Omega is called explain any function complex function can be represented on Sigma J on I think this is max you must have done by now N times.

This is just to show you I hope the poles are real ok well then there are then they must lie on the left top plane Sigma must be 0 for them but the imaginary sorry JJ Omega must be met but only real values if there are only real poles available then all should on the left top plane and which is the dominant one which will occur earliest.

So P1, P2, P3 PN poles will be shown here is that clear so let us say well 0 can occur 0 can occur here maybe we will say you know and in that case it is on the right half plane and then system may become unstable as we shall see here.

So we will prefer 0 to occur somewhere here on the imaginary axis or even if possible it is on the left table and even safer oh it actually sits on the P1 is that correct I can do that I can actually adjust the value of this 0 or either here or here or anywhere so that the system becomes more stable and we will see this little bit a little more detail when we come to stability any 0 or poles on the right half plane actually leads to instability.

What does that mean that the gain starts increasing and not decreasing is that correct and if increasing means it keeps increasing infinite main system will go to VDD power supply maximum voltage so it will start saturating on so it will not remain amplifiers so we say it is become unstable is that clear so we want to see the system remains amplifier.

So what does the trick on keep keep on telling you all the time that please remember amplifier is the only system in the analog circuit which is of relevance everything else is drivable from this ok all that we keep saying is if I know my amplifier design I know almost everything because all are only derived part out of it because the trailer which I will use for amplifier design is as much required for oscillator designs or a to D converter anything.

Which I do later and this is good enough for me if I know my amplifier theory properly that is why I am spending so much of it time on this otherwise I would have actually said ok beat this you are done in wealth or maybe in first year, I want to make it very clear that why we are spending so much time on amplifiers well once we understand.

How do we get amplifier designs then we know roughly everything in analog ok so if I take an amplitude of a base it will be a dominant pole for this would be a B0 1 0 and 1 applaud this color as long as Omega is less than P 1 till that time gain is constant beyond we do not know whether dominant poles where they occur.

So what I am saying if I have dominant this is my pole P1 up to this at least ok I know gain is constant from here onwards and then I do not know access other poles may further start following it down minus 20 minus 20 further and further ok, but I am interested in where it falls first ok, which is called the bandwidth why it is called the bandwidth the term bandwidth was given up to which gain is constant ok.

So that value is of our interest ok, can we tailor p1 as well yes I can as I said other day if I put a 0 here per se what will happen to there till the next for occurs which then will become dominant the gain may become but something else I have given by that just yet just we see what happens in feedback we use the theory, I never find that but I something else increase bandwidth definitely ok is that clear.

So something I must be losing in getting higher bandwidth, so we will see what exactly we lost is that ok we see that little letter so is that issue clear so this plane has been shown to you that I must get my real plane real poles on the left tab that is valid they must occur so that the system is stable otherwise will be a growing system and we do not want system to grow outputs in the inadvertently.

So this part as I said this figure is just shown here will come back this figure again ok, so the method which I suggest which is called 0 value what I suggest is given in many other books I didn't see very much in the this book say does mean book and therefore I thought I will lie down for you in JIRA all the time and I say what we see every capacitor see some equivalent register seeds.

Now that the word CS is a very important and then we say and if that resistance equivalent resistance are you key the time constant associated if that capacitor it is RS time see is that correct so if you are as many capacitors you have find our equivalent as seen by each of them now the analysis which we did is something interesting here our assumption here is superposition theorem is valid what does that mean that is the influence of each capacitor is independent which may not be in reality many times is that correct the capacitance.

Which CGD may influence both all sides in fact but our assumption is each capacitor is independently controlling outputs to input resource and therefore if we can take independent influences of all capacitor and we add all of them as their time constants then we say ever values ok.

This is our assumption superposition theorem is what we are going to apply what is the ban-ban superposition theorem is true when the system is linear, then only superposition is possible and I repeat I did tell you once if not we check again y is equal to MX+C is a straight line ok so looks to be linear this looks like a linear but it is not a linear system is that correct y is equal to MX+C is not a linear system but which are linear where Y= MX is linear but Y+ MX+C is not aliases.

So, do not think that if a straight line our is a linear system ok what does suppose you say if exchange 2 plus y should also become 2i, ok only, then superposition it is valid in this case so this is since we are making an assumption N+1 so there are M capacitors we say is are equal and 1C1 taught me are equal and C2 tau n is this and then we say the net tau is just sum of all such rows then the dominant pole will be 1 upon tau average this is what we are going to say ok.

Now let us see in our circuit which we just now put these are this how many capacitors you are seeing one is CGS one otherwise Cgd1 CDB Cgs2CG and see David, there are 6 capacitances which are of relevance 1, 2, 3, 4, ok, so we like to see each capacitor sees how much equivalent resistor is that correct and if I get that equal and register I get RC time constant for each of these capacitance and then I sum all those time constant of 1 upon tau is the dominant pole.

Now I am saying this my method thus first day when I saw something a MOS amplifier and I give you a dominant pole expressions please verify whether the expression I get from here is same as what I got there ok and you will find to your great surprise it is almost same if not exactly same almost say ok.

So let us see that almost same part is how almost so the first capacitance of interest is CG d1 which one I tap CJD one I am talking of this this circuit CJD one ok is that ok this is v2 this is this so whenever I will do this analysis the first thing I will do is chart all independent sources open the current source and shot voltage source ok.

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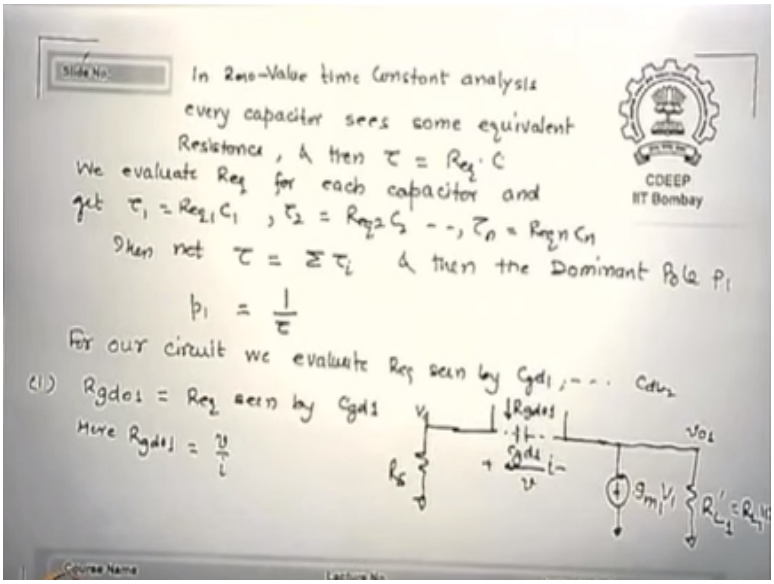

Short all voltage sources in kelvin and please remember the word independent short all independent voltage sources are open all independent current sources if I would ask ok then at the V1 I get only Rs, please look at that circuit since Vin 0 so only RS remains this is the voltage V1 then there is a Cgd1 and capacitance here at the output gmV1+RL and now we are shown that the next stage is right now removed as if equivalent T that is equal and input for that is shorted removed from this ok.

So, let me say the output is V Rho 1 which is RL1-is RL1+or if you add as how you can say already is our l1 that is fair enough now the condition which I am going to say replace this

capacitor by a current source I replace this capacitor by a current source I is that correct and we say the drop across the capacitor is plus minus V is that clear.

We across the capacitor the voltage is V +/- is that ok, then we say the resistance seen by the capacitor is V by I is that clear method I repeat replace the capacitors by voltage we calling this call as V+ v +A current source of I connecting that is that correct so what is new is that every capacitor I will replace it by current source beep and drop that across his V is that clear.

This is what the 0 time constant analysis is what we are going to do all shudder then I replace the capacitors by equivalent current source I, which gives your drop loss V then the V by I is nothing but the resistance seen by the capacitance ok now I better show yes why we remove Oh we say now that is unloaded circus ok.

Because you are doing superposition we only take care of each individual efforts the IR capacitance I short out ok so the other nodes as if are not no input is going to the output side equivalent Leasing ok that is what we did there is a I mention is superposition theorem is valid in broad cases.

While we can sum off each component time constants have nothing to do with time constant per see any function can be such a added and ever which can be taken this is the theory mass theory we just have applied it to our case to get equivalent values of that ok it is a functional system I am just applying it to a circuit system ok is that ok.

Now if I do this you see keep seeing a circuit that is the drag across RSV1 what is the drug that was RSV1 so all times RS is V1 ok if you look at please look at this circuit, I do not know whether you can get ok so the drag across address is V1/RS is the drop which is V1 but if you see the other side this is all minus gmV1 remember R is in this direction.

So the current passing in RL dash is-R and –gm both are currents opposite please remember this is the your current direction to get VA1 is that correct however they will take over this is the

whole current site but both opposite sign so - R –gmV1 x RLM dash is nothing, but V0 than or yeah please ask conduction is in this direction.

So Vin is essentially –R-gmE are some of them actually with a minus sign in to RA when Vo1 however you notice resistance associated PV is how much voltage drop across capacitor is how much V1/V1 ok /R is the resistance is the resistance.

So if I substitute from here in this I will get -I 1 the gm1 IRS X RL is V0 then take V0/I is this V1/I is Rs from here so I write V1-V01 if you keep calling then RGD1 this is the name I gave you see Cgd1 is the capacitance the resistance seen by Cgd1 is Rgd1 which is RS+RL dash +gm1RS r l wonder is that ok just some there is nothing just get the terms correctly ok.

So how I got, which cup resistance I got resistor I associated with Cgd1 I can do same analysis for every capacitor is that correct and if I do this I can get correspondingly our equivalence for each of them ok is that point clear I shown you one every time you must do that circuit draw that and see if there is no current source is gm time will go away from there ok.

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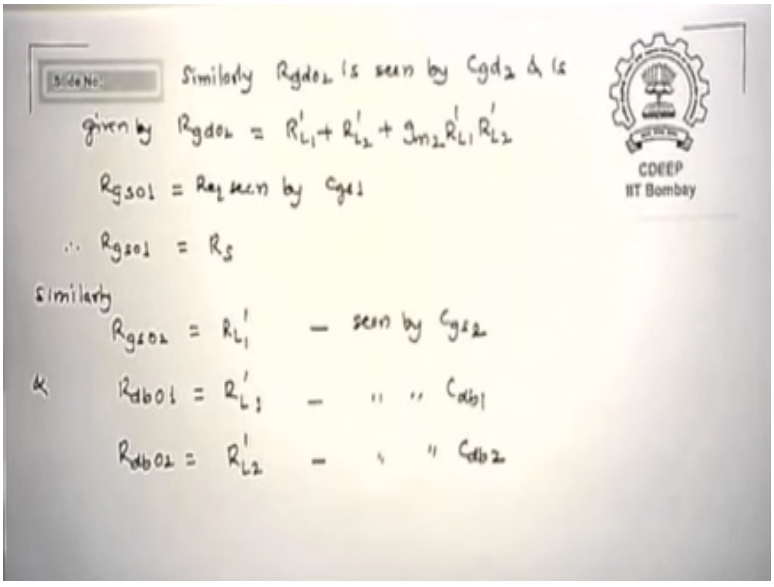

So having shown this similar LGD 2 is CGD then all CGDO2 will be RL1, why this RL1 is coming here what is that RL1 - essentially equivalent the RS for the next stage ok so all over 1

plus RL2 x gm, 2RI1-I2, so this is the distance seen by CGD that is second sketch feedback capacitance CGD ok.

It is identical stage is that correct the first stage and secondly thing is RS is replaced by RL 1 because the RL1 act like a source resistance for the next stage ok similarly then I can see all 0 so 1 is seen by a CGSO1 R01 is how much is R0, so 1 you can see in the circuit how much is this is see you shot this RS will no resistance it will see it RS.

So I said ok if all that so then all 0, so 1 is RS I will wonders which is the RS for the next stage how much is already given how do be I want this capacitance e seeing formal combination of our l1 and l2 because the next stages are short all capacitance are removed, so only resistance in age this much ok alright other all along.

So if I do that this is all DB o one is all l1 my same argument is Rl2 has seen my CDb2, so how I now calculate equivalent resistance seen by all six capacitors is that ok so that is the method I am suggesting see for each of this only the case which will occur wherever the GM terms on the be other times occur then we will get this longer especially simple surface will appear only most cases you will get RL+RS+GM RS kind of rest of the time it is straightforward.

So I will calculate all equivalent resistance seen by capacitance so I can calculate six time constants is that clear RC for all of them is that ok so if I do that then I see our G or so one is TGS1 TGS2 is RJ so3 GS - Cgd1 RJ do and Cgd1 only thing this is long enough because you can say that is the only place where the value is large enough Cgd, Cgd is this, Cdb1, this CD and then by our assumption of 0 value transfer function Theory one can say every stock some of the town at tau is sum of all this tau ok and the dominant pole is 1 upon tau ok.

So, in this method clear to you to everyone what is the method I suggest taking a capacitor find equivalent resistance seen by it take our Cs of all of them some of that 1 upon tau is your whole dominant pole now maybe not today next time I will give one problem show you at all you soulfully and you solved it this the values are very close to each other and therefore valid in the example.

I will take ok please see I are repeatedly telling you the circuit solving which last time I showed putting all nodes all capacitances all everything using neural equation is the ideal solutions is that clear nothing can go wrong in that because we are not missing any term anywhere ok so if you shall know all equations for film equivalent circuit that is the ideal situation but many a times.

I may I know that I am not interested in any other parameter than the bandwidth I can even resort to this technique and can get the solution faster is that clear like first day I showed you if you only use dominant poles then what is the problem we got 0 ok arsenical yeah then you say Nene then how do I so in this assumption where the 0 is not only 1 if that is 11 this theory still is not valid ok.

But in most cases it will happen that 0 will go beyond GBWB that is gain bandwidth 0 1 DB gain bandwidth one day we frequency it will always go beyond that so in most cases unless of course you tailor for the other one change it this will not occur ok and therefore, the solutions are normally ok, but not necessarily every case is correct ok.

So having shown you the tricks which we many of us plane actual designs so I am trying to keep saying you all that if you are only doing analysis do collect analysis why stop it is that correct you are a circuit you draw equivalent solve it now if you are going through a space you does not require any approximation let it put everything there now squall occurrences in let it is all any difficult problem ok.

But if I had to solve numerically in some circuit now I do not know I say ok time constant replicate now it may second say microsecond say Nana oh it now bandwidth is so that is the way designers in the lab do or in the chip design be ok we say ok roughly ionic wire this so should I put W while so much because this gm will help me ok and that is how I keep adjusting value.

When I because remember spies which is a external circuit solver it requires input file from your side ok that means you will have to give that inputs ok now if there are variations how many variations you will try one hundred thousand million so somewhere at least where to start at least

should be known to you ok even if you are going on a spice the first guess has to be released already ok.

Even if you are doing a full circuit analysis using spice so you otherwise what will happen you will get you will put some inputs and you will get some output will always PI's will always solve that as it cannot stop you otherwise but what is the values of GZ and I put it depends on you which currents it will show therefore how many things to be within control you should use is this technique is that that is how we keep telling you.

How we are on a spice it is not arbitrary you have to decide how much otherwise meaning of my graduate student say Oh show a whole night I was working so what was he working he gives some wrong guesses whole night music soon there a spice little there I was called to op which come is he is taking step by step and trying to solve it finally I said it is gave a correct solution after that 23 hours or 23 hours hour.

You did not know anything actually go you were foolish to start with a longer inputs and now you are just doing this repeatedly changing d or some no it will come finally so you have to understand that even using assimilators you ought to be academically sound enough to give correct inputs otherwise the time conversions will never occur ok and therefore solutions will never seen by, so people always say serviced by say we can always yeah.

You can do it and you do it in 10 years, but tomorrow I need the result so what do I do so these theories which we keep telling you the methods we are suggesting are even using you should know otherwise you said everything is doable now no it is not doable ok let us do something different before we could this amplifier this frequency business last time we said in also for analysis that this so called coupling capacitor the shunting capacitor across others are neglected by us ok.

We solve everything just for high frequency and all that the high frequency they were all treated short circuits ok but at frequencies very very low small enough where impedances are not infinite are short or whatever it is they are effective then but at those frequencies the other

capacitors may not be working CJD or Omega is very low then where bad impedance will be infinite.

So the capacitances which were very dominant at high frequency may not be dominant at low frequencies the capacitance which will have impedance is dominating at low frequency will be not dominating at higher frequency so this is the value system which allows us to separate the 2 if they are very close more than this may not be correct then we must take all of them together but these are going to occur CC1 will be of the order of micro farad.

How much less Egd1 and this value last time in the class I said, so I am talking of the order of 10 to power 6 that is 6 or higher or lower values are chosen for the other 2 so these capacitance this value 120 micro farad or 30 micro farad's and on this exam I think you must have already done in a lab.

How much the electrolytic capacitor you are to put across the RE or RS ok very high values ok also a small query which in the lab someone should ask why electrolyte capacitors cannot be their polarity cannot be changed by all other capacitors you can connect both ways ok but it little ID capacitors need to be connected as given plus minus y what will happen of course I will rupture that I can tend to try once it will burst also ok.

But why those come otherwise all capacitances are directionless I mean you can put this way or that way, so Y electrolyte capacitors be here little differently ok they are a polarity dependent ok so much look the effect CC1 CS and CC 2 and which capacitance are now I am neglecting CGS CJD and CV either these are not relevant for me this is a why did I put a signal VD D4 AC is ground.

So this is AC ground this is my AC equivalent I am showing you with an transistor on this is my bias capacitance RG this is our signal this is C C 1 this is all right this is our D and of course there is it RS I should show here now I fell out let us look at the only input side this side how much is VG itself divided this voltage this impedance or resistance divided by the net impedance is that correct into V is Vgs.

So VG is our G upon RG+R signal plus impedance due to capacitance is that clear which is 1 upon s cc1 look at this part in RG 1 parallel R g2 but that is same as equivalent RG because the other term terminal will go to the AC ground are once the second terminal is also going to the AC ground that is ground our g2 is also other terminal is going to the ground so both are in parallel anyway.

So they are equivalent ok so this VG is VN I can do a little readjustment of the turn that is what I say first x SSC1 plus this foot I see one above then tack RG as s1 outside as I did and they of just the terms so I will get our G upon our G+ our signal into s upon S+1 upon CC1 x RG+R signal into same expressions can be converted into this expression what is this value DC because DC means 0 frequency do not so DC per se that is frequency independent term ok.

That is not any 0 kind equivalent leasing this is s upon s plus Omega tau a transfer function kiss counter 1 upon S+Omega other tokens are filter no pass go pass a pure blocker they go a once over it is a high-pass filter ok let us say a transfer function for a high-pass filter so why cannot this start CC1 is giving you high pass filter is that correct.

This has to be understood that this is giving certain up to certain frequency it may not pass but beyond that frequency it will pass is that correct that means below this particular frequency the gain may hold that input may fall out that is VG will be very small or negligible we are not only full VG will be made available this is the trip we want to utilize ok please take it if you read the books it is not identical to what I say there but still you read book much more seriously.

But they give mainly no details and what are you ok but what I will teach here is only that you know how they we look into it what I say essentially is I actually tell you something in between the lines ok and what gives all the lines so do not miss lines or do not miss in between the lines so I am only complementing what is given in the book I am not replicating what book gives please remember I am not duplicating all of it.

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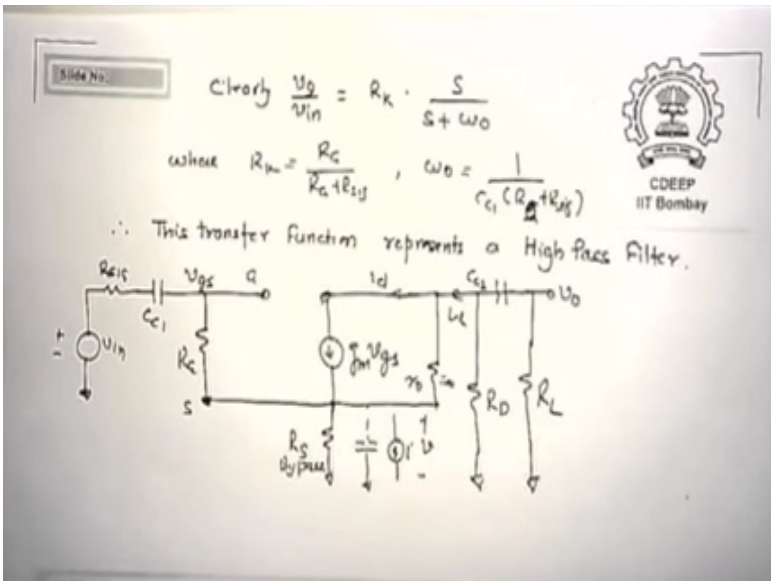

I am only telling you what is they meant by that clearly V0 by way of a transfer function which is some constant into s upon S Omega 0 which is the transformation quite a high pass filter ok so yet through data yes I am as a dictum essentially so do not rod make a how do you expect the bode plot to start if I plot ice again the harmony or Omega energy high pathogenic alga either the high passes.

For either follow joining the aqua hi buzz will on up and this is aware told where it starts becoming constant ok so on are the what we are going to see now that each there are how many capacitances PR3 this is R mid band name so the 3 capacitances must say for example something 3 pulse must appear on due to 3 capacitances and each will actually give rise value 20 DB 40 DB and 60 will be to reach this mid band value is that clear to reach this mid bandwidth and beyond this what will happen gain will become constant.

So this frequency is what let us say this the frequency at which mid band starts and this is our first code so this is called a fault this is called fetch and what is the bandwidth really bandwidth is defined where gain is constant normally if else are very small compared to FH fells are very small compared to FH.

So FS many times we call the FH itself as the bandwidth is something like billing this is one megahertz and this is say 1 kilo Hertz ok so you subtract thousand minus 1 999 kilohertz which

is the as much as one my guards is that clear so many times we do not define bandwidth by FH minus FL.

We may say a fish itself but if FL is not very small as we thought here let us say it is 10 kilo 100 kilo Hertz it is reducing substantially so I must understand what is the value of FL before my assumption that the bandwidth is only FH all otherwise calculate FL and subscribe prom if else you know independently numerically it may get subtracted or not is not your choice.

We just subtract numerically if it is very small it will not be worth 6 decimal or if it is in equivalent will reduce number in first decimal ok so you have to understand that we must even have them every time and numerically value sometimes may not be worth actually subtracting ok but we must know what is the low value itself ok so where is from this now only you are coming there for CC1 CC2 and yes these are the capacitance of being very high, they will start dominating at low frequency is that clear.

So first thing they all only we want to now calculate the effect of CC1 these to see this so CC meant that they operate a diamond which is the pole for CC1. this RS Rgs on let me write again the first pole which I am seeing is our G+R signal into CC1 first of all and maybe we call it Omega P one for the sake of it.

Now we do not know whether Omega P one is the first or second or third we will see values and we will accordingly say which one is 1, 2, 3, but right now we call one our K for example this figure this is the value which we are talking as well is the number than the ark essentially it says that MZ.

If there is a 0, 0 itself that means beyond that the gain is rising anyway when s is 0 means that Omega equal to 0 the 0 occurs what it tells that the 20DB + it should start at right from the head but this are not only Man 1 is a pole which is also now increasing because of the s upon term which essentially you say you divide by this you are equal and Vin if you calculate it is still rising equivalent this is reducing but this is rising ok son average is still rising for you ok.

Where is it still rising that first called high-pass as you rise its then at s is equal to infinite it will become constant which is equal to this you can see what I say it is 1+Omega 0/S, if this becomes infinite or very high this will become constant then I am only saying that this is what transfer function or high pass filter is I have 1S+Omega is a high pass filter ok, will those filters again and we will show.

How it is high pass actually we will evaluate that value ok right now you are showing 1 upon s plus Omega 0 the low pass filter S upon S+Omega 0 is a high pass filter ok at lower frequencies are s is non bypass this fact has to be understood but at higher frequency RSA bypass so this in calculation of low frequency RS cannot be neglected because RS is used for DC RS is a coming there is that correct this is only bypass man then frequencies are very high.

Otherwise RS appears because this impedance is not shorting RS this is finite the capacitance due to CS 1 upon Omega C s is comparable with RS so RS cannot be neglected, but if that is equivalent to 0 then we say RS is shorted is that clear said no frequency RS must be considered at now frequency CS is not shouting at high frequency CS shorts and therefore RS shots across R java method because on a time constant was Kelly.

I am a barber now a few arm a like a problem I tell you but then a capacitor will look tile-based, I hope ok if that show has done for one of the capacitance waste you try yourself I will take a case of say CC 2 it is at the output side please look at the circuit again so this capacitance this is the RL and this is the already input a shorter corresponding with these gods so we say CC 2 V1-V2rd and RL.

So how much is our equivalent for that others done the even is our LDV2-IRlV2 and -V2 bar is V/ZRd + RL, so what is the equivalent resistance seen by CC-I do plus RL so policy C2 is RCC2 x CCC2 which will give me the SEC another pole which is 1 upon 2 pi RC 2 CC - I have been analysis for all 2 but I am showing you the final result tribe methods are suggested then the poles occurring due to the CS capacitance shorting RS across others can be given as GM/CS.

Solve the same method as I suggested GM/CS the GM go awry rapper can you think why it is coming please look at it this current is passing through RS we are then coming source with source resistance same method I am using this current is passing through so this voltage is this drop Plus this job and that is what that GM term is appearing ok, please note that what we did earlier ok.

So another pattern which I see due to CS is GM/CS ok how much will be CC1+ is your indicator same method Cibola a figure named Ellicott Naga RU+ our signal that is the only color resistance it will see these methods are not so very common in the books of course you can go and now read the book I there are four of them which are I give they had little more rigorous or maybe they are putting some areas looking gray to the GM equivalent.

This finally what they will get is what I am getting without doing all that that is the way I do it is that come clear you sound complete circuit everything comes you do not have to do any of my methods but I always show you plus something which is otherwise known to others opt game in an ammeter up ok if that is so last part we write ok.

This also is done follow me if we see there are 2 thoughts Omega P1 due to CC1 Omega P2 due to see s and Omega P3C this since we know roughly the values they figure out Omega P1 occurs here Omega P2 occurs here Omega P3 occurs here this is the bode plot you will say it can be Omega 3 also which overcomes, but by general knowledge of the values we use our GS we use our signal.

We use you can see why this is the lowest can you think because error function make sub cell Louis like a trap for our G is very high honor, so obviously that will come first ok, then between the 2 also, but because the CC to our very high ok this will actually come this it will come the last but I know this may change once a while because GM Valley's decided by the current I bias ok.

That may change some values but I left now because CS is you are higher this will start down please remember CS is relatively very high shorting the RS the capacitance are 30 micro farad,

25 micro farad, so GM/CS will be earlier than Omega P3, but if happens to me then call this Omega P3 and column AI, do not tell me when they give you but since I know CS are very high they and then of course.

I am not as high energies therefore first will come this then it will come this and then it will this is 20 this is 40 this is 60 ok you are perfect he is right essentially what we are saying that once your round is the certain pulse picks over and then it also gives another 20 DB the comma separated it must decrease a sense you know what we say it is a pole means it will decrease 60 to 40 or rather 20 ok is that clear it is a minus 20 DB from their head.

So where is that ok and then it you charge so notice FM here which one you repel Omega P3 is the 1 upon 2 pi f LS Omega P3 so I got my lowest cutoff frequency which I can evaluate and say ok this is the FL FS, how do I calculate by my dominant pole theory I get my fetch and FH-FNH the bandwidth please remember an amplifier which 2 parameters are of interest was the gain and the bandwidth.

So we evaluated both of them ok, what is the third one which is also worrying us please share this but somehow are showing stable phases less than 180 aware perfect phase margin as it is called but what else there is a another term which is worrying us which we never so far calculated in every system that first we must calculate what is that power the most worrisome part in all of this at the end of the way we find it is the power dissipation which will limit ok.

Everything ok, sentence which I said was I am dear to you I do not know design is not our power amplifier when I say power amplifier I want higher power is not it that is what I meant by power amplifier there were voltage amplifier normal currently so I say power and then I said now you please design in now power amplifier.

What do I mean what did I make me amend that time the dissipation should be very low in the devices or the circuit but the delay of power to the load should be as high as possible is that correct so that is also called low power amplifier because you not need large power to be delivered but you do not want the circuit to dissipate larger power ok.

Sometimes this phone is made low power amplifier so it is essentially meant this ok ok so this finishes all kinds of normal amplifiers single stage others which I have not done please read common source common gate common emitter follower all of them are given in both method is identical to all of them the most important of all of these all the fires are not very single-ended amplifiers ok.

Which amplifier we use max, already started working on it this amplifier chip you are using ok so is the open is essentially different from all that we did yeah it is somewhere different but it follows much of the laws which we discussed in single ended amplifier, so that amplifier open has 2 stages maybe n stages also you can do a typical Oh will help first blow up as we shall call differential amplifier ok.

Then I will put it second stage we will say gain stage and finally the typical op-amp has 2 stages differential followed by a gain stage followed by a buffer stage ok, so any op am you see you see or know how do you see all of this you only see this of course this plus minus is relevant but it is care of coordinator bias points they also show here +VDD-VSS this is your Vin some way connected and this is your V.

So, open essentially contains a below time a case should have around 22 transistors with a clamp loop and make it now transistor level a dome a bias transistor hmm so it is a real simple looking things but individually if you see it is not very difficult, so let us look from this stage I should start it before I go for a you know different first stage in the open is different so let us see if M the word deform essentially is called differential amplifier ok.

There is also a difference amplifier which is not same as differential amplifier please take out there is a word which we will use called difference amplifier there it is similar, but not saved so do not this do not make same name difference amplifiers and differential amplifiers are different as far as their outputs are concerned the architecture may not be very different ok, so please take this in your mind sometimes someone very casually uses.

So, I thought I should explain you there are 2 kinds of de femme in the market opens on the market one using B, which ones you are using the numbers right now 741, which is mostly bipolar ok seven more seven for one C is a device so either you can get fan or you can get BJT defense all the differential amplifiers have 2 inputs V in one and V in to ok.

Then, we define 2 different to signals for any difference differential amplifier 1 we call difference signal what we call is difference signal which is called V ID I stand for input D for difference is that correct v ID ID R subscript V is the voltage ID so VI D means input difference voltage which is subtraction of the 2 inputs we in 1- V x K.

So what science we already can have we already can have with signs both are 1 though because V in one can be larger than V into or vein - can be larger than V in one if you define being 1 - we have V into as VI D it can be are either plus or minus is that ok + - we already can be +- depending on which one is higher or lower we define a wireless signal which is called common mode signal called VCM common mode.

Which is nothing but the average of the 2 way in 1 + V x 2 these are the 2 input signals, we will use in all our differential amplifier theory ok now first thing first why are we so keen about differ a bit on all amplifiers we have seen we can have again of any stage by cascading or by cascading ok.

I can also fool people by not losing bandwidth, but getting the gray hire, so why I am interested in differential amplifier so here are some big advantage with differential amplifier gives overall sing amplifiers major advantage uh become is it has a much higher humidity to environmental noise that means if the knowledge is please remember in a normal single under amplifier at the input if noise comes.

What will happen at the output noise will also get amplified by the amplifier along with the signal so unpiloted after pass minimal a motto and noisily, so I still on it at the noisy noise become common so either if you use single and amplifier noise cannot be illuminant of course I

should not say that word because we do try that also but I got now we say normal common stage cascade or stage noise is enhancing every gain stage because that also sees the same gain ok.

So, the fan has the biggest advantage that it illuminates so-called this noise that is what we are looking for why we are looking for a reduction in noise because we want signal to be amplified and not noise what is the term we use for this signal to be amplified higher than the noise then what is the ratio we look for signal to noise ratio.

So, what we are really looking for any amplifier is large signal to noise ratio SNR that is called s and our signal to noise ratio ok so all amplifier should show higher signal to noise ratio single and amplifiers do not do that ok because there is in our third maintained let me say now you also get announced I want to improve ok.

So, how do I do is the differential amplifier improves is enough that is what it is alpha also allows you higher voltage swings than the singer by what is in the higher voltage sing a larger signals larger swing of signals what happens in a single ended amplify what will happen if the input signal is very high we kept saying on day one small signal small signal if signal is higher what will happen saturation harmonics will start coming other a frequency component will also come.

So, it will start saturating compare the signal under this can be a larger swings that is the trick of the trade actually were large in here it can a pair of assault all the racket or if there is a lot IQ signal bang sort of fooling hands, but there is only one disadvantage how many transistors single ended will require one transistors ok here.

The minimum requirement is 2 transistors or more as I say as you please team to login me what duloxetine as I said total number of devices required on the Omega 22 minimum so or will accept so none of the additional area penalty on the chip,""/ ……if you are making a chip of an analog block, otherwise the form is very good very good and it is difference gain as we shall see is extremely high.

How much any one typically difference amplifier or differential amplifier has a large open circuit gain is very hot and to call for a 10 to power 5 how much is normal gain of an amplifier 10, 20, 100,000 maximum 600 to 700, I can go to 10 to power 5 ok that is the biggest advantage they found will provide very large gains it can create an open circuit system you will see what that word means all to single mm amplifiers m1 related to this m2 related to this is a clear.

I had 2 single engine amplifiers how and power supply voltage drains are common the only thing was now I am saying I am substituting inputs being one and waiting to do the truth amplifiers and I am picking up 2 output voltage V01 and viewable but what I am going to do if in the general this amplifier is all I can solve individually fire to solve I can solve but what I will be interested in what is being one- being amplification to be A1-VO ratio.

What I am looking for output difference VRM-Vo - is the outfit difference divided by difference Vin 1- V what is that value that is where the difference amplifier is differential is that correct is that point clear the difference of input and difference of output I can also say 1 at the output divided by difference input that also I can look into is that clear that is we want to know whether by VN 1 - V or VAY 1/ 1-V 2 also can be of interest this devices are these are called single mended outputs.

When only one of the output is of interest us that limit event but only one is of interest to us so we will see both of them if I do this and these are then I had 2 independent biasing for both of them is that layer because there are 2 amplifiers all require bias for both of them they were salted the current source here current source here.

So I know 2 current sources to bias independently and they may not be identical any time is that clear so I said ok why not I will join the shores of the 2 transistor and connect the comments current source is that were clear to you here if I put up I will require one current source here one current source here ok.

They may not be identical in many cases may be identical but but I need to source I have moles done and put one common source common current source ok what is current source doing the biasing the 2 transistors is that care by thing that were and where should they get biased what is the state of these 2 transistor should be all the time saturation they must remain in such is the command of saturation they long amplify this will go to linear more cell ok or cutoff modes.

So, they must remain in such as that is our condition for amplification right now they can be different but in most cases if you are in a single silicon chip howdy one it must will be equal to RD2 it so if you go in the lab you pick up these 2 separate amplifier and connect them in this 2 may not be identical even if you let say you trailer 47 kilo ohms resistor to 47 kilo ohm resistor beam on top other 7 kilo ohm exact values some may I for the 7.15 some may have 47, 46.9.

You there are more task 47 key, so how do one may not be identical to external if you put 2 devices in a but if I am no than a signature small area I can more lightly sororities would be equal so is that one now getting clear do you guys sing opens are not made by making simple separate MOS transistors and hooked up on the board is that point clear to you because nothing can be then made yeah and one cannot be same as EM to an end to separate turns you buy ok.

M2 or M1, they can never guidance cavity same seemingly ok June I got but on a single chip that is one less than 10 micron area micron square area I can almost ensure that both transistors are identical both have Center showed the resistance values are same so all the time such circuits should be always integrated circuits and not discrete circuits is that clear because this straight circuit will lose all this advantage ok.

So, all opens will be always ICS and not made the an experiment uh a set of 990s I think it continued for a while I do not know now I purchase some loss arrays ok that means on a single G more than one transistors maybe each has available so they are into you use there is a risk and then create because since on a single all those runs have you made they will have almost identical properties.

So, there is race through which you can try making an open at least if an in your lab and you say it may come closer to what you are looking for no still it will be good but at least it will come closer to this where on a single chip everything is acceptable are these will be same these 2 runs will be identical how much non ideality either non identical term you can tolerate is another is called variability show.

Some other time we will discuss that very late they also is an issue but not here if I see its input output characteristics while we are interested in doing all this if I plant then one - that is the difference VS VID which is V2-V1 is shown here but individually if I plot V out 2 and V1 I figure out the V out 1 will follow this curve and we have to follow with this curve and somewhere here both will cross halfway this is very important point the out one.

I saw I got it, person each Geiger become value means I got or am will talk Ida what does that means M1 M2 are complementary occur there - on each I do forget DG IRA, this is the trick which define is playing is that correct because I connected their sources and I am now applyingVN1 V in truth change in V1 V2 this feature word which transistor will start conducting ok.

Because of that I will get and if I subscribed without one way out taupe and plot VI D the typical curve will be like this what is this range should be called this is the linear range that is the plus minus VI D this is the only plus - we already acceptable for D fan for which gain what will happen to here it is constant ok constant means what 0 gain or high gain 0 gain no change in output, but change in input so gains are 0.

So only in this range they found they will operate is that correct because they need changing DV by d VN is changing has that correct here it is 0 here it is 0, so this is changing that ok this one is very important this is called input range ok up to which the FM will operate we will show you this latter if the fellow quit last minute as I said and define the noise is eliminated that is what I said you can see being 1 and being and I said nice because they are close by same area.

So whatever noise appears here will also appear here is that clear and now we will see noise does not come because the source noise come from the environment is that clear noise come from the systems EMI will be interference a you see resistances you can cable at a passing what is up Kelly same of it, ok.

So, generally then environmental noises are identically in a small area if you show this area why when they are the noise my voice is noisy let us say and you are not shouting so you are nice is 0 there so it is a differential but in chip the noise will be almost same for both it is like over reading whatever is true it will all read on both inputs and then the game, which I am looking which we say Vin 1+V x/2 and if the noise is same what is the common mode value will be same as one of the noise and the output will become 0.

What I am going to say so what will happen noise will get in a minute at the airport this is exactly what I am looking in a define that Colin mode signals should not get amplification but different signal should get amplified so common means which once noise is common.

So, they that will get illuminated signals are different voltages here they will get amplified there for a DES fan has advantage that it improves the plane of a different signal but actually removes the common mode signals is that clear that is the advantage of differential amplifiers, see you then.