Analog Circuits
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Lecture – 13
Frequency Response of Amplifier

Okay, here we go, last time, yes, we started looking into operational amplifier and we said the first stage of an operational amplifier is a deform differential amplifier and if you are used to them recently you are seen that there are two terminals one they called V- the other they called V+ are essentially the tau input terminals of a difference okay.

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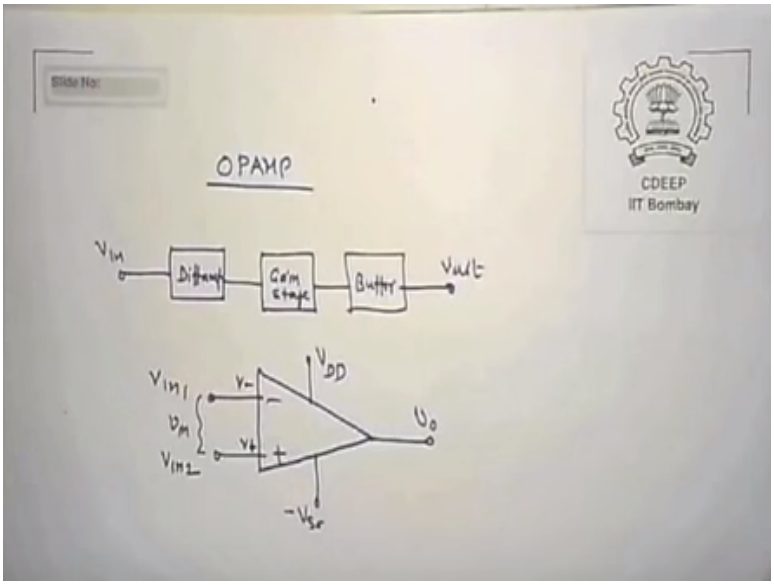

So we are already done something, but I just want to recollect so you can see the input to our Pam is essentially input to a differential amplifier. Now this here, shown here is there is only one output there is a possibility that it may have two outputs so call it VO1 VO2 and I can actually take a difference between the two and can get VO1-VO2 as my new outputs.

I may see I only get one of those outputs the other is not relevant. The way I do as in most of camps and we say that is my view. That one small thing you must understand, the circuit shown here or the symbol shown here does not have any connection between V0 and when except for the capacitances there are Cgds and they will give some connection.

So there will be poles and 0s associated all the time even if we do not say there are capacitances. However all OP-AMP circuits barring exceptions are safe. There are no internal capacitances CC1 CC2 or CC. There is no such capacitances present in any operational amplifier so what is the advantage of such system, what does CC1 and CC2 doing they were decoupling DC and AC.

So the trick here is, now, what I am saying that an OP-AMP can also this DC inputs is that correct OP-AMP can receive DC input all our amplifiers. We do not amplify DC, what do we amplify, only AC signals but this difference from all normal single ended amplifier de femme is or the firm is that one can amplifier DC signals is that correct, that is the major difference between normal single ended amplifier which are small signal AC amplifiers.

So, if I really plot the bode plot, for that what will be the typical gain you will see from here if I play it, gain versus frequency at 0 frequency gain. It is not 0 are not following so typical characteristics of a bode plot will be something like this. Even at DC 0 frequency there will be a finite DC gain.

Now this DC gain is same as what we say other well DC gain. So, that is the major difference we should understand that in the case of photons or in defense even at DC outputs are possible is that correct so in all my analysis ahead why I am showing this? I am actually not differentiating too much between small id and capital ID.

So I may use the term like ID which actually takes care of AC+DC. All only DC are only IC as if I am having some signal which is getting at the outputs, okay, is that clear to you? So that is right symbolization sometimes because you know we have been talking single ended amplifiers, small signal ones and we have very categorically saying, small we sell put a CS only okay here.

We may see what is the difference, however, normal gain of this amplifier which is a small signal gain is still an AC gain. Whereas the DC gains are not possible if this circuit acts. What will happen if there is an input signal between this input terminal the output because, there will be large gain of an amplifier the output will go where gain times the input.

Where it will go very large value, but the maximum value available to your ward maximum minimum, VDD and VSS so actually the output may become either VDD or VSS depending on this. However this is, however is that clear what this circuit should be called therefore I have two inputs if this is how this goes to-VSS, if this is higher compared to this. This goes to +VDD compare repair.

So I can now use the same of thumb, if I compare the two inputs are depending on the output whether it is VD D or VSS one can declare VDD as 1-VSS 0 and therefore it is like a logic block. Two input signals can be compared and the output can become digital 1 and 0 is that correct, this is the advantage of open over normal single ended amplifier and therefore we want to know what exactly goes in how this is possible and that is why the present thing we have started with differential amplifier, is that clear?

Why we are soaking, because every other circuit in future will use open and whether it is A to D converters or D to A converters or any filters. Everywhere will use operational amplifiers and since we are going to use operational amplifier the first thing we must know what it contains and why it gives such a behavior which we are can then utilize and read in systems, is that okay?

So, this issue which yesterday or deficit I did not say I thought I just started. You can, because it was a, I mean, let late in the class I thought maybe that time I did not spend time but you must know my context why I am doing this. I do not do anything here which I do not think I will use later unless I have some reasons to say okay.

I will I know it is important but I do not want to use it right now. I say whenever I do something it has a repercussions ahead, that is why the whatever teach Rho will be required tomorrow. Tomorrow means next ok, have not shown you the operation characteristics, operational amplifiers. So, also one interesting feature about this opens is this which is also interesting to show you because, if I plot VO vs Vin of it operational amplifier, depending on if I can ground this and take a reference - Vin also can occur.

So, I will find, sorry. It will cross to 0 there is a range in which 4-Vin or +Vin the output will be high. I mean linearly follow it and at certain higher input signal, it will start saturating. So, even in open, there is a limit up to which inputs wings will be allowed to have larger outputs beyond which what will happen, they will saturate and then what is the essentially whenever the output saturates, what is the gain?

Gain is 0 essentially it will never reach 0, but it will be a very small gains. It will start coming closer to , and because of that the outputs will be non-linear, and nonlinear, if I expand it in a Taylor series or Fourier series ,then I will get different frequency components Omega 1, Omega 2, Omega 1 to Omega 2, Omega and +- Omega 2, these are called harmonics okay.

So if you operate somewhere here, not only Omega 1, your major frequency output will appear , which will be much reduced, because part of the power will be delivered to other frequency components, is that clear? So one does not want to operate in the saturation, around saturation region, so there is a limited range, a one for DC is that correct, it is even for DC there is a limited range, in which amplifier will act like a linear amplifier is that clear.

Otherwise it will be a nonlinear amplification, in which it means that other frequency components will start addressing power okay this fact has to be understood, that even I keep saying DC it does not mean 100 the word I apply, and I will get thousand volts because if that happens, it will be a great thing you know with a small device.

I can have a generators put everywhere in the houses and I can supply power without any power coming from anywhere, else such a thing thermodynamics will not allow; so therefore there cannot be energy creation, without any other creation giving energy, so do not believe that it will have infinite ranges it will have limited ranges for amplifications as well.

Yes no because linear region is sine Omega T term all sine Omega terms will only get amplified, no I tell as I say, you please come do not confuse between DC and AC signals.

We will get all other frequency components, DC signal cannot get it with just a 0 to 1 DC value on the + side or the-side, is that we are clear to you if I have the only DC inputs either it will go to VDD at the output, or VSS okay but if AC signal over reading a bias voltage, then that AC signal in the non saturation region you see understand; how do I write down saturation a 0+A1 X+A2 X square, you write the expansion Series X square term will sine square Omega T sine square Omega T means 2 sine Omega t-1.

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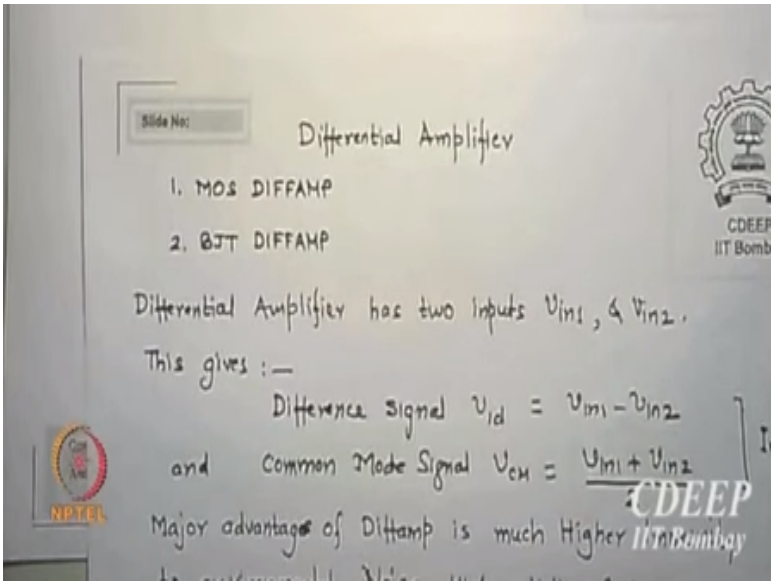

So 2 Omega term appear, do you take the Q will get 3 Omega D terms, so you can see when small signal AC goes, it will give harmonics DC does not, is that clear it will give it as fixed value of 2 DC 1 that is what comparator does it actually fixes it to fixed 2 values. So it willing enhancement that much gain .Whatever DC value input you have into the gain that is the DV0/DV.

Which is your gain m multiplied by the DC input that is output voltage. Right well not because in those regions there is no signal, okay the device is not introducing any harmonics from itself. The device gives you no non-, harmonic content because in nonlinear relationship the term square cube for terms of occurring, and that only when you are sine Omega T as signal.

Then sine square Omega D sine cube Omega T they will give 2 Omega T 3 Omega T and combination of these, as these signals okay . So only AC is giving you this kind of okay they

looked into yesterday that their differential amplifier can be in the differential amplifier or it can be BJT I will not do B or maybe at the end of this diff I am I may just show you a bipolar which are deform.

I may solve something the similar thing has happened in moss, but other things you read in the book which I officially said Sandra Smith and me okay. So you read there the other parts of bipolars. Okay I will only do mast parts and will expect you that you read bipolars if you have to be sure that okay it is not same and it is not correctly coming, and you do not understand that part we may do again in the class.

Otherwise we assume that techniques are same and therefore can be applied to any other blocks as well. So we said we define two signals fbn1 and we in two are my inputs to a differential play which has two input ended signal, to sing it is not single-ended the two inputs then we define signals as VI D which is abstraction of the green one ,and V into whereas there is another signal we called common mode which is the average of the two Vin1+V x /2.

Now as I said yesterday the term has the advantage that same noise normally is common mode what does it mean?On the both terminal noise has same sense. Okay our same amplitudes and the diff am has the biggest advantage. That it rejects common mode signals. That means anything which is common output does not show that is that clear.

So if there is a noise or reading on your signal , and if it is common mode, which should have been normally occurr, then the output will not show noise amplification .Is that clear. That is the advantage, why the fans are open, are used because it rejects other signals which is common mode, and the word there, we use it what common mode rejection ratio, how much it can reject, this the criteria the good of an large CMRR should be good but this word.

She will come back and say no, do not go 125 DB a seminar, or 200 C because if that happens something else will be hurt heavily. Your bandwidth may not with your phase will not be occurring , so there are issues but larger the CMRR, larger is the CMRR other , the better is the

circuit for operational or defense okay .So minimum deform CMRR should be around 80 to 85 DB. Should exceed a not more than 120 DB but around that 120 is okay.

I am not saying it is bad but never trough a cm error of 200. Okay in fact theoretically the CMRR may come as infinite , how much chaotically ideal situation cm are not is in finite, okay but there is nothing ideal in the world, so CMRR is never infinite in the world. Okay so you will see why that does not occur. Okay so this is just what we did yesterday okay.

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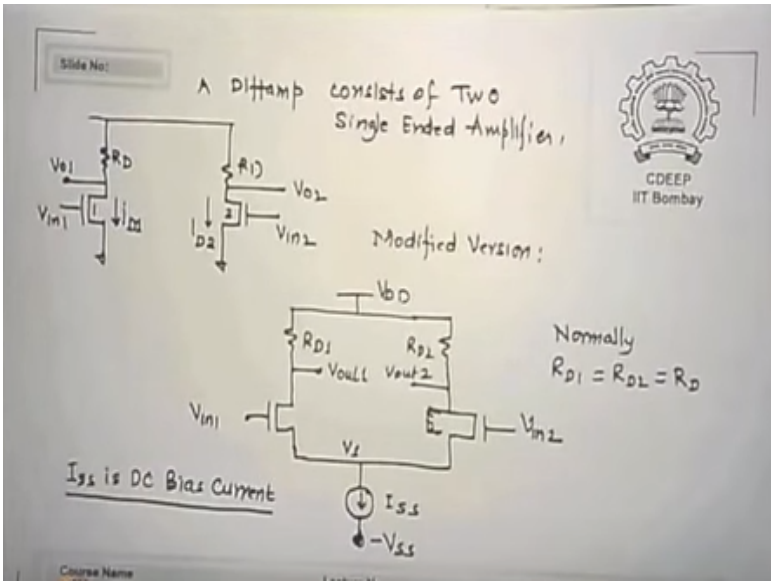

We said a deform has to signal, and an amplifier in which their sources are connected and two resistances, there are two single linear amplifiers as shown are do 1 is equal to Rd 2 equal to Rd. Then this is the circuit which we call the differential amplifier , or deform in short diff. This is the biasing current. It is inverse. It is normally called Isis and bipolar they call it ICC or just I okay.

So if you are doing otherwise, just look. They only may cause capital I. That is it VSS is the negative supply so opens with always are having dual rail power supply . What is module L+VDD and-VSS. But there are single lane op amps also available. That is only will G. Is that clear. I am not trying to say that single LO times are bad or worse of course that they are worse than dual rail power supply based on amps.

This has I repeat again has anyone started looking why negative voltages are relevant in analoge, rather than digital. We never look for it. Think of it, what is the advantage. The difference while still I am VDD-VSS - way that the net voltage if it is 2.5, 2.5 it is 5 volts so I have got I will put 5 volt single supply if our power supply can make 2 point 5-2 point 5 which is also 5 oh I make 5 0 but why I do 2 point 5-2 and normally we also see that the same opposite is offering 2.5, 2.5, 3 and2 okay.

That also has some disadvantage so think of it may be at the end of a pan I will say why dual lens the oils are very relevant okay some partial answers I give someone who watch me here but I will give them more detail later let us say the first case deform please remember I again show this Vin1 Vin2 are the two inputs and the common mode is Vin 1+V in 2/2 different signals is Vin1-Vin2.

Let us say the fan has same inputs at the both and Vin1 and Vin2 is that cut so how much is difference 0 but what is the common mode VN+Vin/2 means Vin is that correct Vin1+Vin2 if they are equal that means both side the signals are so beam okay so then 1 is equal to V into and since they are connected at the gates VG1 and that is equal to VG2 is that correct.

This is the common mode part in that now you can see from here in our circuit can I show you a little bit the source of both call it M1 M2 for future source of this both transistors are connected common they are same so what will be the potential on both side will be different or same same because at a at any node there can be only single voltage that voltage.

I call BS source voltage is that correct so how much is VG s for this we in 1-V s how much is this being 2-VS the Vgs 4M2 but since V1=V2 and call it VN both transistors have same Vgs is that correct if they are same devices of same threshold Vgs-VT is also same let us say is S is so balanced that they give sufficient current so that both devices remain in saturation so what is that means this current half will come here half will come here.

Because both are laden Vgs-VT is same for both devices is that correct because if they are equal PTS are same the half of current must flow through them that is exactly what she said yes we do

not apply it comes if I apply B in one window there will be a possibility that they may be equal at a point is that yeah.

So common mode is there not necessarily of course noise if essentially is a common mode signal here I show you the game there how do we given a different signal it can always be represented some of common mode and ok so we say VG1=VG2=VGS1=VGS tube and we define VCM as Vin1 even 2Vgs1 VGs 2 and the source voltage is of course VGS.

We say M-Vgs what is what is sex or not VDS actually it is VG VG-VR is the signal there VGS so we say Vin is source voltage is Vgs-VT is that correct Vgs-VT is the drop across that that is we define as VOV-Vgs we define as wavy so we substitute this is Vgs1=Vgs 2, one can always say that ID1-ID2 are equal if they are half situation.

If they are equal but even if they are not equal they show now please take it here they are equal that correct even 2Vin1 is not same as being to one may have a larger current than the other but the net current will be how much also that is what you fixed so sum of ID1+I do 2 will always be equal to if they are equal.

So which each will be is S/2 if not equal 1 will have a larger value than the other this is what the allows if they are equal half of if they are not equal one will draw larger other will be drawing smaller but sum total will only come - I said independently this is exactly what we are looking into okay VG-V s is VDS but we s is common to both okay.

So is that clear to you because the subtraction is same for both is that concerned because V s is common voltage okay so if I do that if I do n is equal to ID - it is S/2 but we know the current in the AI this is – W/L/2 Vgs-VT square is s is then represented a VOV square so VOV is - is s upon beta and - by W/L at what point but where is this defined when the current is half half in both circuits is that clear our d1 is S/2 and ID 2 is also our size by 2 for this condition.

VOV has been defined normally we do not defined that way we define only normal but in this case for the common node ID1=ID2 and at that condition the VOV is defined by two isis upon

Vita and - into W by our mats a scalar Lajoie squeezer yeah okay, this half this is half B ty w is w ball but the current change this is RSS please remember.

What is Isis if one of the device is working it is beta and -/2 is-VT square if it is half current how the current will go to I/2 on one side Isis by the other side I agree what you are saying I fully appreciate but okay call it like this to say that okay if one of the device is operating normally we define that my VOV if one of the transistors since it is harmed the current for individual cases when equal currents are there we now define a new VOV.

Which is related to half currents I also scatter pure formula other can way or the other can be asked is that clear and for that we define new view that is for single transistor with one drive completely driven by it but since it will be half off then I said for that half P define new view this is not I agree ringing like I define usual I kept normal so to additional two terms somewhere there fair enough nothing goes wrong is that clear it is only a normal creature.

Which Sarah Smith has been using and I thought says you are going to read that book I should follow their nomenclature I realize I myself would not have done it I agree with you what does he say this for while this half is coming here this half is essentially this is a normal I ideas current for any transistor so I say if only I is flowing in one transistor ha beta into Vgs-VT should have been the current is that correct but since each is going only.

I assess by two I am just dividing it by huh both sides that is what I am saying you know when one transistor works if that is what the definition was something like this that if only one of the two transistor works the other does not all the current will flow through one and that I call heart beating – W/L x Vgs-VT square.

Whatever videos for that transistor is that clear to you that is the current it will flow now you say if it is half off then the VG is equal still equal okay but the current is now shifted half up so I derive the current by half old one whatever we use earlier I divert other either okay we will come back to modify curious at the do not worry this is what they are than it are normally I will agree I would not have done it.

But since they are following this method I thought I should give you their method okay you are perfectly justified so what is VD now can you tell me VD okay, so that is a drag at the drain the resistor drop I into R is the VDD-that should be the output voltage so VD 1 is equal to VD 2 equal to VO1=VO2 is VDD-is s by taught by 2 times Rd if R these are equal otherwise they may also not be same then what is the output subtract subtraction of VO1 and VO to 0.

If they are 0 what do you expect again if the output which is defined by me as VO1-VO2 and input is how much common node Vin=V1=Vin2 so what is the common mode gain what is the common mode gain output voltage divided by common mode signal output voltage in how much 0 VO1-VO2 is 0 so the common mode gain is 0.

In the case of differential amplifier that is what the rejection word is clear to you that any signal which is will not get amplified at the output if the difference of output is collective is that here if the difference is collected VO1-VO2 there is no gain for the common mode signals now question is this valid statement because it is not true because the wave will define later which we just now said word CMRR is essentially called ad indifference gained upon common mode gain okay.

So what is CMR alpha days infinite and I will say ideally that means this condition which I have put is an ideal condition ACM is 0 is an ideal condition why does not occur as 0 and how much it will occur will go and Chile evaluate the issue is that kind no it is not to four it is equal in common mode the signals are same VN1=V2 is only common mode correct.

So the curve if the 2 signals have a component which is dif possible they will get amplified but the common will reject itself yeah but we already said we will always operate in the Linnaean mode that is what as day 1 I started we will see to it your biasing is such and VO VN is such restricted that we are always in the linear mode that superposition is guaranteed by us is that correct that is what I started with you.

When I show you that I am always going to stick in this is that clear and that condition is still valid if you are doubt is doubt so let us clear the doubt if this is for any transistor this is my VG

and this is my VS if this is my VG and this is my VS so what is Vgs VG to-VSS Vgs to Vgs say VG1-VS is Vgs 1 if S1 is Vgs1=Vgs to Vgs1 it must be equal to VDS - that is what I said yeah that that is because the difference between the two is same what I said it is ok oh sorry.

I made a mistake I should direct Vgs Vg1-Vg2 is always equal to Vgs11-V yeah I agree with you yeah your point of view well what I said maybe I wrong what I ascension is saying what she is saying is that the difference is equal Vgs = Vgs yeah you are right the idea all that yes since it is common this it will also get as it close to 0 the reason why I said for AC this potential will go to 0 so that is for that AC part yes they are equal for DC.

They are not alright yeah you are not VG s 1 is equal to VGs 2, ok perfectly justified ok normally our assumption in this that all transistors are identical all resistances are identical and the current source is ideal current so please put these three conditions in deriving this thing we made three possible this one is the two transistors are fully identical the W boils are equal the thresholds are equal okay seven condition.

We said are these are exactly equal and third condition say the current biasing current source is ideal is that correct if there is a resistance there may have some issues okay three conditions are called ideal conditions under bad state yes the common mode gain will be infinite in finite alga sorry 0 and therefore CMRR will become in finite please the three continues actually our three conditions okay.

I should say third one also and I assess is ideal current source I will come to this very soon and I will show you why I said so otherwise the current in both VO1 VO2 will be different for both even if the currents are same so so essentially VO1-VO2 will never be 0 then even for half currents if R these are not equal then the drop across them are not equal so the subtraction will not be 0.

So that should I say says if they are not equal that means there will be some difference voltage so common mode will not go to 0 there will be some finite value is that your V1-V okay will not become 0 then it will have some value which will be smaller because all D1 or D2 even if they

are not equal they may not be true for 110 200 Canova 10.05 ok then 1 0 2 K that is because of the process which later on registers are made one cannot guarantee.

But how do we say we guarantee on these circuits why did I say in integrated circuits this is very well this case nothing is doable is that correct indiscreet I can never guarantee our D 1 equal to Rd to keep now be sold registers lay cow says most of the meter given to you to monitor is you are only using o meter whose car lease count is as a direct he pen point 0 chaotic which were correctness they innocent.

So, you always feel both are ten okay essentially if you have a good measurement system you will find they are not equal and if they are not equal even if everything else VT equal but the meter will not be equal for two transistors okay so in which case what is going to happen is VO1-VO2 will be some finite quantity which means will be some finite small quantity but spy night quantities are really it should go to 0.

Therefore, CMRR rejection should be almost infinite ok however is this number is what we are going to see as I say how much I said you please remember this is range you must work in real circuits 80 to 120 degree many CMRR like is that ok these numbers are only for those who are someday going to work on individual kids designs for these numbers are crucial ok ok.

There are two these are two may I am just this is not the ideal but I am explaining the just there is another term which all Graham people use they call input common mode range what they call eights ICMR and this is essentially coming from the deform itself so shown here is that were clear input common mode range so what does that mean in your mind without seeing this what does that I mean input common mode range.

So what is the max and minimum common mode voltage which are possible which will allow device to operate and saturation mode transistor to remain in saturation and in linear mode is that correct if that occurs we say this is the maximum Vcm and another is minimum VS you must work within this so what does that mean if the knowledge or is this value then it will show you at the output as well is that clear.

So there is a limited range in which VCM can be operated okay here are some tricks on that yeah general method map to but I without the scanner in here hooray circuit wallow Cali ahead whenever I want to get a maximum value which is occurring at the input you always go from VDD you calculate from VDD down is that correct.

Whenever I went the minimum value you should always calculate from ground or-VSS towards the input is that point clear these two terminologies you take independent of this which I am going to use I repeat for the maximum value you come from this for the minimum value you come from this whether any maximum values are included you are trying to see for maximum start from power supply and for the millions are from-VSS either fake it.

Now or either say that means that same manner decided by videos of this and Rd of this we know mainly decided by this as well as the VGA sir is that clear so these two values are different from each other and one gives max other gives minimum this is true for this circuit for any circuit in this such calculations are to be performed is that correct I repeat for the match start from higher end to the point.

Where you want and for the minimum go from the lowest end to the point where you want to come this is the standard method which should go here independent that what I am going to teach now okay this I keep saying it because you should know the wavelets we follow later okay so we say we shall occurs when M one and two are the age of saturation when both transistor are at the age of saturation.

We say that is Vgs-VT is equal to VDS so we say what is common law at the gate source voltage okay so VC max-VT=VDD-ISS already harmed the current vote resistor on ha path maximum-VT= V is that current what is this value again see the circuit I just now said VDD-this drop you are here at the drain please look at it really-this drop you are at this end down here and actually Vgd what they want to reach here.

You need a Vgd but if you say Vgs-VT equal to VDS I can get VD D which is VT is that clear so I can get this into VT+VT as I repeat if this is under saturation I am now saying okay that expression anyway I am showing you VC max-VT VDS okay at that point it is at the edge of saturation Vgs-VT=VDS is the edge of saturation so if I substitute this and that voltage must be equal to radius which is VDD-this this.

So if I is equal then then I get VC max is VDD T+VDD-is S/2 x RT is that correct this is the maximum input common mode possible what is the condition it is it will if you go beyond that this condition will get violated is that your device will enter which region linear region and then your whole linearity will be lost is that correct is that point clear.

So that condition which I put is the device should remain in saturation but the Maxima will come when it is at the edge of saturation is that correct so that is the condition now coming to the minimum side from where I should minimum from the south side or the minimum occurs says that VS which is the source voltage please remember source voltage is you just source well today yeah is current source are the current source of capital.

How do I make a current source if I use a transistor put a proper Vgs this and I will see to it that the current is constant here okay is that clear then it becomes a and what is the other property of a current source not that the only current is constant or source is close to infinite that is the condition of a good current source.

So that is your voltage drop across this transistor VDS of the current source so this vs is essentially VS-VSS is how much the VDS of the current source that name are given as v CM vicious what is VCS is the current source voltage drop current source now ideally what should be the voltage drop 0 okay, but it is not ideal.

So it should be some drop across the VDS which is the VDS of that transistor is the VCS number I gave you so the V VDS for the current source is VS-VSS please locate this is-or-that means this adds in fact is that correct VS-of actually that voltage is adding to that is tell it will do so the VC minimum band is okay first you remove this VT this it is this VG they forget.

This voltage you is taken what I am saying the minimum value is Vgs+Vgs is that correct is that clear this value +this value is the input is that correct so if I do that I adult VC minimum is Vgs+VCS my V says-V the is equal to-VC just now I wrote common source voltage VDS for that so we say and I added a VT and subtracted VD why did I do that just to make it some vo a term appearing there okay actually this VT.

You are not there but I just added and subtracted so I get VOV+VT+VCS+VSS okay if white is a-VSS, but it will become +y VSS is negative quantity so this is called VC minimum so what is the input common mode range then what is range called maximum-minimum is that correct what is the range max-min so we see max-VC min is the input common mode range.

What are the 2 conditions is satisfying one is device is at the age of saturate it would at best to the age of saturation for maximum input signal to allow in common mode okay and it goes to the minimum of that value when the current source is a constant current shows anything violated there will not allow that VDS to remain in saturation.

Which means the device will done it will not give a constant currently is that correct that means the bias point will shift away is that clear and therefore these are the two swings voltages in which common mode signals are possible to be amplified the current source will not act like a current source because that VDS will be then smaller than Vgs-VT for that current source the device will enters a linear mode.

So, it will act like a resistor there and very small resistor if it is larger this said there is no problem because it is still at constant current source it becomes smaller resistor that is the issue and then we will say CMR all will go to 10 dB okay that is what happens current source is not coming from somewhere else it is a part of the different picture and the way it will created I just show you how they are going to create that okay.

There will be a transistor sitting there okay is that okay, so having shown you so I CMR is VC match - we see min so your that is the range in which so many times when I design an open one

of the space they give me this is the ICMR okay this is the isomer, so I actually from there I know what values I have now value I can get out so that the ICMR is within the range given to me say they may give you -2, 2+2 or +3.

So, I must now work within this range so at no time the device W boils and the currents are use should go beyond these values to make device going out of this range is that clear that is something one has to design we take care of ICMR day one because that is the limit I always see ok.

The current source must remain current source that means it must saturate better then that is always because that ayah says if it comes out there between us as long as that current is constant that device is in saturation anyway even at the edge of this RSS is still flowing that will still access by 2 will still make M1 saturated but that as soon as this is condition that will automatically get satisfied we chose is s says that M1 M2 bridge satisfy.

How the current will make both saturated as long as you are under age you are still satisfying the upper condition anyway if you get out of bed that the current size does not remain same current or much smaller then it will come out of saturation anyway not only this the upper one will also and that is why I say we say input it will come out of it okay so device will not in the linear mode anyway is that okay to some extent, yes okay.

Then I have designed a current source I know that voltage what DVDs I am using okay is that clear this will be close to a VT okay so we say VT as we call it so we know that value yeah so best current source will be video is larger than that so at the edge it will be VD Vgs-VT is video so we say V T so let me to drop hair difference Vgs-VDS my third glass saturation per head that is the criteria.

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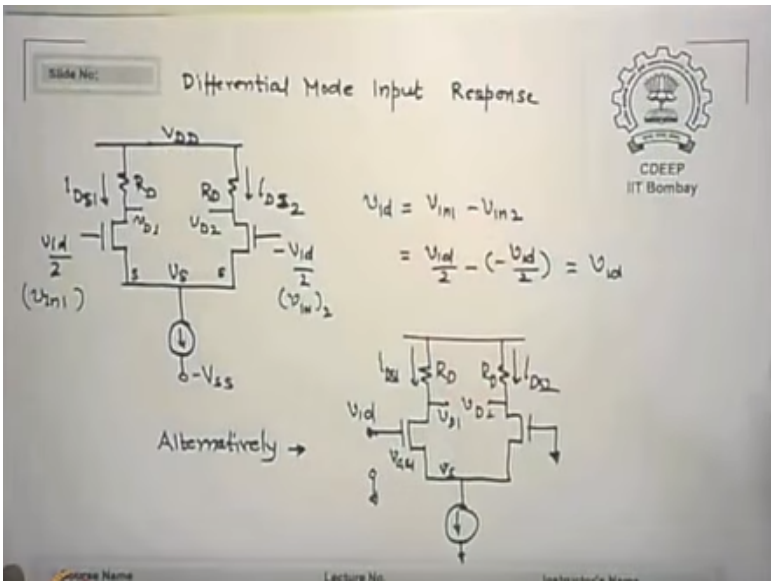

So, as I was killed for nothing it unsaturated a is that okay analog circuits are only 10 to 20% of any mixed signal chip which you used like wireless mobile or any other but if that 10 to 20% circuit does not work well if you are 80 to 90% digital will fail immediately because I is a push carnival I have object front an area all analog walks are at the front end if things go wrong at the other everything is out anyway so our power ask is cap which B.

So, neither fact ion is on either side so remember it is like saying this is the people who control everything in the world right now okay, so we are seen common load so let us look for the major very major interest for us is the difference mode common mode is very small we are only trying to reject common mode signals fine but if amplifier is not for rejection amplifier is for amplification.

So, let us see what amplifications we get and that is our major interest so we do the same define once again shown here if I say I have an different signal of Vin 1-V into that is our different signal to input signal cut difference to I have a different signal and V in 1-V into depending on if you know one is higher we had is +if in one is smaller we had is negative fair enough but otherwise difference is always there.

So, I am not game I say I apply a VID/2 here and I apply-VID by to the other side so how much is the difference signal VID is that clear so when I say VID alternately I can also assume that the

one of them is grounded and this input is VID so we already - 0 is still VID so there is a single input the other input this is what I is doing and why and show you is this okay.

We will collect that first circuit which I showed you in most cases this is grounded one of the terminal is grounded and you give input only at the other end this condition is exactly what I am showing one input is given here the other input is grounded so automatically input signal become different signals this is what you actually do in op amps equivalent I saying this is what we are doing in a defense is that correct.

I appreciate I agree with you anything you do yeah our cell half which voltage even a different signal Lin I Omega V idea irrespective whatever we do the DC biasing is not controlled by this this is biasing is only controlled through Isis so I am not worried about the status of m1 and m2 so I am only interested to see VO1-VO2 divided by Vin1-Vin I never said anything more than that you tell not as long as you take a different signal here.

How does it matter we are also breaking a difference of VO1-VO2 you but the point if you spec to whatever I will do here this will be different in two cases as you are saying but the difference should be will come same that is what we are trying to say this is what superposition is trying to say chili now okay you wait for this I will show you this is called when the superposition opossum this is called half circuit analysis circuit.

Which I shown you is called half circuit analysis and when this is valid will explain you when this is valid if this potential is constant this half circuit analysis is valid there is a theorem for it okay what your questioning can be proved at this writing equivalent of half by two is equivalent of saying VID and 0 that is all the difference in the output voltage will corresponding to the values here and here.

So,they change so is this change the difference will as long as you are in linear the difference will remain same independently that is exactly what I am saying what you are asking is what I am saying it will always this lower will change this this higher will change this the difference will be amateur saying one goes up the other goes down if this goes up this goes down.

So, difference is same as that condition I keep saying e well as long as you are in newer situation this will occur like this if this is going hard this will go load this is equal R equal 0 that is that will come like this is that here so our assumption is not if I say equal means what condition I am saying equal means common or low output is 0 is that point clear in polymer that is already there - yes VO1-VO2 is 0.

Otherwise, one is higher other is lower or other way depends on the sign is that clear so essentially we are saying this is always valid as long as this voltage is constant we will prove this point called half circuit analysis oh sorry everywhere please amount unless never ask me okay I am very sorry.

If I do not know anything you do not ask me unless I said it is single layer you show me every weld unit okay is that point clear what if the difference signal we are looking at what she is questioning is very good but she what I am saying any it do not get half-half, half-half then one of them will conduct heavily other will be smaller as they change you change the polarity still it will be oppositely it will okay.

So difference at the output will remain same independent way how input goes the more you put words so the output will shift correspond okay and condition is linearity is maintained okay okay bye now logic VRD=Vgs1-Vgs2 because source is common okay what is VID Vgs1-mean which is Vgs1-Vgs.

If VI is positive what does that mean if your pennies are now coming the answers are now coming if we always positive Vgs one is larger than Vgs- if you add is negative Vgs2 is larger than Vgs1 okay in the first case IDS1 will be larger than IDS- in the next case ideas- will be larger than IDs 1 just copy be current rock are Vgs-VT Cos square.

So the beach ever has larger Vgs will pull more current whichever other smaller videos will pull less current so it can also occur for a given value of v ID the other transistor may switch off is

that point if I change the ID this other is optimal at that so that becomes smaller and smaller so that ransom message of one of them all the current will be drawn by only one side is that clear.

If I change reality from say-to +one of the transistor may actually go draw start drawing higher and higher current the other will start reducing at a given via d the device the other side may become off all of the current will be picked up by the higher Vgs okay all of it that means when we yes to both less than VT that transistor will be switched off whichever Vgs goes less than VT that transistor will switch off than the one, which has larger the yes will draw all the current is that kind of clear all the current.

So, we may say whichever is fully on transistor it will draw all ID in the let us say in the case I will be was such that I just one is greater than Vgs - and we always increasing Vgs - is going down so in that case IDs to 0 and ids 1 is equal to I assess all the ISS is now flowing in that transistor is that ok all of it is going through one arm ok.

What is the condition I am using all the circuit please remember if I add lambda here 1+lambda VDS what will happen this equation will become nonlinear okay and then I will have to really do on the spice only and not analytically I am not adding those turns because otherwise solving numerically is the only possibility is that clear.

So in when the problem you will solve in the tutorial which I am now giving next time you with you first learn spice and then that time lambda need not be 0 in fact you do this analysis put lambda 0 and put lambda point 0 one or point 0 two and see what difference it give it will get relatively sufficient difference and that is one of ovaries also is that point clear if I change VID such that one Vgs1 start increasing Vgs too small then Vgs too may go below VT M.

To transform a switch off all m1 will drop will current I assess that all why say as I can open if I make reality - larger then we say M2 will take all the current and M 1 will become fished off this is yes okay. So, there will be some maximum minimum V ID in which one of the transistor will draw full current is that correct so let us wait for that expression one can see from here sorry a root on a cha here if we are the minimum becomes equal to-2 root Vgs Vgs-VT.

We may say the transistor let us say this is IDS1 and this is ideas - maybe I should write this this is IDS - oh sorry maybe ideas 1 this is idea sorry IDS. So, M- M - thanks on ok and in + m 1 turns on, so they also help so eight-0 say is diagram this is 0, where they will meet which point is s by 2 point though they will both we already by 2 and-VI D by 2 / both 3 K equal over time is that clear this ascension is saying except for these ranges currents are not linear is that correct currents are not linear except for the fringes.

So row here we - 2+root 2 VA we may here input signal AD VID then only amplification in linear models we are linearity is possible so the limit of input for even different signal is there is that point clear I am a conservator them in a common mode how many difference motor they will they are key in between these two only values there is a linearity and if chilling I should not come even closer to this why because if you punk later here.

There is no linearity so actually it should be less than that both side is that clear is that of aha at this where they are not linear so actually it should be away from the edge points what does that trying to tell you again small signal attitude against me do you get the point if reality becomes larger then what will happen only one transistor will operate and it will go into a saturation values either-or+is that clear.

To remain where transistor in linear system you should not exceed VID within this more than these two ranges what does that mean reality should be small values so again difference amplifiers can only amplify if input SC different signals are small enough is that correct so parallel bar my common mode can limit the are given a difference cupboard David Abby of you can write because I have not shown you properly this slope is very high.

What is the typical slope of this lines do you know it is the value of gains open-ended gains is 10 to power 4 and a bow so if you let us take a case I have one millivolt signal so how much will be output 10 volt is that correct 10 volt if I or a - one hour - 10 world but power supply the pasture party hair the best design is is that correct.

So, here one minimal different signal may not be a lot of the gains are very high in the open-ended system that means no feedbacks dominate the fan cannot do it larger different signals is that correct because the gains slope of these curves are very very sharp 10 to power 4 10 power 5 that is what we design in fact so the other thing the larger gain will help you.

In the case of which circuit reaches faster -+VD D or-VSS what is the circuit should we call fast comparator is that correct small change output when timidity or-VSS output immediately came to you came to know whether it is +or-so I compared the signal as fast as possible is that one clear if the slopes are very steep the gains are very high turns out that value gain requires a very small change at the ankle okay.

So, if I Serbian 1 is 0 are going to 0 and then one is what I am trying to say is this, which is interesting again you should know what I do in the normal case let us say this is my V in one and V in to is grounded so if my input is something like this AC signal as this crosses 0 let us say this 0 it will show-value if this crosses.

So, value instantaneously instant means finite time some nanosecond to may microseconds okay so faster the switch will occur when so even with a small change over a 0 it can show you an output going to one or 0 in some sense is that correct such are called fast comparators okay so Kara condition will give us comparator key they should have very high linear gains okay why high linear gains against cursor.

But, I think I am making a how do we increase the gates they found again 10 to power 4 5 case a cart a which may happen in the could beach may post a Scott again coachman ah cha here or skip followed a course stayed home they lock on against each okay Kevin do no milk every month or even there is a does not have a gain function buffer is only going either to 0 or to 1 that means drive higher side or lower side will show what is buffered.

Otherwise, this is how the gains will be very very high is that correct very very high and that is exactly where op amps are used in such analog to digital applications is that here why I am

showing all this because most of the circuit did I what did I say they will be digital your inputs may come in a lot.

So, I want to give them outputs okay yellow member that guy there were such circuits would be useful okay next time first thing we will do this we will first look into large signal operation what does that mean larger signals and then we will say what is the difficulty and I get a larger signal and then how much smaller signal I should get so that the thing which I said I will first we have our signal analysis and then we say okay what is it creating.

So, K reduce your signal to this value for good amplifiers is that okay so next time start with large signal amplifiers please start reading in to say address with which chapter I do not have there are they click on cell mass if it implements is a separate chapter or Bible I do not know I have not seen recently but maybe in the same maybe in the same just look for this two days work and we will start with last signal and finally.

We will kill you, defend that here will make up a room okay I saw it made anything,which may I said Mirabelle gamma you know Dana self solar for his course all could a welcome spoken to bus I saw school they have circuit analysis actually your point essentially it is a small V movies DC+AC to DC the fix T here member you what the point that oh we may owe we are capitals okay essentially saying it is AC+TC the DC value at the fixed year you.