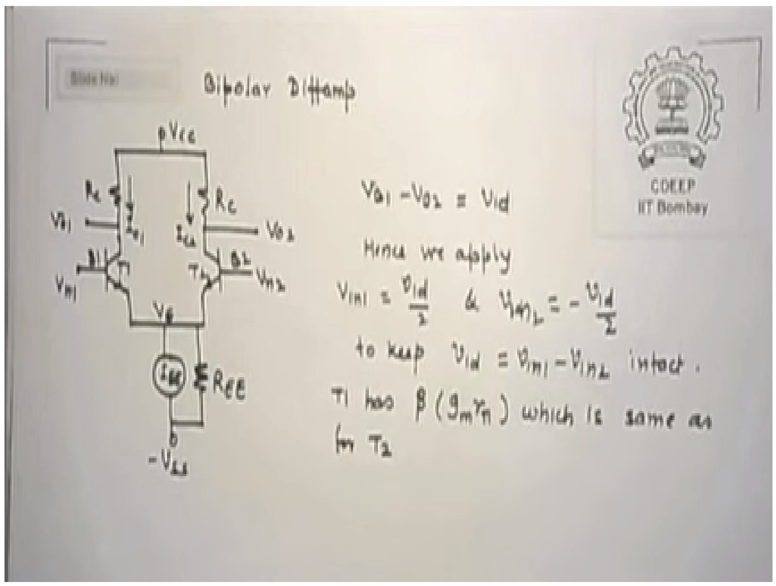
Analog Circuits

Prof. A N Chandorkar
Department of Electrical Engineering
Indian Institute of Technology Bombay

Lecture – 16
Differential Amplifier

(Refer Slide Time: 00:00:24)

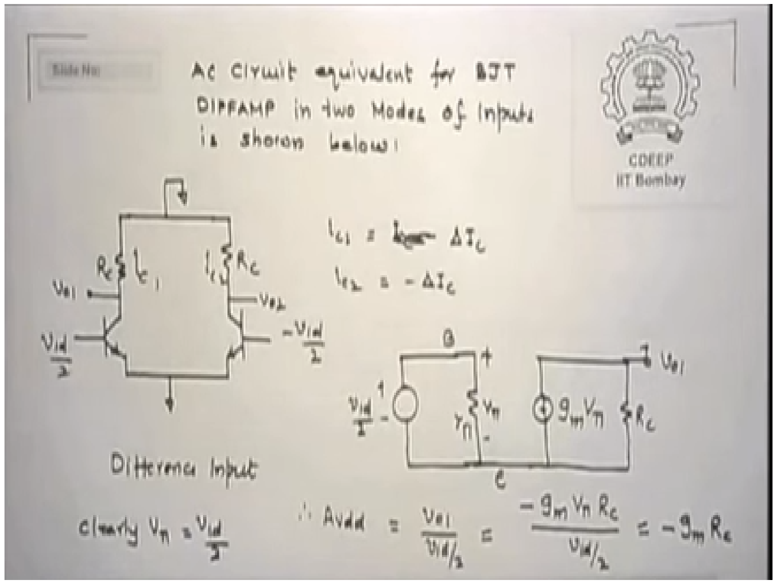


Last time we said, we did something about Moss diff amps. We will quickly, not do all of it but at least show you that similar diff amps can be made out of bipolar transistors and a typical bipolar biff amp is shown here. You have 2 bipolar and in pair transistors T1, T2. You have loads of RCs here, 2 inputs Vin1, Vin2, then the current source which is IEE shunted by its current source resistance REE.

That IC1 with the current in T1, IC2 is the current in T2 and for, will like to see that VB1-VB2 is equal to the difference signal and as usual, we will apply Vin1 is Vid/2 and Vin2 as -Vid/2. Now, let us say T1 has, T1 and T2 both have transistor gain, a current factor beta same for both, which we know it is equal to gm times R of R pi, okay.

Assuming T1, T2 are identical okay, you may find IC1 will become IC2, if signals are same, RCs are same and betas are same, but the only difference is, this DC currents may be same but if this is positive and this is negative, one current will increase and the other current will decrease because that is what the diff amp is. If one current increases because that voltage increases then the other current will decrease because the voltage there decreases from its DC value.

(Refer Slide Time: 00:02:17)



So if I use this simple analogy which I just now said, then an AC equivalent circuit of a BJT diff amp can be Vid/2-Vid, VO1 and VO2. You only calculate right now by symmetry half of the circuit, so we write VID/2 +- is, this our R pi. There are no capacitances used here this is the DC analysis or 0 frequency analysis. Small signal, I will not say zero, low frequency or mid band frequency analysis.

Let us say the voltage across R pi is V pi, then at the output between collector and this emitter, there is a gm V pi as the current source, shunted by RC. We forget right now about all parasitic resistances RE, RB, RS. They can be added and more complication of circuits, I mean more complicated expressions may start appearing. Since the difference input is Vid/2 and we are right now assuming there is no source resistance.

Then whatever is the voltage source you are applying is same as V pi that is V pi is Vin by Vid/2 and then we define the Avdd is VO1/Vid input signal which is gm V pi, RC upon Vid/2 which is essentially gm RC. Which is similar, like gm already in the case of MOS transistors, okay, so it is not very difficult to replicate whatever we do in the case of mass that we cannot do in the case of bipolar, this is per different signal gain.

We can also do common mode, what is the common mode signals will be? Both will have same voltage Vid/2, Vid/2 or Vid, Vid. Total is V common and if I do that analysis which you can read in the book , this is very I am just trying to show you what we are doing, if I apply Vid/2 Vid by both sides common mode and I divide this REE, you look at my diff amp. This REE if I divide into 2 parts, 2RE here and 2RE here parallel combination is still RE, okay.

So, if I do that then I find this circuit can be half circuit with 2 RE here and half circuit with 2 RE here, okay, and then we actually write equivalent circuit, V common voltage, this is your R pi, this is your 2 REE, gmVn by for one arm half circuit, gmv pi and this is your RC going into the ground and output this. Solving this circuit which is A common mode, AV common mode is VO1 divided by Vcm is -beta RC upon R pi+2RC this say, just solve this network, okay.

How much is VCM here in terms of V pi and something. The drop across 2 REE+V pi is the common mode voltage, is that correct, the circuit has to be understood. This is one loop and this is another loop, okay. So solve for the 2 loop equations and you get VO1/VCM is beta RC - of course, current is downwards R pi, 2REE beta + 1.

Let us say, beta is large enough, which will be around 100 plus, please do not confuse this beta, with beta in the moss transistor. There beta is essentially, beta - W/L. It is not here, here it is just, common emitter current gain. So if I say beta is larger than 1 and then REE times B is larger and this is roughly equal to RC/2REE, this is like emitter degenerated amplifier, is that correct? Emitter is degenerated by resistance of 2 REE.

So the gain is normally equal to RC upon 2 REE, is that clear? We are done this in any transistor, if there is a source or emitter is degenerated by resistance. The typical common emitter gain is load divided by the source resistance or the emitter resistance, is that correct, equivalent. Yes, for the change in this, one change would be + and the other changes - so RE, there is no current equivalent saying for AC signals, one change is +IC, Delta IC, that is – Delta IC.

So when they pass through RE they cancel. It is like R5, which we say no current goes, okay. Equivalently saying, is that okay? In the case of common node, both currents are passing through

REE, is that correct, in the case of difference, opposite currents pass, is that clear, and therefore we assume that they are equal, if they are simultaneous, the runs are identical and there is no current in REE, is that okay? Same, same logic which I described for RO5 in the case of MOS transistor is valid here as well, is that okay.

So if I write my common CMRR which is AVDD/AVCM and I write the expression, typically this expression appears to be 1+2gm REE, is that correct? If REE is infinite, assuming current source is ideal, then how much is CMRR? Infinite, but since REE is finite, there is a some kind of finite value of CMRR and this value may be typically as I said, 100 DB, 80 DB to 120 DB.

The REE values which a current source will give, will be such that gm times REE took 2 times gmRE, will be of order 20 log of that, if I get and it will be around 80 DB, 80 DB to 120 DB. Which will be higher when RE is higher or lower? When RE is higher, that is better current source, you will get higher CMRR, when you have a little bad current source, you will get lower CMRR.

What is the advantage of CMRR? Why we are interested in CMRR because we want the signal, actually, we are only calling it, there is a common mode and difference mode signals. In fact, we will only apply Vin so any noise if we supersede, superpose on these signals, then we say both end will get same noise and since common mode rejection is very high the noise will not get into the output and we will say, we will only get different signal outputs. That is the purpose of differential amps, is that clear to you, is that clear.

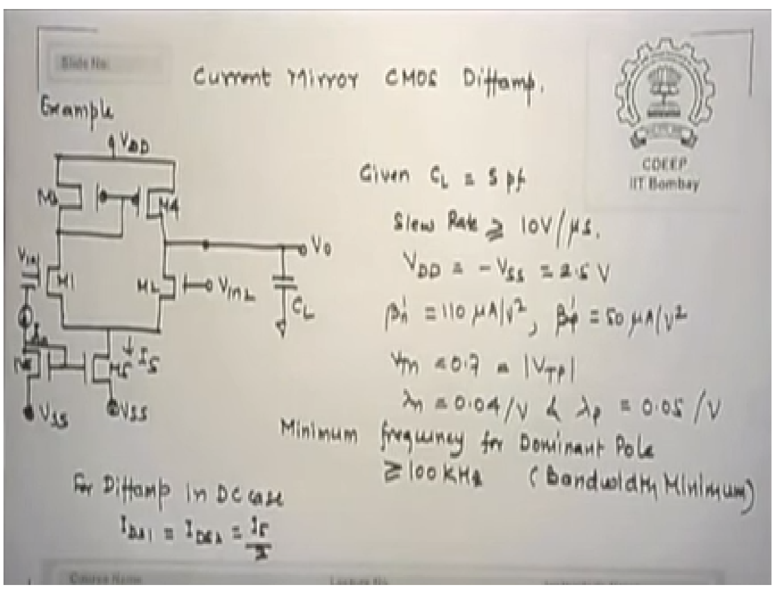
So we are always designing, of course CMRR is not a fixed quantity in design. I may choose CMRR, say 680 DB, 95 DB, 100 DB and typically get a current source value for which RE I will choose and then correspondingly I may design my current source, is that correct? So, it is not the inverse way, I put something and I first actually decide how much I should have, okay, 100 DB for this, I found RE for a given gmw by, or this beta is given and then I will find.

Okay, I should use the transistor here which makes a current source, which will give me typical RE of this value, is that correct? This is what we, everyone does, this is just a small, this, think of it normally. Of course here we have everything as an NPN transistor, but a good current source can be made out of a PNP transistor or a P channel transistor in mass, Y compared to n channel or ambience.

Think of it, if I only want a good current source, I will prefer a P channel device or a PNP device. Here of course I have one technology in which everything is NPN so I am using NPNs everywhere, but in case I have options, just to create a current source, I will prefer PNP and PMOS transistors over NPN and NMOS, is that clear? This is something as a designer we must know, if I want the current source, I look for P channel devices or PNP transistors, okay.

This is just to, I am not doing great detail of this, this is just to show the analysis which we did for moss, is similarly, can be done for any bipolar circuit and method is identical, in the sense, give an equivalent circuit of the 2 cases, whichever cases you are looking for and then solve the circuit and you will get both, all the parameters of your interest. I promised you last time, that I will solve a problem for same Moss current mirror based loads.

(Refer Slide Time: 00:11:29)



This is of course a design, actually designed dif amp in our lab, but I have just modified some values as well as what I did is, there since we were designing, in the case of design of a moss circuit, what do we actually design as a word? The size of transistors that is the design parameter, in my case I have whatever values I have actually got there.

I used them here and say what is the gain and what is this, inverse problem has been shown to you or simpler problem shown to you. In real life, you will be given some value of gains, value of this and find W/L, okay. So let us see a problem, which is simple and actually wants to tell you, what, how do we solve such problems. Here, a standard CMOS op amps with a current mirror loads.

Let us say, you have, this diff amp is driving a large capacitive load. Please remember, this five puff is a large load, why? Typical value, do you know how much is, CDB, CGD are what? .01 point kind of puffs they have, okay. Typical technologies, this is hundred times those values so this load is excessively higher compared to any other capacitances in the circuit, what does that mean essentially.

If I say, this capacitor that this node has a very large value compared to all other parasitic capacitances, what does essentially in response term, I am talking about. Let us say there are 3 more capacitances available to you, actually more than 3 are there, but at least 3 and this is the fourth one. So what does essentially I am talking to you and I say this capacitance is larger. How many poles it will give, say four capacitance will give me four poles.

Which will be dominating, the one with the CL because one upon RC, so, C is the largest there, so the dominant pole will come from CL itself, is that correct? So my assumption right now to tell you is that CL is governing the dominant pole and what is dominant pole in terms of frequency we say? What is dominant pole essentially tells, if I have a response it falls at certain frequency what does it tell? Bandwidth, it gives you bandwidth, is that correct.

So the bandwidth of this diff amp, loaded with heavy capacitance CL, will be decided by the CL itself, is that correct? Larger the CL, bandwidth will be smaller or higher? Larger loads, smaller, so this is an important parameter in thinking that, if the loads are higher, the bandwidth drops, is that correct, if the loads are higher, the bandwidth drops, okay.

That is why we keeps saying the values should not be too high to low because otherwise it will open or short wrongly, or at least we should forget the bandwidth of your choice, okay? There is another term last time I introduced to you, the output, depending on the input changing, the capacitor at this will charge or discharge. Charge through m4 discharge through M1, M2 or essentially saying, change at V0 or V0 going to a value of given inputs will take finite time, is that word clear.

Will take some finite time, what was the time it is associated with? The time constant associated with resistance of M to N M4, is that correct? The times will be associated with this Rs into this C, is that correct? So, we now want to, we are saying how fast the output responds, when the input is applied, is that word clear to you?

How fast the output comes after application of an input, is that correct? And this is defined by the word called slew rate, S-l-e-w r-a-t-e, and essentially slew rate is rate change of V0, DV0 by DT. What is slew rate? DV0 by DT, why I am talking our DV0 by DT, can you think what is the current in the capacitor will be I = CL DV/DT, is that correct.

So how fast this DV0/DT appears, is called slew rate, okay? So, someone has given me a specs that my diff amp should have a slew rate greater than 10 volt then volt per microsecond, per microsecond, is that clear, or 10 x 10 to power 6 volt per second, okay? I am given VDD 2.5 volt, VSS -2 and a half volts, I am given beta n- and beta P- at 110 and 50.

So what is the mobility ratio I assumed, 2.2, okay? So, that is the ratio I am assuming, of course this is the actual data from a actual cadence tool, so I am using their model files, okay. Let us say VTN and VTPs are same with 0.7 volt, okay. I am also missing, but we should not, you should not do, everywhere units must appear properly.

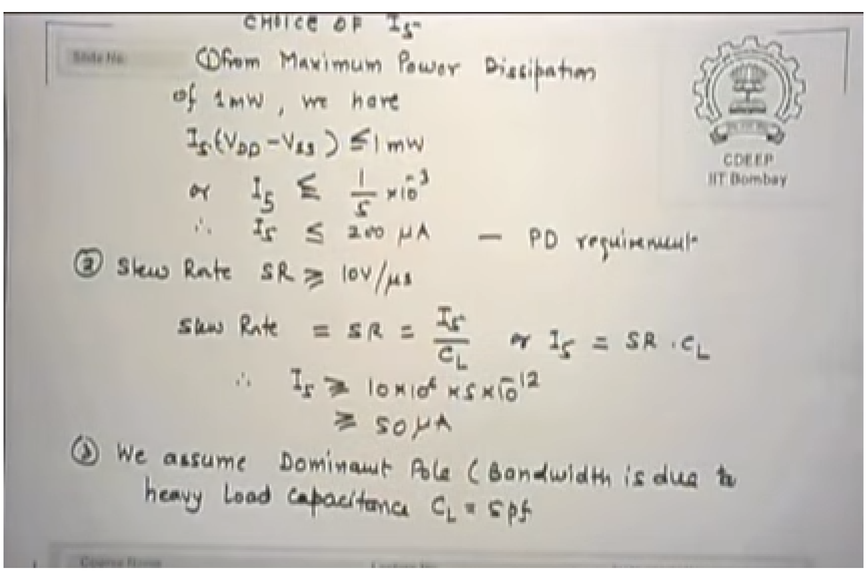
Let us say lambda N is 0.04 per volt and lambda P is 0.05 per volt. Can you think why I gave higher value to lambda P than this? Generally lambda maybe close to each other but P will have a higher lambda than, marginally higher than N channels, okay. Now we also, they said that the, at least the bandwidth I am expecting is 100 kilo Hertz, preferably more than 100 kilo Hertz. So is that what, designed clear to you?

They never say 100 kilos they say it should be greater than 100 kilo Hertz is that correct fluid should be also greater than 10 volt per micro Center minimum value expected is 10 volt per microsecond you get 1215 fine with this also satisfying fine is that good so that is the word design in analysis we do not do the greater than or some he said this is the value, so I want to ask as soon as I chosen this value from my design of a de femme and therefore some things.

I am using them something I am actually specifying now one can see the current DC current in M1 and M2 is IDs one IDs to its I 5/2 is that correct for the biasing okay for the biasing of a define half the current in the m1 half the current in M - now this is what something given to us I have not been given the value of I-5 and that is what first thing I must know how much is the I-5 but they have given me some more specifications.

Let us see why I chose this example of a design so you should appreciate that analysis helps you to design and therefore you must see design as your ultimate and look your theory to adjust to that here is something you will appreciate when I say there are three ways or three parameters which will decide myIi-5 value here are the three they are specified that the dissipation of this D fan should not exceed 1 milli volt okay.

(Refer Slide Time: 00:19:14)



What is the constraint they are given the net dissipation in the where is the dissipation occurs in transistors resistors are equivalent their resistor I square R loss is going on IxV is the power loss in the transistors is that clear to you so we will like to see if they say power dissipated is less than 1 milli watt then we say I 5 x VD maximum current is I 5 maximum voltage is VDD-VSS which is actually 5 that should be less than equal to 1 milli watt is that point clear.

I have they say 1 less than 1 milli watt okay so I can I need not get 1 milli but if I get six hundred micro watts fair enough 800 micro it is better or 600 is even better but whatever I make a choice they should also satisfy the other conditions of unit and the free bandwidth if they don not then I will say which one okay.

So let us say one value I got it from this that this I 5 current should be less than 200 microns is that correct which is that condition is coming from this 200 that the power dissipation should not exceed one milliwatt okay if that is so I take the second parameter for me first you read understand and then you.

Write first is I five has given me it should be less than 200 from the power distribution requirement the second basis new rate should exceed ten volt per microsecond slew rate I just now said you rate is I five by CAI 5 is the maximum current available either the last transistor will drive or sync so I have five is the net current available to you.

So I5 lease CL is DV0/DT which is your Stu rate from here we say I5 are into CL and therefore I am now saying I five should exceed CL is five hundred power minus twelve SR is 10 volt per microsecond so 10 into 10 to power 6 so I five should be greater than 50 microns is that correct to meet a slew rate requirement of 10 volt per microsecond I should at least have a current, which will be of the order of 50 micron band about okay.

There is a third parameter which is also governing D what is it governing the bandwidth okay because Pole will be also decided by gm please remember poles will be decided by genes gm is a function of I did you buy I5/2 so I will now like to see for given bandwidth how much is I5 is that correct is that particular first I say power dissipation I got some value say can I say slew rate I got somewhere I say okay.

I am seeing the third parameter even the GM term is function of I5 and they are saying me this is the bandwidth I should have let us say then I must get some value corresponding that is well, so I got the second value third value is that now point clear this is designed this is what part I am doing only partial design rest I will now substitute values but this is how we start designing we are given sweats and we must meet every one of them okay.

We must meet every one of them yes and that 10 you from the power supply to the ground the maximum current available to his I5 current source is that clear so when the capacitor is charging all of it going through CL when it is just shining all of it is coming through lower transistors essentially saying when the slew rate what is actually DV, but it is charging so the full current is made available for the charging full current is available for the discharge okay having done this I have been given the bandwidth as one upon okay.

Now I say I have already assumed you can actually find by Poul theory that this is the dominant pole why I assume this what is the why under what conditions and I shown this then the C else is at least 1 or 2 orders higher than all other capacitances and so is our okay and if that is so then 1 upon RC of this will be the smallest value and that will decide the bandwidth what is our out in this case D fan please look at our circuit of deferment.

What is our out here and the output what is our out ceiling RO of M2 parallel of arrow of M4 okay so if I do that then I get 1 upon go2+go4 to understand why I suddenly shift to go jeez addition is much easier than doing 1 upon R+1 upon R so I know this is what the tricks of the calculations nothing great in that okay.

How much is gsg output resistance of Fernet transistor lambda ID is that correct lambda ID is the G sorry this is – I am sorry but you can see the next line I are written I fight so this is the expression which we are derived and this is what we are substituting now so this is lambda n+

lambda T/5/2 if I calculate this is 22.2/I5 now they say bandwidth should be greater than 100 kilo Hertz.

So we say this should be greater and if I calculate now I five from this I get a value of 70 microns okay so I have now three values got how many values I got first I got 200 microns second I got 70 micron 50 micron and third I got 70 microns now what should be the choice I can make which will satisfy all of them it should be larger than 70 but smaller than 200 so for the heck of it.

I chose 100 you may chose 125 you may choose 150 is that clear you are right to choose those values because then these three conditions still will be satisfied but there is something else will occur and I will show you why that choice is not necessarily always correct you may have to boost this current further also okay, how much you can boost up to 200 okay, so we will see okay we just calculate for 100 and see what results.

We get and then we say our area boys are like 400 or 100k we are now given that I 5/250 micron W by L 1 is equal to W by this 18.4 value is not very good value in design, okay we will make it 20 in their life but calculation wise whatever I actually have got it I substituted back here.

So I am just to make clear for you other uses are up car division gala takes me I mean I exact value Joe Mary I here with the Kyoto so W by L 1 is equal to is 18.43 and 4=8 this data actually we will find in design is that clear in design what will we find these W buyers actually really value it for given specs right now I gave you this values and then I only calculate gains.

There I will be given gain now I am asking gains what is gain of a de femme Gian times are out is that correct gm1 or gm2 they are a same so gm1 or gm2 are out I substitute that gm is to be turned as W/L x 1 I5/2 divided by our alumni on plus lambda PI5/2 if I just divide this correctly by substituting these values I roughly get difference gain of 100 okay say in real life.

What they would have specified that the gain should be at least hundred and then reverse back to fine right now I give you that okay find the DC gain why I call DC difference again so notice the difference again because for this expression we derived for differential amplifier with difference inputs okay common not what is if the rod is very high we say we do not consider a V common mode right now.

In any case assuming it is to be so close to zero okay, so I have calculated these values gain what else I have to find now I do not know I have got everything I only want to know this transistor v which is giving the current source what is the condition I am going to apply on that it should be in saturation and it should have a corresponding re e which will make CMN are very high is that clear.

So that is some indirect condition in my mind okay, so I just want to see whether that can be guaranteed by me okay so I am now going back to my little analysis okay one more specs, which I have forgot to give you they will also give you input common mode range what does that mean the maximum and minimum inputs which this diff an into linear modes is called input common mode range.

1 will be minus 1 will be plus why it will be minus from minus VSS you will calculate is that correct and the upper one from VDD down you will calculate is that correct so one will be maximum from the VDD side minimum from the VSS side so I am okay I do not use it days there I am only saying okay Vic a minimum given to you is minus 1.5 millivolt what is the expression.

I wrote there please look at this expression this figure common mode range is calculated from here is that correct, so that V inseam is VD side drop across 5 okay + Vss Vss+this drop plus vgs is input this plus this is this this Plus this Plus this I repeat Vgs + drop across this plus potential here signs will take care okay is that correct this potential is this this and this that so if I use this expressions which I showed it will be VDsat +VSS+Vgs putting the correct signs VDsat 5 is 1-Vgs1 okay.

But Vgs1 is the current in what which transistor m1 is that clear Vgs1 is giving a current in M1 what is the current in M1 for a DC value of I5/2 I = beta/2Vgs-VT square is that correct so

Vgs=2I is that correct by beta my plus VT is that under root of that this is the expression I wrote is that correct it is what expression 2I upon beta or beta into w by l under root of that is that correct is the covariance.

So, Vgs1 is I by two half a beta and W/L please remember this is current is half why one transistor we draw half the current plus Vtn because the Vgs-VT+Vtn solve this and I get vgs one is 0.9 - 2 volts how much 0.92 2 so if I substitute back in VDsat what is the VDsat value for the fifth transistor 1 minus 0.9 - 2 which is 0.08 volts.

So VD saturation across the current source is point zero eight volt if VDsat is so smaller this is essentially Vgs-VT, so small and I is very large so what can quantity will have increased I repeat if the years minus VT is very small square term is very small even smaller current is larger and which term is will be increasing to my balance left and right Corbett and H is constant.

So on W by L is that point clear so now if I use this value of VDsat for the transistor 5 this is 4 5 if I substitute this value in this current equation for the transistor 5 and assume that is in saturation then I get W/L is equal to how much 300 in an integrated circuit such a large W/L will take huge area is that correct so how do I increase or decrease this W/AX this is designed this is what we will do.

So what do if I want to reduce this W/L by smaller value say 1 2015, what quantities you should see from there what should I do now this content is fixed for us now vdsat should increase if you say VDsat has to increase so if I increase BD sub we decide what should be the quantity here I should decrease increase this vgs1 should decrease sorry vgs1 should decrease if PGs one is to decrease what should I change there in the Vgs1 expressions I five is that correct.

So now is that point clear to you why I fight with a design parameter because if I want to change my W/L for five I have a choice still I fight with me is that clear, so I will increase that I fight further from say 100 to 125 let us say recalculate it back if this quantity has to reduce what is the gm what is the current is in this okay whichever side so if I have still 70 to 200 range.

So I should now start moving my i-5 whichever side you wish such that this W/L comes to around 50 or so on lower but then it should not still come out of any of the constraint of power bandwidth or this relates that is the design word is that what clear design means given aspect, so I did have designs for you given a specification I actually iterate okay.

I got some values and I start iterating okay this is giving too high so let us reduce that on this increase that I keep varying also please remember that slew rate which I chose is the 10 but maybe 12 I to some other this value will come, so we must adjust your values as long as your bars are met and get your I5, which will satisfy all three of them as well as satisfy sizes that correct they are all dependent on each other this is essentially called deform design.

This is essentially called a differential amplifier design is that clear to you now what design is clear that what why is called design I am varying to get my specs so you got the point there is some kind of a interrelationship I do this change something else changes if they change it come to third changes but I should remain within a bound which is given to me okay.

I am allowed to change but I should remain within the given bound of specs this is what we say designs is that clear so this problem is not the universal problem in the pan or something this was specifically when we did some years ago this one different design for my student, so I showed him exactly on price how this very varies rather tool so I told him that now think of it and how to adjust this value so when first time he comes.

I show something second time I do not go on system okay, now you know how to do so is that correct why I need to know theory because theory gives me where to start is that correct spot you must have seen spice you have to n parameters you can vary and outputs you will get is that correct so where do you start do you want to have convergence to come after 20 years after you all are already in estrogen a job with a big money.

You want to see just as fast as possible so your solution example I may give you which is very relevant in math and all of you have done this often if I have a solution F X versus X this is the solution if I start my initial guess Here I am iterating and after some years I give up okay I am not reached here but if I start here across immediately okay.

So, this initial guess has something to do with your thinking and that will come from where analytical because analytical values gives you where to start okay and the accurate values will come from actual semi actual models all parasitic everything there is that correct but essentially do some analytical analysis before going to system this word has to be understood by all electrical engineers that if you do otherwise solution will never converge okay is that clear.

So choice of your initial guess come from where some equivalent analysis you do then fix your values around that and let it read them and it will give fast results then you can design get it will test in time and it will be marketed in time that so please remember why I keep telling all this why analysis is so important in my opinion.

Otherwise you will keep doing analysis of this and it will never come with their design values okay 100 parameters to vary you know that temperature everything else will come and you keep doing let us go yoga or keep so some initial values should be correct so that you get the correct time outputs is that clear.

So learn analog circuit digital circuit whichever circuits you do for this purpose because at the end of the day application is very time she do that this finishes all that I wanted to say there are few more things left please read this Smith's a draw and me okay now we start today with a very important chapter or important topic which is not necessarily to only for us but it is true for every system in the world okay.

What is happening in Japan why those reactors are going growing one after the other the feedback is not working is that correct the feedback is not working that is the problem is that clear and that is why I say let us learn feedback a bit okay a typical feedback system is shown to you here typical in the sense I am not saying whether it is voltage or current or anything okay.

Actually, I need not ascend a also it should have been transfer function something HS or something okay we have a signal which is excess how many kinds of signal in electrical we can have excess either in the voltage or it can be current f0 is the output of a system X0 is the output of a system whether what can it be either it can be voltage or it can be current.

So how many combinations it gives for voltage input the output current input voltage output current input current output voltage current output so four possibilities are there so I make a generalized statement XS is the signal x0 is the output depending on in real life you can adjust either voltage source or current source or current input current of what are you let us say there is a gain function.

Which is written UN what is oil stand for open loop that means without feedback okay if the gain of the so-called amplifier or any transfer function is a well and they are also other functions of frequencies then what I did whatever I receive an output X0 I take it back and return it to input in some ratio okay this is called beta is essentially called feedback factor.

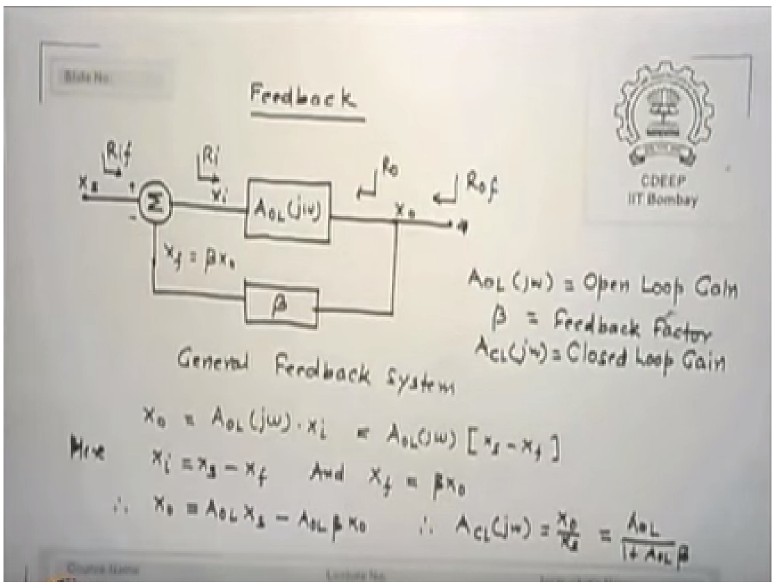
Please remember beta is normally about kind it will be able to frequency dependent or non frequency dependent non frequency difference should be passive network it should be a passive network typically such that it does not give too much of frequency responses however this diagram does not insist on it may be J Omega also beta J Omega also for us this is anyway irrespective all that is analytically.

Then solving becomes little tougher otherwise because you have to keep worrying about phases okay but right now assume beta is something constant but please remember this is not a condition we are taking it for simplicity a CL is again which we call when the feedback is applied X0/XS when the feedback is applied is called closed loop since it is a closed loop we say that gain as a CL is that correct with feedback the gain is a CL without feedback again is you an open loop and closed loop a typical feedback system shown here.

If I look for this expression F0 is now I have not seen actual sign here if it is - or + corresponding signs will also come right now it is more generalized a can be plus it can be minus so I am just putting some values but actual science will be taken care in actual decisions is that correct for a normal amplifier gain is positive or negative why if I using a source amplifier or follower.

So, do not always jump on it depending on the amplifier gain may have plus value or minus value so I am reusing plus but if it is minus put correct sign there okay so f0 here is a some kind of a summation given to you the part of feedback is such that the output of this feedback network is such that the output except which is coming here is some part of x0 so what should be the value of beta should be should we have limit what should be the value of beta should be less than or greater than less than 1.

(Refer Slide Time: 00:44:40)



Otherwise the return will be larger than the output then this will further either dam down completely or grow up completely depend on the science it gets ok so right now assume beta is less than 1, but that also is not a condition for generalized system I know see later we will see that it matches okay so in amplifier we say it should be less than 1 okay but in other case it is any Y1 it should be 1 or 1 greater than 1 possible is that clear.

So we are right now not saying whether B ties done but general amplifiers will have less than 1 what is the signal X I coming here XS and let us say the way it returns to you XS-X negative feedback it reduces the input signal summation is such this is signs are such a college should be plus it should be shown both plus then only it will subtract JV+ -A+- a sorry yeah then here - you are right.

So it should subtract basic idea is the signal is reduced by a feedback it reduces now what is the advantage of this kind of feedback we can immediately understand for some reason some reason the gain is not constant for some reason gain increases suddenly temperature is for example one of the case then what will increase X0 so what will be accept will be larger or smaller than earlier it will be larger.

So when it suspects from input what will be excited reduce now with that larger gain with lower input X 0 will come down let say a 0 goes lower down then this XF will be smaller so, X I will increase and a 0 whatever it is it earlier so this means after few iterations as if whatever happens X 0 will become on standard so is the greatest thing.

What this feedback is giving to as an amplifier is gain we made constant is that that is the otherwise other parameters will keep varying the gains I do not want gain to vary again I want constant is that correct why I am one gain constant because gain means the output voltage which is going to be input of the next stage or next whatever system if that keeps varying that will have also a problem okay.

So, we want to see that the gain does not change okay by using a feedback we cannot negative it well essentially we can always set the gain to a constant value however this creates a problem what is at the cost of what if you see XI which is XS-FFXF is be direct and if I substitute back here I do J Omega I will burn X0 is AOL XS-l btec 0 so, the closed loop gain is X0/XS which is AOL upon 1+U and if ever is negative.

It will get minus sign correspondingly a beta is the gain beta is less than 1 but a beta still can be larger than 1 because is very high beta may be 0.9 0.1 0.2 0.7 but still a beta can be larger than 1 so what will be ACL if a beta is larger al beta is larger than 1 what is the ACL value will be 1 upon beta 1 is neglected a will be does greater than one means AOL beta L/L beta means 1/beta but beta what did I say it is a passive constant value.

So what happened to the gain it became independent of the transistor parameters is that correct but what is the problem with a then beta is less than 1 the gain has Tottenham is that correct at the cost of lower downing of lowering the game we could stabilize the deal okay so that is what feed destroying hope it is always less than one who will use an amplifier is that clear so you cannot have a beta.

So higher than one that it would be only one upon beta so there will be a dependence of AOL also but that will be overweight by this denominator and therefore we may say the gain will become closer to a constant value and lesser than normal you will every time is that correct this is essentially the crux of feedback if on the contrary there is a positive feedback then what will happen to this term XS+x-l exiled by XS+ accept positive.

It adds to the input signal then what will happen to V0 XI will further enhance X0 will further enhance so what is the system going it is called growing system okay it will start growing towards infinity or saturate out so essentially then it will not remain in linear mode and you will lose the game factors is that correct so positive feedback is not needed or not desired.

What feedback we are interested will be negative feedbacks is that I am not saying we cannot have positive feedback we may have a combination which is what the oscillator does we make both positive negative such that they compensate every time okay so for a given frequency nothing changes that is what we will do so is that theory clear to you.

What is the feedback advantage feedback actually stabilizes the gain to a smaller value but it makes lesser dependent on device parameters or environmental parameters because we chose a passive network okay this is what is achievement of a feedback system now you think of it this can be any transfer function this can be any mechanical input this can be any mechanical output the system in UE control in there some system mechanical system you can have optical can have optical system.

So, any energy system can be created and feedback can still do the same job is that clear so it is not that electrical feedback is only relevant we are looking at because we are electrical people aro people will be using everyone will be using feedback very strongly because control is only through how much feedback are you ok and that is why control theory is very strongly depend on feedback theory.

Who are the best people which country has the best control people do you know no most of the control theory has come from not from Germany or India or anywhere way I see country Haskell normally live in Oscar Russia has the strongest control system people that is why with all this big very I mean trash looking systems they could put Sputnik earlier than us because their control was much far superior than Americans ok.

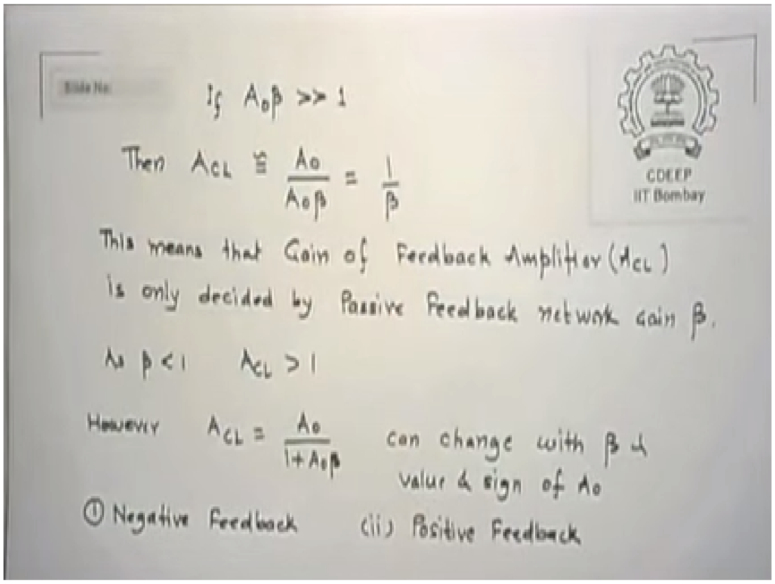
Let us continue in a normal feedback system which we will use open loop gain beta closed-loop gain and 1 plus a beta minus will accept them actually a beta is cobalt a return ratio it is cobalt a loop game since you may read books somewhere some may write return ratio some may write loop gains 1+A is essentially deciding how much is feedback returning ok.

That is the amount of feedback it is provided these are definitions open loop gain closed loop gain since output is part of the output is going to be fed to the input the circuit which allows you to take part out of it or pass on something output to this beta network this is called sampling what is it called sampling is that what layer output is sampled whether to return current or voltage in series or in parallel will see four of them that ok.

So it is called sampling at the input the actual input signal is mixed with this feedback signal so this area is called mixing so there will be on inputs and you have a mixed circuit mixing circuit at the output side you will have a sampling circuit is that were clear so on the output B sample at the input we mix ok.

Now depending on what many possibilities if it is a voltage okay and return is current then either one kind of mixing will happen ok current and current and voltage and voltage all 4 possibilities can happen in this mixing and sampling ok so let us see there are four possible circuits 2 here and 2 here and very interestingly we will see what do they mean this is true for any I just now said all of it I just repeat if the a beta is larger it is only function of beta therefore constant whatever I said is this ok.

(Refer Slide Time: 00:55:01)



Why are we so much worried in the analog circuits or circuits per se negative feedback properties so the first term as just now I said the gain reduces as we said due to negative feedback and this word we say gain D sensitivity it is called what is D sensitivity now what is this word D sensitivity is shown here the closed loop gain is a 0 upon 1 plus please remember right now A0 is not given any sign okay in real circuits.

I will start putting - + is that clear right now I am putting generalized so you must have some last time plus D are be generalized so if I differentiate this with reference to a 0 so DACL is DA0 upon via terminal wide or term a numerator correct denominator differentially so we say if I is that ok differential 1 upon a 0 beta due to a 0 and 1 is -0 bit on the square due to the other term if I subtract this value I get DA0 upon 1+A0 beta square.

So if I define what is sensitivity analysis means the change in that value to its original is that what clear what is sensitivity change in X with 3 or DX by X what is the change with reference to its original value that is sensitivity I really want on 0 no we see how much it is so DACL/ACL is zero this upon I define divided by ACL on both sides so I get 1 upon a0 beta DA0/AO.

I just divided DACL/CL both sides is I divide on both sides this is the expression this is 1 upon ACL then this this cancels this this cancels so I get DA0/A0 multiplied by 1 upon H0 DM in the sentence name without WABCO DA0/A0 is sensitivity of what function open loop gain function discuss Institute echidna let us say it is higher okay.

Then what will happen because there is a denominator term which is higher what will happen to closed loop gained in sensitivity it will be lower and we say ideal it should be 0 so by adjusting this values we actually have reduced variation in the gains those loop gains so we actually desensitized it is that correct is that what these sensitivity is clear that we actually do are very sensitive so if it was very sensitive here.

This got desensitized okay so first advantage of feedback is desensitization okay or D sensitivity so clearly we say percentage change in a CL is always less than percentage change in A0 and therefore 1 upon 1 plus a 0 beta is also called D sensitivity factor that term will be always in denominator greater than 1 so obviously change in A0 will be much less because that factor is in denominator okay.

This is something we achieved that either coach open-loop my problem her I they so close look unless a problem come could be another is that clear that is the first advantage which negative feedback will provide for an amplifier concept a bandwidth let us say you have a bandwidth is decider of each pole dominant pole separated the what do you expect will the bandwidth increase or decrease gain combine with agreed it.

It should come yes I forgot with me otherwise gain bandwidth is gain gum the bandwidth bunny honest so how does it here is one which is essentially saying bandwidth enhancement what is the first thing we did desensitize the gains now second is let us say you have a dominant pole at Omega 0 which is bandwidth related so a mid ban upon 1 plus Omega is open loop gain we call this a M upon 1 +0.

This is our standard a 0 term in the expression which used this is now please remember there are no frequency terms now it is first time I introduced frequency terms so a upon 1 + Omega 0 is a 0 Omega R 0 is your dominant pole or bandwidth pole related to bandwidth, so having A0 a function and I say 0 upon 1+A0 beta H0K M upon 1+ A beta.

So what I got EAM upon divided by 1+S you know 1+M into same expression all that I replace a 0/M upon 1+S by omega0 I collected the terms and I got a CL 0 which I defined as a map on 1 plus y this word 0 is coming M is fixed or not what is am wit band gain constant and I see a mid band gain a open loop me or feedback 1+AM beta, but M is constant beta is constant, so the mid band gain under closed loop is a CL 0 what is mid band value become a 0.

We call 0 no there so it is a CL0, so a CL0 is a m-- upon 1+ A beta and the denominator, I avoid 1 upon s times or division Maya 1 plus M beta times Omega 0 is that point clear mathematics where ACM Els upon a OLS Vita AOL is M upon month yes of stewed Chiappa terms collection and then M upon 1 plus M beta/S upon 1+M beta Omega 0+1.

If we define this numerator as a CL 0 then it is a CLS is a CL 0 1 plus s upon 1 plus a beta times Omega 0 the Polka having a Vita is higher than 1 is that clear whose Co multiplied by Omega 0 beta times the original bandwidth became the new bandwidth is that correct so feedback circuit disadvantage the gain reduced for that photo squared one does, additionally with me is Roger URI gain bandwidth constant Peter company.

So I repeat what I said the gain is open loop closed loop gain is M upon 1+0 is in beta and the new pole is omega 0 1 beta which is your new bandwidth frequency because this is larger than 1 so Omega F becomes much larger than Omega zero so we same bandwidth extension is C is that point clear to you what 2 things I said today.

What I said by feeling any feedback I will reduce the gain ka CL is less than you but if I do that I will get an advantage that the bandwidth will go a beta times 1 plus a beta times A beta times Omega 0 will be new bandwidth so gain the frequency bandwidth count I gain come here the bandwidth version bode plot mechanic hang up may throw a bode plot calculator again once again.

I have been any kind of yes I am your open-loop gain either carbonate econ, yeah I say yeah papaya La Puente Omega C this is open-loop normal amplifier a feedback here or let us say a beta is 10 for the sake of simplicity the other word it value can lead us clear so bandwidth town is heavy it decayed again x, so let us say this is 11 Omega 0 yet the a line many Hooper acid rock earlier be a VM air our second poll.

They dominant pole the gain cannot keep non reduce one which is with x somewhere we exactly to make Amazon, but somewhere here sorry so game Guerra times Messiah bandwidth Guerra times are getting away is that clear this is exactly what will show you this may a call conditions of young on the face skinning like I will face good garbage car Gaia the wolf will be we will discuss that word what we call stability you mean lose stability but in this case I am Telling it will not.

So is that correct this border plot correct well again shift okay again each other the bandwidth of so it is an advantage me the temple why do want to do this because bandwidth to improve okay what important but he said advantage or a second again desensitized are we a parameter dependency come car beyond this is that correct joke is Cassatt the open Ichiro sector hibiscus hardly a reduction.

They say some quake advantage surely a constant Gator of other additional I do not tell music mill they have very bandwidth birthday but maple a inane aircraft I was not looking for this I was only interested the gain became constant which I achieved but in cotton a byproduct buy a product asana o'clock give me a favor me on you I got higher bandwidth so a feedback it is not interesting hey about such ok.

Why we are so worried about feedback is or why we study so much feedback systems your head controllable Hornets a word is controllable so what do we actually change for control the feedback you know how much feedback we should provide so that the system becomes controllable within the range is that clear.

So any system you choose please remember this has nothing to do with electrical Percy ok we will only look electrical every time but otherwise feedback systems have nothing to do with electrical input outputs if greater or less go here is essentially feedback is that clear so conditional is a big push outputs later here that must come through some feedbacks is that clear next time you.

I will start with something more about desensitization of our linearization this is very important for us yeah once for all Medicare or a word what I am talking in future is this ok, I have signal excess excise the input to the amplifier and XF is feedback signal x0 is the output and then what is being mixed and what is being sampled if all three of them XS x voltages and x0 is also a voltage then the amplifier must be mixing voltage in series and sampling must be shunt kind which will be current.

We will see later, I repeat we will have voltage mixing in series and current being sampled actually voltage being sampled converted to come and see this like now you only write down so this amplifier when the all three inputs are voltages and output is also voltage and mixing is what we call series shunt and sampling is shunt these amplifiers are called series shunt amplifiers first is series shunt okay.

First yet you know voltage of the voltage heck mixing series their outputs are sampling yes / 8x qualm going a series shunt amplifier, yeah the XS x I XF voltages a but output currents and then we will say mixing since is going to be at the voltage then it is called series did that collect series by same logic if the inputs are currents and currents but they may outputs are current or voltage it will be called shunt series.

So, we will have 4 possible amplifiers do not do all of them in our we do at least 2 up to 4, I will show you that similar thing can be done for the other is that correct that will finish feedback for normal amplifiers see you.