Analog Circuits
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Lecture-19
OPAMP Circuits

We were looking for the all these days the difference amplifier. We have looked into the response, we also looked into feedback.

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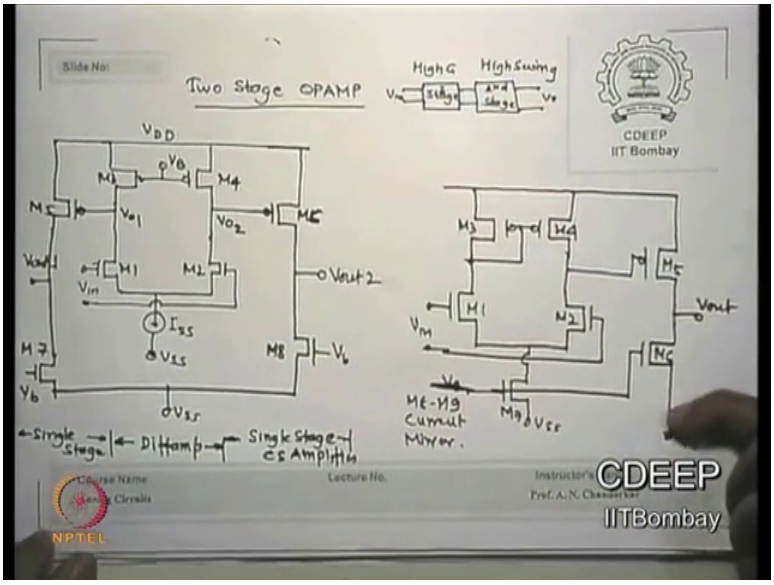

The first and the foremost circuit in a second which is available in market for use of amplification is called operational amplifier. And typical circuit which shown here it of course the normal OPAMP has three stages but in designing we also have what we call two stage OPAMP. Essentially a two stage OPAMP, is OPAMP without buffers or the output circuits. So, there are two stages the first stage of course is the very high gain stage because of the DPAMP.

Followed by a high swing little e lower gain stage which is the second stage of the OPAMP and third of course is the buffer stage which drives the output, typical number of transistors required to create a OPAMP is typically 22 may extend a bit here there up to 30. So, it is not a small one transistor circuit it has a large number of transistors. Even for 2 stage OPAMP the number of transistors shown to you here of course.

The transistor related to ISS has not been shown which may be more than 2 that is 3, 1 coming from mirrors for example so you keep adding such to understand you find as many as 30 transistors or at least 22 transistors are required to create an operational amplifier. The two stages essentially say you have a DPAMP. There are two kinds of two OPAMP one is the two outputs VO1, VO2 the other is C this is called double ended output.

And the second part which is shown here on the right is called single ended two stage OPAMP. Single ended means output is only one way out okay now one can see from here of course there can be different loads okay it can be mirror loads or it can be constant current sources shown here different loads can be given to define as we did earlier. So, there is nothing big about that right now I assume they are current sources with a;

Whenever there is a current source what is the output resistance of that transistor always R0 okay. In which case it is not R0 or R0 parallel something. Like diode connections shown in the next stage and it will be G1 upon gm parallel R0's okay. Whenever there is a diode connection we have proved n times that whenever there is a diode connections you will get 1 upon gm shunting R0 and essentially it may be 1 upon gm itself okay.

So, here is, as I say the output of the first DPAMP are two outputs of a DPAMP are given to a two amplifiers one on the left one on the right. What kind of amplifier do you see this; this is a p-channel device, so input is p-channel input. Device is not in channel which is receiving input okay and what is the load for that for example for M5, M7 is acting like a load which can be a current mirror load or any other load which you can create them, is that clear.

Now this means which kind of amplifier it will be single stage, source is here so where common source amplifier, this is the normal common source amplifier with P driver is that correct with P drivers not much different between analysis of n channel drivers or p channel drivers is that correct. In CMOS normally what we to do, we have M channel drivers with a p channel loads here we have a p channel driver width M channel loads okay.

So, whatever gain of DPAMP see VO1 will be proportional to Vin's okay which is then given to the input of the next common source stage which will have some gain A2 okay. So, what will be the net gain at the VO2 or VO1? The out one way out if A1 is the gain of DPAMP and A2 is the gain of the output stages then the net gain is A1 into A2 that is what we essentially do in a to stay OPAMP. So, will this gain be then much higher what is typically gain of a DPAMP do you expect.

What is typical gain of a different gm times RO1 parallel RO2 or RO3 parallel RO4 others are typically order of mega ohms is that typically order of mega ohms, gm's will be order of at least 10 to power -3 or mine in between -3 -4 ampere volts okay. So, typical value will get gains of around 1000 or 5000 kind of things can be achieved through only DPAMP, is that correct. The gain suffered DPAMP can be as high as 10 to power 4 okay or even higher sometimes.

Depending on the gm values you choose RO is value on what these depend on gm and RO's both it is depend on the ISS is that correct. So, choose your is to get the possible gain values. Now once you decide that DPAMP has this much gain and you are another gain stage which may have again gm times parallel RO of this okay and you are just the if the currents are same for all the transistors one can still get some amount of gains maybe 10 to 200.

So, typical OPAMP may have a gain of how much 10 to power 4 to 10 to power 5 typical OPAMP will have a gain stage gain outputs of the order of 10 to power 4 or 10 to power 5 okay maybe in best design maybe even higher but it may have some other problems if we gain too much gains on that so is that point clear. So, OPAMP's are no different from amplifiers which we already designed, already seen how they are solved okay.

This is the second part of this circuit is, this is called single ended output and what kind of loads we are using here mirror loads okay, mirror loads ISS bias current, 2 beta dash WVL into IS is under root of that is gm 1 upon lambda LS is IS of that. So, one can evaluate what gm remember is increase and is decrease will have opposite effect on gm and RO. So, you may get reasonable again if you still want I will make sizes double increase W by L okay.

That is the way gains are adjusted okay. I will give explanation I have returned on those expressions but before this I just thought what I am doing I showed you this is my standard DPAMP with the current mirror loads. This is my input between one and two terminals is my vein. This may be coming from the current source this maybe you are standard M5 or M7 number earlier we gave and this is your common source output stage okay.

Please remember again this has a P channel device which is receiving signal output of the first DPAMP is given as the input to the common source amplifier with P channel drivers and N channel loads N channel loads. So, if we now calculate here are some expression which you do not have to think too much.

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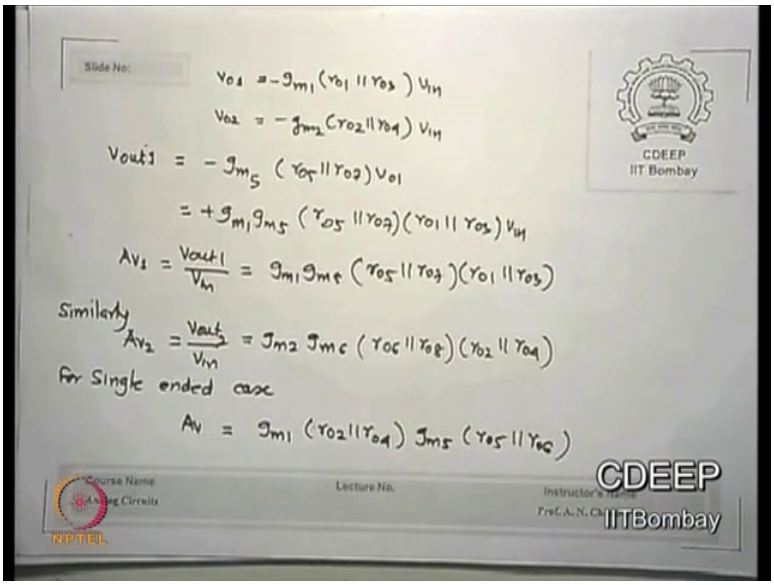

I just wrote down without you were seeing for the DPAMP for this DPAMP first VO1 and VO2 will be gm1, ro1 parallel RO3 into Vin VO2 will be - gm2 ro2 parallel ro2 into Vin if gm's are equal all those are equal there will be correspondingly gm ro terms will appear. Then what V out, V is out is the output of V out 1 is the output of Vo1 as the input and that is gm of I into RO is parallel combination of 5 and 7.

So, that is what I did gm of 5 ro5 into ro7 parallel ro7 into Vo 1 substitute Vo1 from here, so you get gm 1 gm 5 r05 ro7 parallel ro7 ro1 parallel ro3 into Vin, so the gain is V out 1 by and by same it will be V out it should be same gm's are same you have V out by V in, so these are the

two voltage gains. Please remember gm's are getting multiplied, so are ro's are getting multiplied so essentially A1, A2 the two gains we are multiplying is that correct, they seem to want this into this and this into this is A1, A2 is that clear;

gm5 into this is A2 gain gm1 into r1 parallel ro3 is the A1 gain, so A1 into A2 is the net gain of it 2 stage OPAMP is that clear. First stage of DPAMP as against trade of AM A1 which is gm1 r1 parallel ro3 the second stage have again gm5 into ro5 ro7, so that is multiplied to the first stage gain. So, a1 into a2 is A final is that okay. So, without even evaluating all of it as we did equivalent in a circuit we can directly write this explain.

Why, how can we write this directly because we have derived all of them individually every case. So, in future we do not have to keep deriving everything we say okay for this, this is what it is. But to; if someone said derive AB initio, please go back write equivalent circuit and solve for all of it okay. But generally I mean for solving these we do not need that. In the case of signal and then what will change nothing much will change gm5 ro5 just look at this.

The output will be gm5 times parallel combination of 5 and ro is of 5 and 6 and into whatever output coming here which is nothing but same as what we did earlier gm1 into ro2 parallel ro4 into gm2 are still the same only thing is it is single ended on the one side. And what is the advantage there, advantage there that everything can be mirrored now from everywhere. We do not have to put any current sources directly is that correct.

Because mirror why I say mirrors are easier to create because once you create a mirror source, current source we can always mirror any number of places. How do I pass on that gate of that should go to the gate of that with a diode connection on the one side? So, it will just replicate the currents the next stage and if you change the size you can increase the double or triple or any number of amount of current can be pushed to the other side.

So it is much easier to control the currents and therefore the outputs by just using the good current source as mine, once current source I create and that I mirror everywhere wherever I want additional currents is that clear. Now the only thing is if P channel mirror has to be what

should I do? I last time I had given example this; from N channel first you have to go to P channel the output of a second stage should be a P channel load mirror which then can be connected to the next P channels is that point clear to you.

There was an example given to you, first clear the N channel mirror then the second part transistors this output or drain should be taken to the drain of P channel which is mirrored to the next stage by again connecting source and drain and gain keep then going to P channels and if you want back N channel what do you do? Bring that to the next in stage at the output mirror it again for the N.

So, how do we go from N to P transferred, P to N transfers so any number of times any stages I can keep transferring the current to N channel to P channel which may be ratio of W by L which I can create is that clear. That is the trick which we all follow so we do not actually use current sources normally. Why we do not do it because internally putting another bias is difficult you know VV you said.

Normally what how do we get that current source I need some biased potentials here this may not be same as VV, in that case I may have to put too many voltage sources inside that means connection from the pin so many pin connections should get in for putting voltage of current sources creation. So, we normally put one VDD, create a current source okay and then replicate everywhere whatever bias currents you need, is that clear to you.

This is a trick we follow because otherwise on a board we do not mind for supplies no power supply (FL); but in shape what is the importance of a cheap compared to board what I said? So, many transistors I want to put in a smaller area that is the integration I am looking if I put additional voltage line somewhere I will have to leave some space for it that means I am not using that space for transistor.

So, the trick in entire circuit is avoid any extra lines if you, can if you do not I mean if you need it you have nothing else can be done is that clear. So, this is just to give it out why I normally use current sources and not so much normally current mirror loads are this is just with it. But in

reality on a board I can put all kinds of loads resistive loads current source darkening. I can connect physically anything and get any outputs.

So, the theory were shown to you what purpose what are the advantages, disadvantage of any kinds and if it is a discrete device you can use most of it okay. But in into a circuit the first major thing we do is to avoid areas giving not doing any silica or any transistor there. If transistor area is taken by something else I forget it that is what IC's are slightly different from normal discrete transistor circuits.

No difference basically in performance only thing why do we some things okay. So, yes; no but on the like in this case I want the current to be taken from somewhere where from I get P channel currents. So, the gate of this must come from a P channel site. If I want a current on this we fixed by me, let us say I want, so this P channel gate cannot be connected to n channel gates. So, they must be connected to P channel gates.

Now P channel gate must be mirroring from other P channel device whose drain current must be the drain current of N channel mirror okay. So, you come from you create only N channel mirror but pass on to P channel on the top and then move to P channel. When you want again n channel come down create to N channel driver go back. Keep doing any number of times (FL) is that clear (FL) okay.

So, this essentially what I was trying to say I may not do details about this OPAMP basic entire internal circuit.

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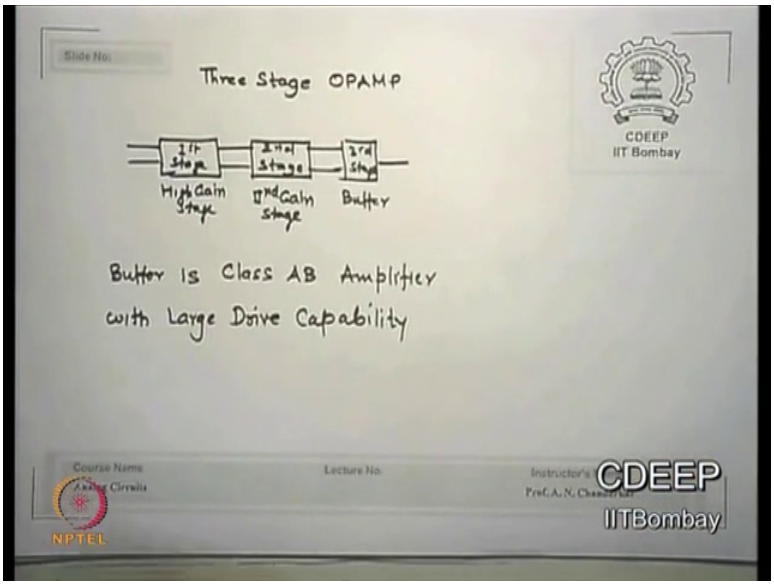

As I said the three stage OPAMP which is the real OPAMP has the gain stage, the single so a common source gain stage, a high gain stage on associate stage followed by another circuit which is called buffer which is essentially for large driving of the output loads. To drive larger loads we need larger currents and since we need larger current buffers are ones which provide larger currents is that correct, buffer provides;

If you want larger current what will be their W bias of transistors for larger currents larger or smaller if I want larger current, on the cell sizes should be larger or smaller? Larger, larger W by L and larger current will that lead to smaller output resistance of that transistor 1 upon I is that clear. So, the larger the current r0 becomes smaller is that point clear. So, all OPAMP have very low output resistance because of the buffer stages we keep there, okay.

However if you look at the input resistance can you tell me the input resistance of this OPAMP is higher or lower either of them. Please look it there is the gate connection which is insulated from source drain. So, the input resistance of a MOS transistor is practically infinite but at least 10 to the power 100's of mega ohms or at least tens of mega ohms above, is that clear. That takes a bipolar transistor will still be ri will be higher.

Their base collector can base emitter junction is connected there. So, it is still higher you have to be very relatively high, why the resistance of sources which will be Re, Ree or whatever we call

that is emitter resistor how much impedance it will see and then input side on the base beta +1 times Re, Re itself is 10 to power 5 or 6 okay, so 100 times that so in either case open has large input resistances is that point clear.

Whether it is bipolar or MOS intrinsically gives because a MOS, but even in bipolar because of Ree your input resistance is extremely high and that is the property of OPAMP, what is the property of a OPAMP? The input resistance of a OPAMP is very, very high output resistance relatively is very small it is not Ro of the transistor it is the output resistance seen is very low compared to any other resistor on the chip is that clear.

This is the feature of an OPAMP, what is the feature of a OPAMP? Large gains, large input resistance and small output resistance is that correct this is the property of a OPAMP okay. Just for the heck of it there is OPAMP which is also is an OPAMP but it is not called OPAMP is called operational transistor and transconductance amplifier called OTA (FL). So, there is an operational transconductance amplifier are very popularly named as OTA okay.

So, please remember OTA's are normally used in what we call GNC filters GN means transconductance C is the capacitance. These are continuous filters which are called; what is continuous? What is the other kind of filters could be digital filters which are not continuous filters. So, GNC filters are essentially continuous analog filters which can be created by a few capacitances and an OTA okay. We will see that little later.

So, is the issue clear what is the advantage of OPAMP over normal amplifiers. Normal amplifiers unless is the emitter follower is input impedance is very low how much as well as few kilo ohms okay HIV HIV or re is hardly Qi by kt okay so that resistance is KT by QI. So, that is very small so few kilo ohms okay and now few kilo ohms is not what we are looking for okay. So, normal amplifier to OPAMP is first thing we achieved is very, very high input resistance.

And comparatively much lower output resistance is that clear that is the feature and the gain is very, very high and 10 to power 4 or 10 to power 5 will be though. The only thing is this gain

should be called open loop gain what does that mean? No feedback is right now available so from output input there is no feedback connections. So, the open loop gain is 10 to power 4 5 may be higher than 5 sometimes is that clear.

These are the features which we are looking into a operational amplifier okay. Some of the characteristics which you all have them in the lab hopefully I will just list them.

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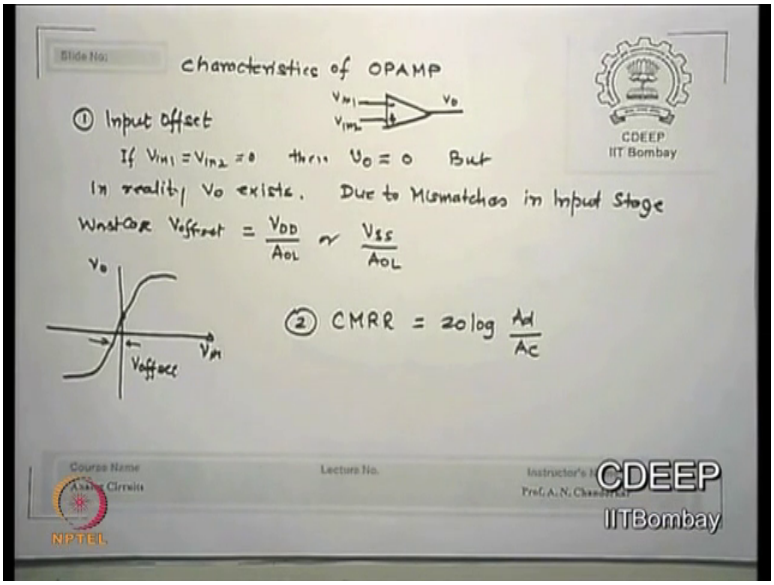

The few things which is of interest in knowing the characteristic of OPAMP is the first and the foremost worry is the input offset voltage. Now what is the time we are talking so if you are an OPAMP may be which is a symbolized something like this + - V in1 and V in2 being given names being this. So, if you have V in1 and V in2 this is V0 we say in DPAMP first stage, if both inputs are 0 output should be 0 because no current output should be 0 is that clear.

And output of an open is if gm is 0 output is 0 currents are 0 there. But if we actually see input 0o and still we see some output. In real life what happens that we thought that when Vin1 and is made Vin2 = 0 output should have gone to 0, but in real life if I monitor even if I say some voltage at the output okay that means the V0 Vin characteristics is something like this even when the Vin is 0 here, there is an output voltage is that correct there is an output voltage.

So, that the difference between when the Vin is 0 sorry V out is 0 to where V in is 0 this difference is called input offset voltage. Where should have been normally it should have cross 0 it should have crossed from 0. It did not cross it crossed on the left so it required it when I went to V in I found some outputs okay. Now this occurs essentially we say this occurs because of the mid mismatch of the transistors okay.

There contact only mismatches there can be size mismatch, there can be what else sizes W&L mismatch what else can VT scan mismatch okay. So, if there are mismatches in the two transistors m1 and m2 or m3 and m4 then ideally we were expecting difference between them to be 0 which may not occur because one of them is not giving same outputs is that correct. So, there is some finite output potential you may see.

So, how do I get rid of that let us say it is + and - if there is a offset here I should put in this or this plus arm some opposite offset voltage here which will actually cancel the other terminal offset on them is that clear. Let us say offset is +10 millivolts. So, I apply - 10 millivolt at the main inputs for 10 - 10 is 0, so, always see in your OPAMP there is additional terminal given to you for offset cancellations.

All that we do to put it is this resistive network with a power supply and keep varying that part. So, that offset goes to our output goes to 0 is that correct. V + you put a divider and change the voltage or change the resistance okay see that when V0 goes to output is 0 we say offset is canceled but in real life offset may be present of course will not look into this there are two kinds of offset which can be two kinds.

Any random this is one of them can be random offset okay the other can be systematic offsets. So, it is much easier to cancel systematic offset because what does I am trying to say, every time it moves there I will actually put - there as if it comes to 0 okay but sometimes goes there and sometimes was there order I do so random offset which is essentially noise related they cannot be cancelled but systematic offsets can always be cancelled is that correct, is that point clear.

So, one problem which you can see why should this the worst case offset could be VDD by the gain or VSS by up the gain because that is the highest voltage do you know output divided by gain is the input. So, the + or - offset could be achieved the highest will be VDD will be maximum output of VSS – V0 really maximum lower side in output, so divided by the gain is the possible maximum offsets possible is that correct.

This is the maximum possible outputs it can swing divided by gain will be the maximum minimum offset voltages; cannot be because output cannot rise beyond VDD. So, VDD by AOL is the highest offset you can get whatever reasons. Because you are now a saturated there is no AOL beyond that AOL does not exist in fact AOL is 0 then. Once we need a rich AOL does not exist at this point there is no gain okay.

So, the maximum possible is VDD or VSS okay the second term of interest; second worry of all of us is to get CMRR as high as possible which is 20 log any difference gained by common mode gain. If your mismatch occurs which is the first call which will also need to CMRR because then a CM will not be 0 but will be some finite quantity that is gm's are not equal actually if you see the term it is gm1 - gm2 occurs so they are equal so it becomes 0.

If they are not equal then there will be a finite quantity will occur and ACM will be present then CMRR will be there which is typically what is the minimum CMRR I suggested you 80 DB there are OPAMP's, I think some of the 725, 723 or these OPAMP's have a CMRR of 70 DB but they are not gaining something else. Look at that some sheets and you see why they reduce the same error okay

All seven for once are always greater than 80 DB and typically the higher stuff I06 8506 will have a CMRR of around 120 DB. Interesting parameter for is power dissipation please remember last time when I calculate there may be some this, I did not show you correctly power dissipation is something like this VD - VA says the maximum voltage available to you is that correct. So, when the current goes from here to VSS the maximum voltage swing is VDD – VSS.

But there are too many currents flowing one is of course this other is because of this then there is a major currents okay. All vertical branches cannot going from VDD to VSS are paralleled is that correct we need to the ground, we need to do ground will so add all those currents because they are supplied by same VDD and received at the same VSS. So, the power dissipation of an OPAMP's is all vertical path currents multiplied by VDD - VSS that is the power dissipation of an OPAMP is that point clear.

Current in this path current in this path or this together in this part this part and mirror what or any other hardware which like buffer output tool Brown. Any current path going from power supply to the ground that current should be added to all other currents parallely going through because they are drawn from the same power supply these two same VSS. So VDD - VSS this is + of course because it will add - of – VSS.

So, let us say 2.5 – 2.5 means 54 multiplied by the net currents is the power dissipation of the OPAMP circuit is that correct.

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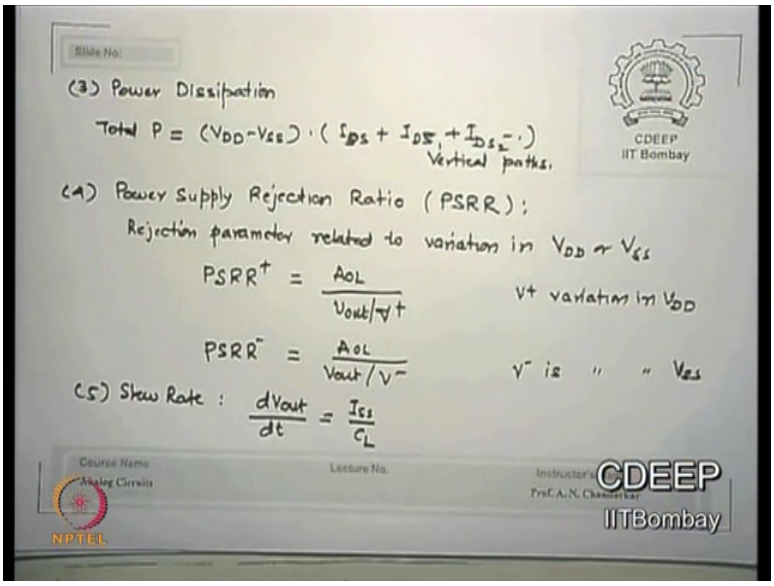

The fourth quantity of interest is called PSRR, now this is also very important there is lot of research can be done on this but let us see only are there characteristic now. This is one of the major design parameters for OPAMP but right now we will not look too into this. Let us say the VDD and VSS are not constant which can occur, why it can occur do you know why VDD may

not remain VDD 5 volts or 2 and half words it may become 2.5 + - something same way VSS can become + - something okay.

Essentially says some noises are reading on them and we know VDD will decide the current or VSS will decide the current DC currents. So, what it will change them all AC parameters are affected by the DC currents bias currents is that correct, gm is proportional to root I lambda 1 upon lambda i's Ro. So, you see any parameter any DC thing change the AC parameters are varying therefore gains may be, is that correct.

So, we want how much should be how much we should tolerate the variation in power supplies this so that gain remains within the acceptable limits. Why we say acceptable limits, let us say I am getting a gain of thousand. So, I say if it is 995 dozen does not matter 1005 it does not matter but let us say IO gain of 10, Then I cannot say gain of 5 and 15 are same as 10, is that clear. So, the amount of tolerance at the gain stage well outputs again you are looking for within a gain the variation in power supplies be allowed, is that correct.

As long as you have within that you may say it is fine okay this is called; so what we are expecting how much is that tolerance allowed so that the output stage gain is not very much vary acceptable limit. So, we define AOL is the open loop gain divided by V out + V + because of this ratio whatever is the change occurring is decided by power supply Ro + by + because it is on the VDD by same logic PSRR - is AOL divided.

You can see what I what is this essentially I am talking variation in output due to variation in VDD or VSS these values are essentially called power supply the; how do you really remove this much of the PSRR problems you are done is already the lab experiment on this. If I want to see that VDD does not change very much but it may officially I do not want it but may occur then how do I remove that what do I do at the output?

You must have seen and if you are not simply seen it now, this is your immediately terminal I actually put a capacitor there is that correct, which filters out those frequency components which changes the VDD is that correct have you seen any time or you are never connected all power

supplies should be connected through a bypass capacitors to minimize the variation in VDD and VSS which will improve your PSRR values okay is that clear.

So, we do not really do good things in VSS outside internally but internally we can do a lot of things. But for external people all such thing you have a choice to put a capacitor. But what is the problem with capacitor because it is only some frequency it will remove is that correct. Because no pass filter, so it will cut some of them okay. Depends on different frequency which you are going to get you may require n capacitor which will be very difficult to look.

So, it is not that so 50 Hertz certainly ohm which is called will be easily removed okay maybe 100 Hertz can be removed kilowatts can but if it is a mega noise nothing cannot you pass, in fact okay. So, that is the problem in; so, PSRR is not just for these it can also for any other noise and therefore internally we do design to improve PSRR is that correct. So, main thing that a capacitors (FL) okay. Now the next value for us which we already discuss is the slew rate.

hat is the slew rate definition we give last time that how fast the output response to input okay, so it is dV by dT is the rise of output to its maximum value which is essentially I said last time it is Iss divided by the load capacitance okay. So, this is also, last time I already given an example and we showing one of the way the current Iss is fixed is requirement from slew rate, requirement from power and requirement from the gain.

So, all three should somehow get matched to everyone's requirement. So, this is essentially there are few more characteristics but these are essential characteristics which all must be knowing prior to we start working on OPAMP in a lab okay.

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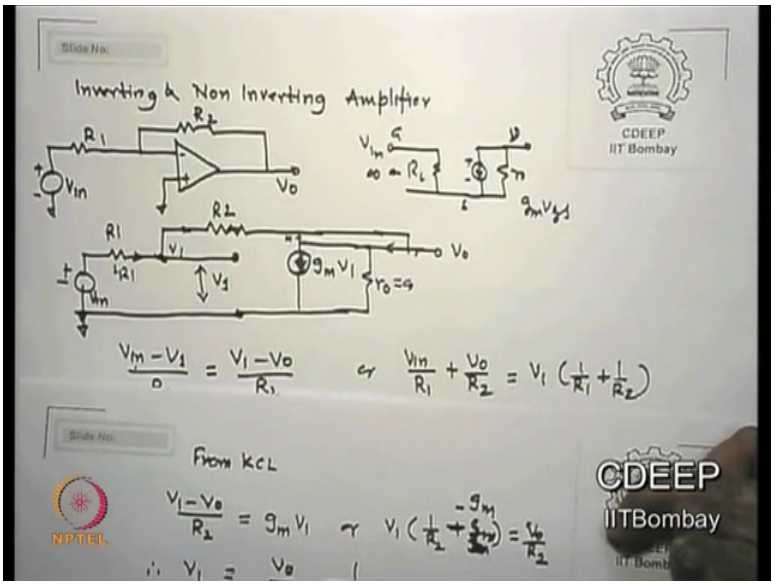

Now here is something the first day we have you know of course this is but just to get to what he has taught and little differently from what he has taught. You know why I say because I always want to show you little different from what others showed me okay. Here is something what others; this is a OPAMP where my ideal assumptions are Ri are very high because of this is that basically I am looking for MOSFET DPAMP MOSFET OPAMP.

There is an input source with has an R1 as the series resistance there, from the; I define for OPAMP two terminals one called inverting terminal the other is called non inverting terminal. It has nothing to do with - and + per se the idea is if I put input here the output gets inverted to the input. If I put input here output does not get inverted and therefore this names are given - and + okay. They are essentially Vin1 and Vin2 of DPAMP okay.

In most non inverting amplifier inverting or not this is inverting amplifier the V + terminal is grounded okay which means V in now occurs between V - and V + okay. So, here is the ground from the V – terminal, I connected resistance R2. I will not solve this problem directly but can you think which kind of feedback circuit is this, output code is (FL) what does that mean, what is being sampled? Voltage has been sampled.

So, what is the kind of voltage sampling? Shunt sampling is that correct. At this node what is being summed up essentially, currents so, what is the sample error mixing shunt mixing. So, this

is shunt-shunt amplifier is that correct (FL) is that okay this is the trick I do not want to show you but I thought you should see it is a feedback circuit sitting right here okay. This is no connection (FL) okay. So, equivalent circuit after this is equivalent circuit of OPAMP is something like this Ri a current source if you wish across there is a resistance R0 this is Ri is tends to infinity.

In case of Vg's, in case of MOS transistors this is gmvgs this source this current going down this is your drain, this is your gate source it is an equivalent of that is that correct. So, we are say gm V1 which is vgs for us = gm V1 shunted by r0 which is the output resistance of the amplifier and a feedback resistance of R2 connecting between gate and drain equivalent leasing. So, if I solve this V in - V this is V1 voltage V in - V1 by R1 is this current IR1 is that correct.

There is no current here, so where can current go only in R2. So, this current R2 is essentially V1 - V0 divided by R2, so V1 - V0 by R2, so V in 1 by R1 + V0 by R2 is Vi sorry V in, V1 sorry V1 upon R1 + 1 upon R2, is that correct (FL) because there is no current here okay. So, whatever current is coming must be going through R2, So, IR2 must be same as IR1 because what is the condition I put RI is infinite.

If there is a finite RI some current can flow then we may have to do little more calculations okay. From the case here you can see from here this equivalent the current V1 - V0 is going we're assuming R0 right now is infinite for the sake of simplicity where this current will be going what is that equivalent current, current gmV1(FL) is that correct.

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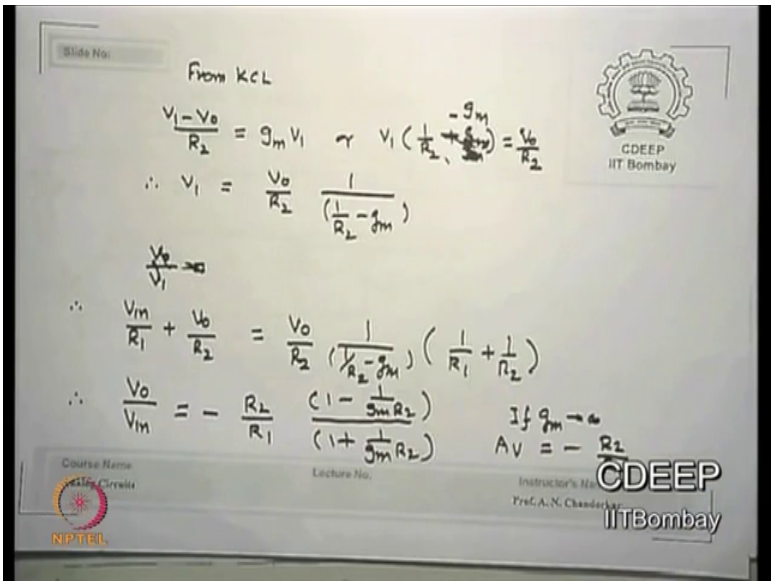

So, gmV1 must be sorry gmV1 must be = V1 - V0 by R2, so I will collect V1 terms V1 is into 1 upon R2 - gm sorry this cancel - gm = V0 by R2 from here I calculate V1 why I am showing all this I am trying to prove that that gain larger gain requirement (FL). So, the V1 is V0 by R2 1 upon R2 – gm (FL). So, if I substitute Vm by R1 + V0 by R2 (FL) V1 term a into 1 upon R1 + 1 upon R2 start collecting terms so, I get V0 by Vin is - R2 by R1 or you do you may have a denominator phase (FL)sorry 1 - 1 upon gm R2 + 1 divided by 1 + 1 upon gm.

We normally say in open the voltage gain is - R2 by R1 that is what we have been telling people again. But I have now derive the expression which is actually this R2 gain is this explained when this is equal to this only when gm is tending to infinity is that current, tending to infinity. What does that gm tending to infinity means what is the gain we are; which gain we are talking tending to infinity, open loop gain.

So, if the open loop gain is very, very high then gm times that value will be very high gm's will be very high and if that is very high these two terms can be one by one and then the gain is R2 by R1, so the condition under which this output voltage by input voltage is - R2 by R1 only exist if AL is very, very high and what is the AL I tell you typically of OPAMP stage 10 to power 5 that correct 10 to power 5.

Since the AL is very, very high we can then assume that the output voltage is just - R2 by R1 times the input voltage. I will show you without doing this also we solve the circuit and we get it. But actually this is bare analysis which we should look under what condition I can assume that R2 by R1 is the gain function okay. This is very important in understanding not that this is always the valid in the case of OPAMPS okay.

But to prove that my case is correct I showed you this is how I explained that things will happen ultimately okay.

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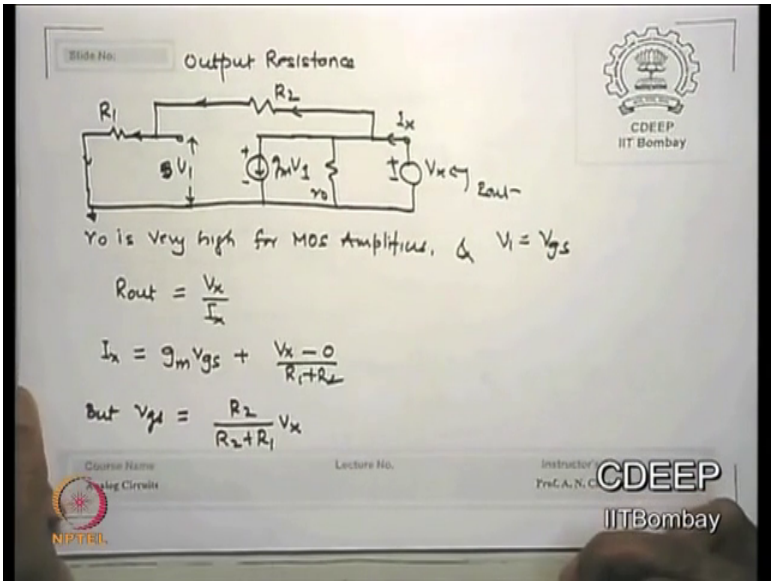

Here is another parameter of interest to us is the output resistance (FL) how they calculate output resistance of a network short input at the output applies voltage source and the current starting from their VX by IX is the output resistance this is my R out okay. So, also (FL) is that okay. The current IX and again I will as of now I will say r0 is very high and I am neglecting current through r0 okay. I can put everything there circuit; (FL)

Where the IX current is divided into one part is this and one part is this, is that correct (FL). So, IXis gm vgs okay and V1 is vgs as I just now said so IX is gm vgs + VX please remember VX - 0 y20 (FL).so, Vx - 0 divided by R1 + R2 the resistance here series me a voltage - a voltage divided by the resistance. So, VX - 0 upon R1 + R2 is this current gm vgs is this current so IX is

gm v gs VX - 0 R1 + R2 is that okay (FL). Some of those two currents, from here I will calculate vgs value which is R2 upon R1 + R2 times X.

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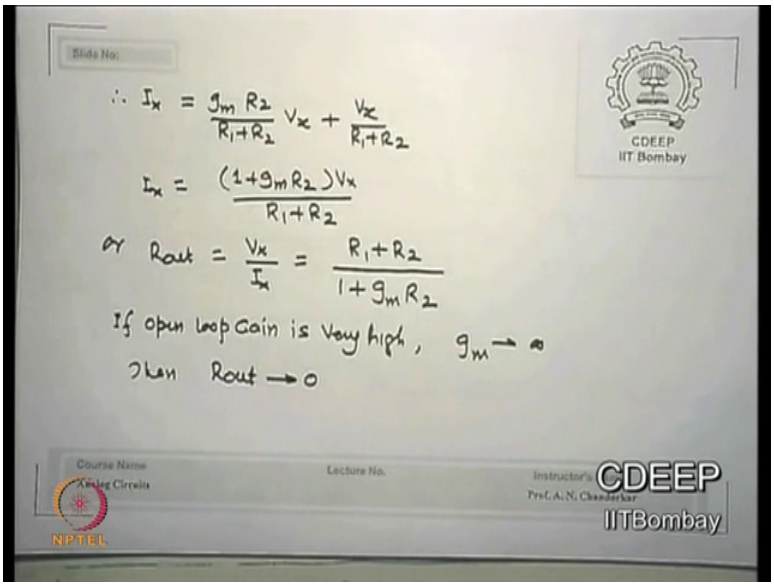

So, I saw IX I get a X and from there I can get VX by IX, so essentially what I am saying that will be also R1 I will come back to correct values but just see what value on see R1 + R2 upon 1 + gm R2 is the expression I got for R out is that correct, from substituting I get VX and IX relationship so I find out that. From here, what is that you are again seeing that the output resistance if the open loop gain is very high?

If gm is infinite how much is Rout, if gm is infinite how much is the value of Rout, 0. So, large okay the accurate value may come but in the divider will always come 1 + gm R, if gm is infinity or very high then the R out will keep going lower and lower values is that corrective is that clear. If the gain open loop gain is very high gm's are very high R out will keep falling as the gain increases is that correct.

So, one of the requirement of OPAMP's what that the R out should be very low. Ri very high although they said will be (FL) okay Ri is high, R out is low and how much is the gain I am talking very large open loop gains is that correct. So, by connecting OPAMP in the networks the way I have connected which is a negative feedback connection I am insuring you that open loop gain is higher if then the output resistance is low.

And input resistance is high is that correct this is essentially accurate value you can still get it the point yes. Other than saying that I must somehow guarantee to you is much higher open loop gains okay I think this is not correct okay.

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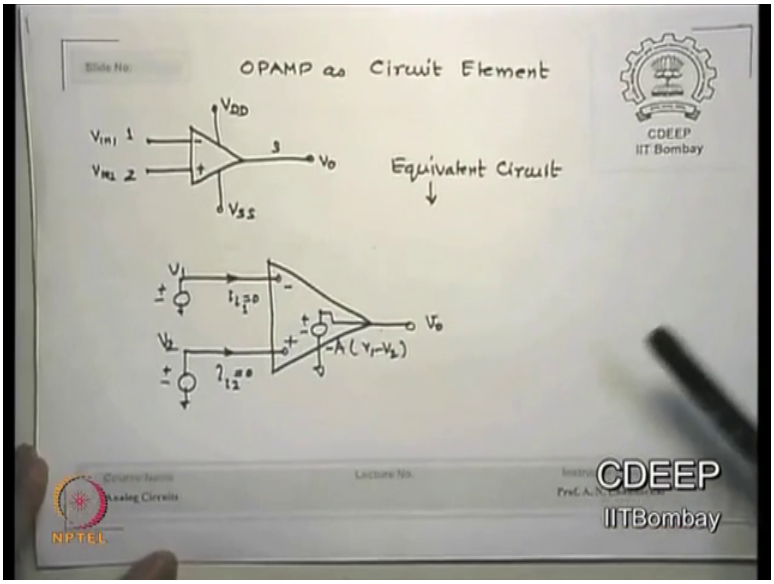

Now once I say then I can watch his equivalent circuit very easily. Please remember how what is the equivalent circuit I am now seeing. A typical OPAMP I am now saying if there is my input voltage I say there is no current inside - terminal why do I say so or no current in the V+ terminal. Why do I say so? I can say so okay I will come back to it. This is my input no current entering OPAMP at the output there is a voltage source which is V1 - V2 times – A.

And what is this A? open loop gain please remember this is DPAMP state followed by a single stage followed by before - Al V1 - V2 is your V0 is that correct I am assuming R0 very low and I am sure removing it. In voltage sources where R0 will appear in a voltage source where resistance appears, series or parallel? Series since that R in, R out is 0 or very small this resistance is treated as 0.

So, this is my output terminal the voltage which is appearing in the output is - AOL times V1 - V2 all that I said no current enters - or + terminals okay. Now we will prove this why did I say so?

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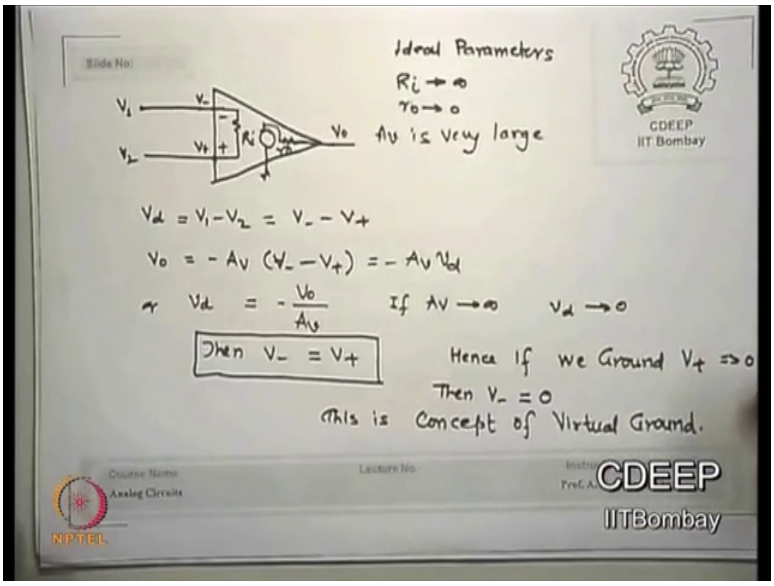

If you see this amplifier once okay let us do this first if you do this if Ri is infinity what does infinity means essentially open circuit. But really there is nothing called infinity so that means there will be a very large resistance connection between this and this is that correct. So, how much will be current V - V + divided by R, what is the current in this Ri, V1 - V2 by Ri is the current in I Ri is that correct.

Current in this, this voltage - this voltage divided by the resistance in this, if Ri is very, very high how much is Ii IRi extremely small or less than nano ants less than nano ants is that clear to you. If that is very, very small we may say or practically 0, we may say this potential must be equal to this potential. When the current does not flow, what is the potential at the 2 and half any resistor say that is why we say no current.

So, we may say now if this difference potential is V - V + the output is AV - V + which is Vd and if Ri is very large, no current flows through this means V - must be = V +, I repeat is that clear, why V- is V+ because if we declare that Ri is very, very high no current flows okay practically no that means the voltage difference between V- and V+ must be extremely small close to 0. So, we say V- must be = V+ that is why OPAMP we keep saying V- is same as V+.

We can see the same thing little differently again we have a V- V+ separate into Av is the output is that correct that just now from this circuit Av into Vd is the output. So, Vd is a V0 by Av is that correct or V – V+ = V0 by Av, if Av tends to infinity, how much is Vd, Vd tends to 0. So, V-, - of V +s tends to 0, so V- =V+ either away if you look at it why this is either a timing because in deriving this circuit I or shown are infinite anyway that is why I derived this okay.

So, it is not two different things but it is a saying is saying both ways you see V- will be = V+ in an OPAMP circuit provided the open loop gain is extremely high and therefore how much gain you expect at least should have 10 to the power 4 and above or preferably 10 to power 5 and above that is the reason. Now let us say if our ground the V+ terminal I have physically ground this terminal.

Then according to me the potential at V- is how much what is the definition of a ground if the currents sinks at that potential then it is ground sinks, current must sink there (FL). So, we say this physically grounded there is a potential 0 (FL) however in the OPAMP we said there is no really current flowing at V- however these potentials are same because we say V+ is V-, V+ are physically grounded.

So, V- has a 0 potential but there is no current sinking there is that correct. I say V+ is V-, V+ I made it 0 were physically by grounding. So, V- I am saying has a potential 0 okay. However that does not allow current to get in we said it actually which means they the pretension is 0 no current sink is going on is that correct. Such a ground is called virtual ground is that correct. Why it is called virtual because current does not sink there is that clear to you, current does not sync there.

Otherwise it is ground but it is not a actual ground it is virtual ground the difference is clear to you difference between actual ground and virtual ground the potential is 0, once syncs the current other does not sync the current is that correct. Their potentials are same there this is very interesting and that makes OPAMP circuit solving easiest because once I make V+ 0 this terminal immediately I say at 0 potential is that clear.

Once I make it 0 potential this current, this current to solve that becomes extremely simple is that correct. So, this fact that the virtual block exists only then DPAMP has very high open loop gain and the input resistance is close to infinity; under these conditions we say OPAMP can say V- can be created as virtual ground. Now here is a case which I must tell you what happens.

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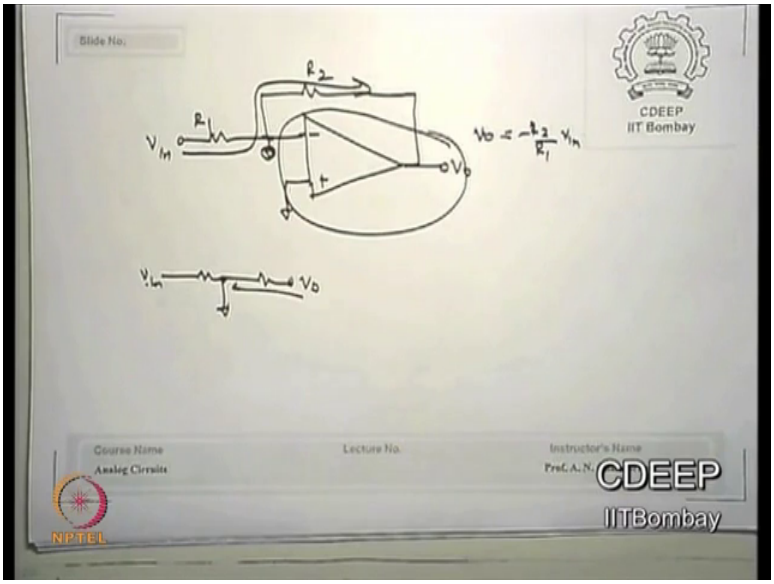

This is very interesting case this is question asked by many people in many interviews too many places including industry if you join okay. If this is your Vin and this is your V0, if you say this is that ground potential and actually show you will show me like this is (FL) is that clear to you. So, this is a potential divider where Center terminal is grounded is that correct to your V0 (FL) V0 is - R2 by R1 into Vin. (FL)

Only when I put OPAMP there which has those two properties then I may say the, this is at virtual ground and the current is same here is that correct. This fact must be understood that OPAMP's presence is the necessary to create a virtual ground and it is not a syncing ground is that correct. By putting this, this becoming a syncing ground is that correct. (FL) As soon as I remove Ri infinite on Ri infinite case this is the divider which has no input.

And that means this will not act like a system which you are looking for is that one clear. So, please do not consider that this is physical ground this is only virtual ground. Once I said it is 0

potential that is enough for me I am not saying it is syncing any current is that point clear. Once I have in my mind.

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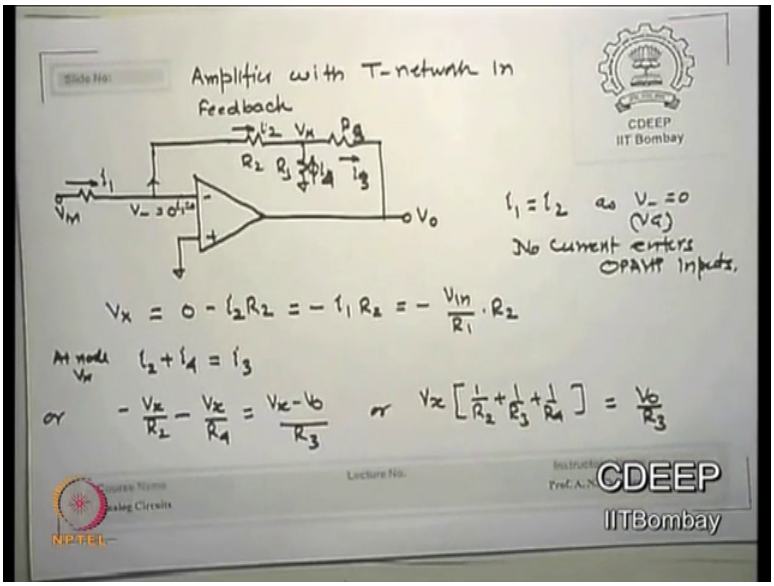

Now I can say another network before I quit no there are a few more networks against all okay. Here is (FL) from here can you tell me if I want to increase the gain or output voltage are not gain output voltage what should I increase R2 either I should make R1 very small or make R2 very large. So, larger they R2 larger is the gain I am I know very well known from there but then (FL) typically Ri let us say (FL).

It should not exceed or at least not equal to it should be always less than the Ri availability that is a condition you must use this is one requirement. There is another requirement please look at it the real theories what we go. As long as the ratio is what you had just gain can be same I can have 100 K and 10K for a gain of 10, 10 ohms and 1 ohm also I can happen. So, should I use 1 ohm, 10 ohm, 1 megaohm, 10 megaohm.(FL)

Okay, it does not cross Ri that much I fixed what what values I should choose and what it depends on R2 by R1 (FL) then I ohm by 1 ohm is 10, 100 ohm by 10 ohm is 10, 1 kilo ohm but 100 ohm is 10,1 mega ohm but 100 K is also 10 K (FL)values. As soon as I reduce the current I actually reduce the power dissipation is that clear to you. So, the choices of values of resistances are decided by the maximum minimum currents provided to you in the (FL) is that correct.

So, one has to accept but too high what is the problem I said the feedback problems will start then Ri (FL) is that clear. So, some way if you want to improve gains you will require R2 to be higher when you do not want R2 be too high is that correct. So, what they are do here is the solution.

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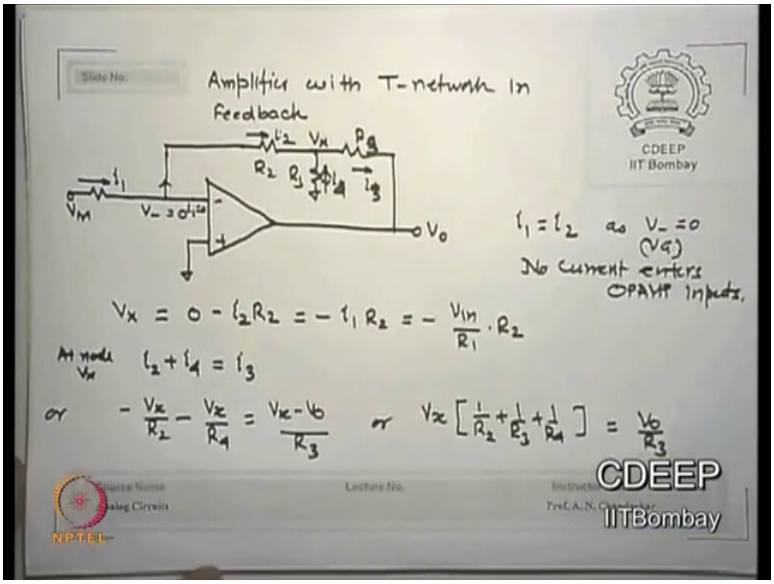

You replace your R2 by AP Network is that clear to you, what is my problem why I do not want to increase larger gain (FL) because if I increase out which will come very close to Ri I do not want that to happen. So, I said fine (FL) even now since it is a good OPAMP I1 = I2 because V- because I have put V+ at the ground equal to physically ground V- is the virtual ground. So, the current starting from input will be same as current in the resistor R2 this network is that clear.

Let us say current in this circuit is I2 (FL) this potential R declared as Vx this is V0 this is Vx this is how much (FL) is that okay, I2, I4 and I3 however I1 must be same as I2 (FL) because you are lonely said virtual ground is created. No, also please remember no current enters OPAMP input this is the reason why this is all possible okay. Now (FL) let us look at this potential Vx, 0 please look at it 0 - Vx divided by I2 is I2 or we can say I2 R2 is Vx (FL)with a - sign is that correct.

0 - Vx divided by R2 is I2, so, - I2 R2 is Vx (FL) voltage difference divided by resistance is the current is that correct, this potential - this potential divided by R2 is I2. So, - I2 R2 is Vx however we say I2 = I1 (FL) so, here I2 I2 is - I1 R2 but how much is I1 because of the virtual ground V in - 0 divided by R1 is the I1. So, V in by R1 into R2 is my Vx is that okay. Vx is –V in by R1 into R2, now we say at this node Vx I2 is I2 + I4 is the I3 (FL) is that okay.

I am summing current at node Vx entering current is I2 entering current is I4 living current is I3. Now you say why opponent it does not matter I will put - and correspondingly anyway okay. So, I say I2 + I4 is I3 but how much is I2 are just now calculated how much is I2 (FL) Vx by R2 is that correct. How much is I4 (FL) is that okay. I am opposite (FL) - Vx by R4 = Vx - V0 by R3 is the I3 current. Sum of the two currents at the node is equal to the third current (FL).

So, this is equal to this I have collected Vx terms from all of that so Vx = 1 upon R2 + 1 upon R3 + 1 upon R4 is V0 by R3. But how much is Vx (FL) -Vin by R1 times R2 (FL).

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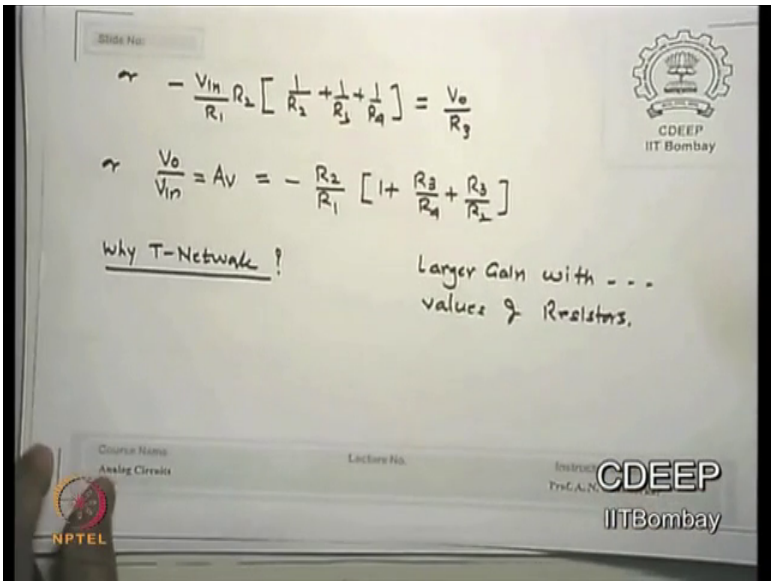

This is my Vx, so -Vin by R1 into R2 into 1 upon R2 + R3 + R4 is V0 by RI is that okay (FL) so that is - R2 by R1 into 1 + R3 by R4, R3 by R2, now can you see if I did not have T network so (FL) is that point clear what did I say. So, this term would not have in there this is a normal amplifier R2 by R1 and if I want larger gain R2, I would have increased. Now I say so not

increase R okay but adjust R3 R4, R3 R2 ratios which may not be very high okay resistance may not be very high and still boost the voltage gain is that clear.

So, now is that point clear many a times the limitation may come on your register values is that correct then (FL) when we are teaching network theory T Network, PI Network everything you are not very keen, we are only solving there (FL) I just showed you is that clear. This is how you actually play the games okay. So, this essentially does whatever most of you are already done but not in this format I am sure this was not the format.

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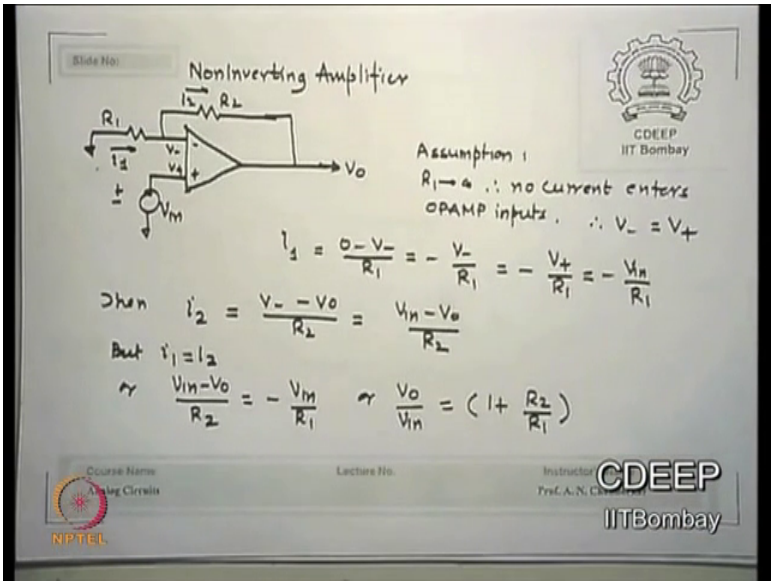

Before we could let us quickly see by same logic inverting amplifier (FL) what is inverting means - R2 by I1 is a phase shift of 180 degree so we say inverting. If I apply a input at the V+ okay and still be a show Ri is infinity and AOL is high V- still V+ (FL) can I calculate current i1 I calculate current i2 so, i2 is Vin - V0 by R2, I1 is I2 = V0 by I1, so, V in by R1 please remember this is V in (FL) is that clear.

(FL) 0 - V in by R1 is the I1 (FL) -Vin by R1 is V in -V0 by R2 they are equal currents same current flowing both sides but V0 by Vin is 1 + R2 by R1 + sign (FL). So, it is called non inverting gain amp lift on inverting amplifier V0 Vin + 1 + R2 by R1 if I want a non inverting amplifier with a gain of 100 what should be ratio of R2 by R1, 99 do not say 100 okay. It is 99 is that clear, so correspondingly you must adjust the values.

But if you do the inverting amplifier then what should be the ratio I want you to the value 100 because it is - R2 by R1 is that clear. So, there is slight difference in ratios when we do inverting and non-inverting amplifier.

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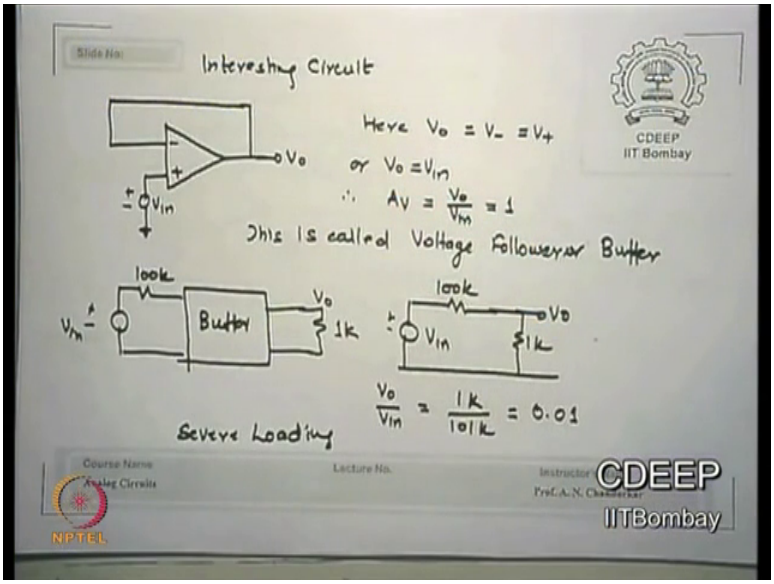

Last circuit there is a non-inverting amplifier with R1 not present and also not present okay I am connecting V- to the output okay there is no R1 there is no R2. I am just connecting V- to the output and then apply input at the V+ terminal. Now you can see V0 is V- same terminal (FL). But V - is V+, so V0 is V in because V+ is V in, so V0 by V in is 1 is that correct. So, V0 is V in what is the circuit I say called voltage follower or a buffer voltage follower or a buffer.

Now the second world why I wrote R buffer, (FL) what is the quality of the buffer that the input resistance and output resistance can be matched to any input side to output that is the buffer part is that clear. What is buffer means? (FL) Now let us take a case why buffers are required I have a sensor like a mechanical Cardinals (FL) if you have a strangers which creates a voltage of V in with series resistance of 100k.

And it has to be sent to a load of 1k (FL) is that clear (FL) what does that mean this has started loading this is called loading. If I have a small resistance here and which has a large series resistance actually (FL) at least it should have cross the input if nothing has (FL) so I do not like

such a connections. So, I said (FL) so, this will not load the other circuit input will not be loaded by the output that is why you need a word buffer is that correct.

So, PCB instrumentation amplifiers (FL) so you have to understand why we do all these gains because in reality we do not connect otherwise.

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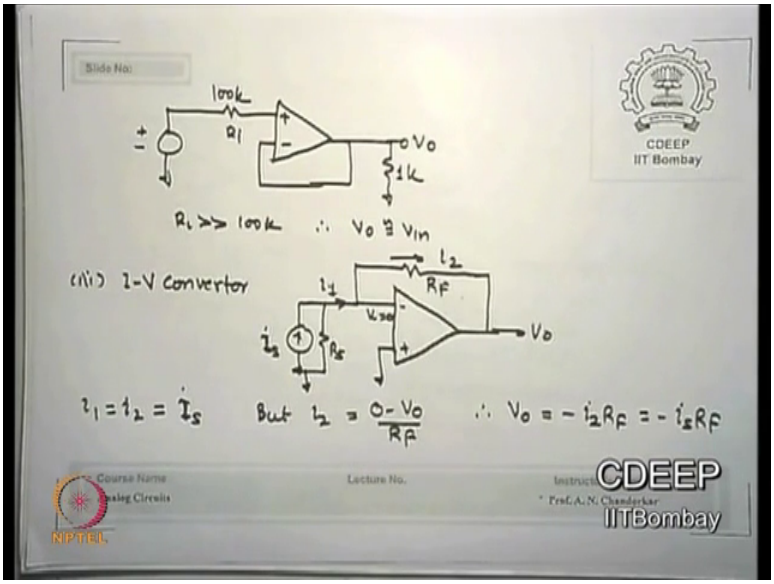

So, here is something (FL) nothing will enter in that so only voltage will appear here that is followed at the output is that correct. So, this resistance is very, very high which is what OPAMP will provide you this will only create a voltage which is proportional around passing so no drop here is that correct, no current passing 100k. So, this voltage appears here it is followed as it is at the output and it does not worry what resistance you are putting at the output is that correct.

This is buffered it so while the first is that clear buffers are essential part in any unknown sources okay. Otherwise like antenna of a mobile okay it has a 75 ohm billings has we called okay internally antennas (FL) everywhere you need some kind of an amplifier whose input should get protected from the output is that clear. Here 1k does not affect now 100 K side circuit because this has very large resistance allow all of it's to appear here and as follower all that will come out is that clear.

So, (FL) V in is that clear, now if you wish you can further boost it by R2 by R1, if you need the first stage must be a voltage follower is that okay thank you for the day.