Design of Power Electronic Converters
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Module: Gate Drivers
Lecture 23
Gate Driver Requirements

Welcome to the course on Design of Power Electronic Converters, we had started discussing with the module gate drivers. And last lecture, I had given you an introduction of gate drivers and I told you what is the need of gate drivers. So, now, let us look more into the gate driving circuit requirements.

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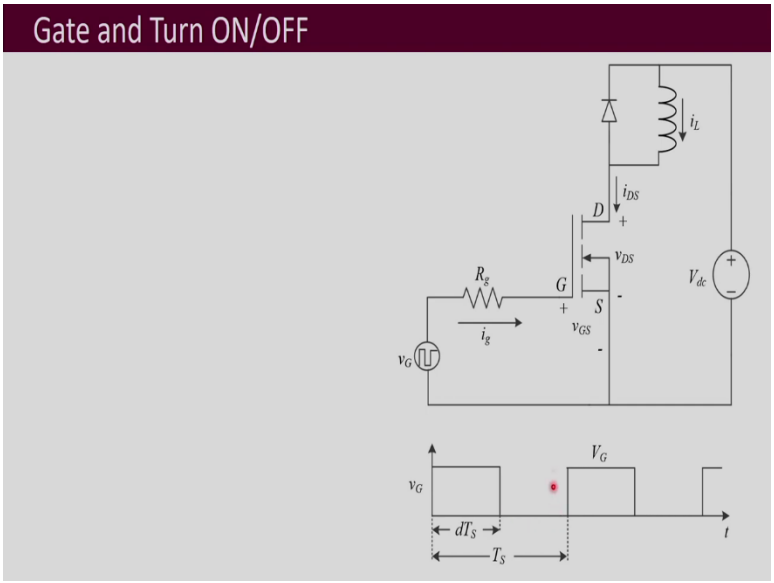

To understand that, let us first look into the turn on and turn off process of MOSFET and as we had seen before turn on and turn off process of MOSFET and IGBT are similar. So, we can take either of them and understand and the same applies for IGBT also. So, here there is a MOSFET and this is the gate circuit.

So, this v_G actually replaces the driver that you may be using and so, this is represented like switch to voltage source. So, then we have the gate resistor R_g which is connected between gate and the gate driver circuit and then we have this diode over here in the power circuit. So, this part is power circuit where we have the DC supply V_{dc} which forms the dc bus and then we have

a diode and when we have formed the current source using an inductor. So, you can assume it to be a large inductor.

So, what happens is that whenever this switch is turned on, the MOSFET is turned on then this i_L current flows through the MOSFET and when the switch is turned off, so, then the current flywheels through the diode. And this is the nature of v_G waveform that is supplied by this gate driver circuit which it is replacing as a voltage source.

So, you have dT_s as the duty ratio time period and T_s is the switching time period. So, dT_s time period it will be high that means, it is going to turn on the MOSFET and then rest of the time it is low which means it is going to turn off the MOSFET. And it reaches to this voltage of V_G. Now, here for simplicity I have shown these to be just as an instantaneous increase and decrease, but in reality, it will be not so, and that we will be seeing just in a while.

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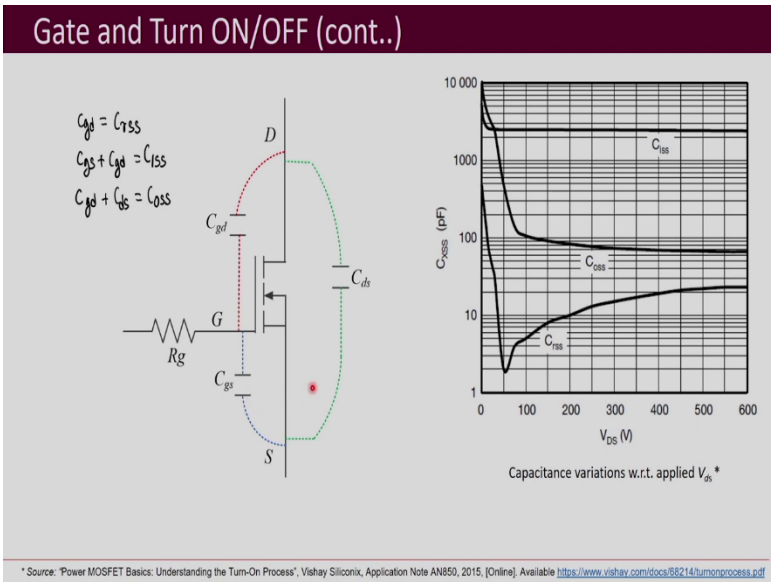

So, now, also recall that MOSFET has these three capacitances associated with it, parasitic capacitances one is gate to drain capacitance, then is gate to source capacitance and drain to source capacitance. Further, you have to recall that this gate to drain we have renamed it as C_{rss}, which is reverse transfer capacitance, then C_{gs} gate to source plus gate to drain that forms input capacitance C_{iss} and C_{gd} plus C_{ds} that forms output capacitance C_{oss}.

And these are not some fixed capacitance values, but they actually vary with the drain to source voltage that appears across the MOSFET and this is what that plot is showing. You can see here

that this input capacitance does not vary much with drain to source voltage as it changes, but output capacitance varies to some extent initially as the drain to source voltage changes and this C_{rss} you can see changes a lot with the change in drain to source voltage. Now, these three as we have seen before also in the last module play very important role in the turn on and turn off process of the MOSFET.

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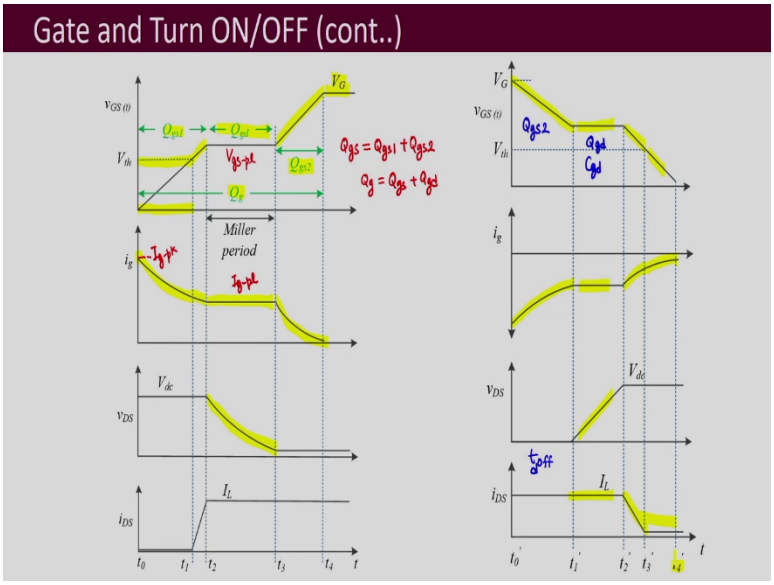

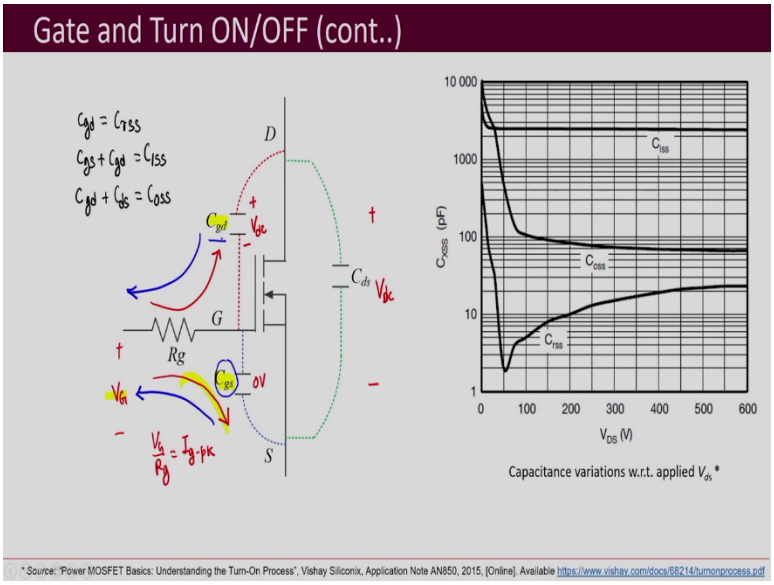

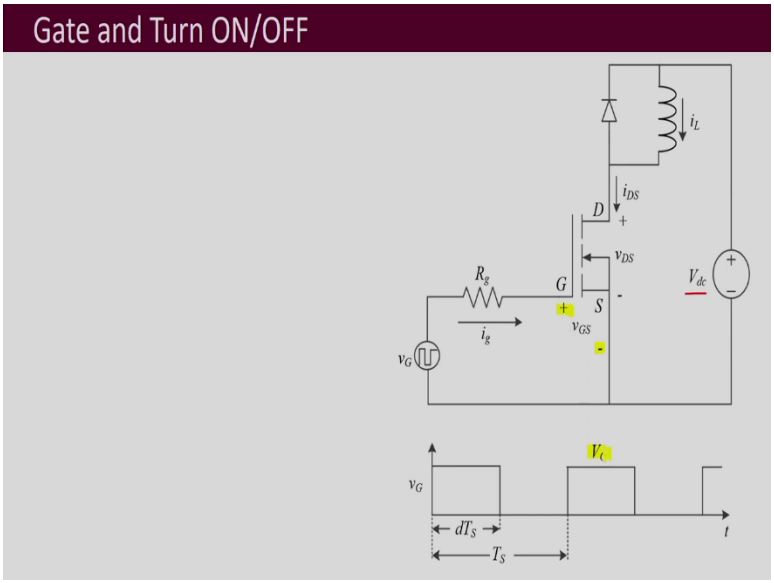

So, now, this is gate to source voltage v_{GS} which appears across the MOSFET. Now, here what we see is that form this time t_0 to t_1 for this time period the voltage first increases and it reaches to the threshold voltage V_{th} and at that time the voltage across the MOSFET does not change it is V_{dc} and the current through the MOSFET also does not increase it is equal to i_{DS} and we had seen that this time period is called as the delay time.

Now, what we did not see over there is the gate current, now what will happen is that during this time period which is called as delay time period during this delay time period, this Q_{gs1} that means this capacitance C_{gs} is going to be charged. So, this is the direction of the current over here this current is going to charge this C_{gs}.

So, that we can call it as Q_{gs1} is the charge associated with it and it reaches to the threshold voltage and you can see that this gate current is decreasing. Now, why we are showing that the gate current is decreasing because over here there is no charge initially. So, you can say that 0 V was there.

So, whatever was the v_G that was applied over here. So, $\frac{v_G}{R_g}$ is the peak gate current $I_{g(peak)}$ that we can say is the current that will flow at t_0. So, this is that current it flows $I_{g(peak)}$. So, this is $I_{g(peak)}$ from where it starts and it is going to decrease as this C_{gs} is going to be charged.

So, it decreases then it reaches the threshold voltage once it reaches the threshold voltage what will happen is that current will start to increase and at that time the drain to source voltage does

not change even then. So, this current increases and it reaches to this steady state current I_L and at that time also it is continuing to charge this C_{gs}.

So, the charge associated with it is Q_{gs}. So, this is that Q_{gs1} further it keeps on building up and this gate current continues to decrease over here. And this gate to source voltage keeps on increasing and it reaches to this voltage which is $V_{gs(pl)}$ we can say that is Miller plateau voltage, this is the Miller region. Here the gate to source voltage becomes constant it is not increasing.

So, what happens over here is that this C_{gd} was initially blocking the or was charged to the voltage of V_{DS} whatever was the blocking voltage. That means, this voltage was so, if MOSFET was blocking $\pm V_{dc}$ as we see here, this is that V_{dc} which it has to block when it is off.

So, this V_{dc} is what appears across this is what this C_{gd} was having the initial voltage as. Now, what happens is that as this capacitor starts to discharge from that, current flows through this and it flows in this direction and it discharges this capacitor C_{gd}. And during that time the charge associated over here is Q_{gd} and the gate to source voltage does not increase at that time and the current is almost also, you can see that it is kind of constant and we can call it as $I_{g(pl)}$ and the voltage that decreases during this Miller period.

After this device is almost on because voltage has also reached to almost towards on-state voltage and current has previously itself switched to the on-state current. So, the device is almost on, but what happens is that here we had applied this voltage V_G and so, this v_{GS} actually has to reach to this V_G voltage level and so, this C_{gs} further charges to V_G to this voltage level and that is you can say this Q_{gs2} and this gate to source voltage increases further and it reaches to this level of V_G.

And this gate current i_g further decreases and it almost becomes close to 0. So, this is the turn on process we had looked into it, but now, we looked into more from the perspective of charging and discharging of the capacitors. This total charge associated is this Q_g charge and the gate to source charges the sum of the Q_{gs1} and Q_{gs2}. So, Q_{gs} is equal to sum of Q_{gs1} and Q_{gs2} and then we have this Q_g which is sum of Q_{gs} and Q_{gd}.

Now, let us look into the turn off process which is similar and it is actually the opposite. So, first this voltage V_G decreases and it decreases to the Miller plateau voltage $V_{gs(pl)}$ and at that time the current flows in the opposite direction and it reduces in the opposite direction. So, that means,

what is happening over here is that, that the current is going to flow in this opposite direction, while turn off and it is going to discharge this C_{gs} whatever was the extra charge apart from what was associated with the Miller plateau voltage.

So, that means this Q_{gs2} which is going to be taken off first and at that time nothing happens this is actually delay time $t_{d(off)}$ and then it reaches to this Miller voltage. Once it reaches to this Miller voltage at that time the current does not change, the voltage does not change and this voltage builds up, however the current remains same it does not increase.

So, at that time what is happening is that this current is flowing in this direction and this $+V_{dc}$ voltage again starts to build up across the device and so across C_{gd}. So, this capacitor C_{gd} charges to V_{dc} and the charge associated here is equal to Q_{gd}. Then further what happens is that, it comes down to the threshold voltage level once the Miller period is over and during this time the gate current reduces and at that time this drain to source current comes down to close to 0 or the leakage current.

And further in case of MOSFET, the device is almost off once it has reached the threshold voltage, but in case of an IGBT you may be having tail current and still the turn off may take longer. This current may be still flowing like this, but in case of MOSFET it will be almost off. So, whatever is the voltage here and the associated gate current will continue to decrease and it will almost become close to 0 at the end of this interval which is $t_{4'}$.

So, what we see from here is that it is capacitance C_{gd} which plays a very important role and gate to source capacitance C_{gs} is charged during the turn on process and it is discharged during the turn off process. Whereas, the gate to drain capacitance is discharged during the turn on process, it is discharged from whatever voltage it has from V_{dc} that is the blocking voltage and while it is turned off it again gets charged to that voltage of V_{dc}.

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Gate and Turn ON/OFF (cont..)

linear approximations
crude estimate

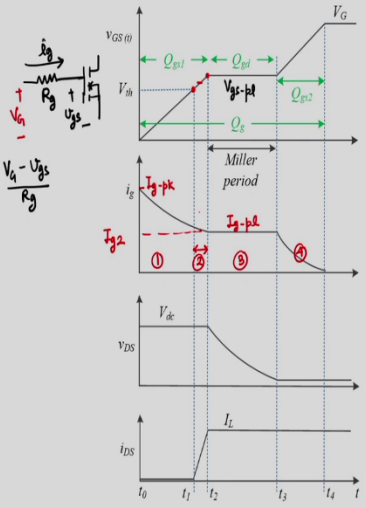
$$I_{g2} = \frac{V_G - 0.5(V_{gs\text{-}pl} + V_{th})}{R_g}$$

$$I_{g\text{-}pl} = \frac{V_G - V_{gs\text{-}pl}}{R_g}$$

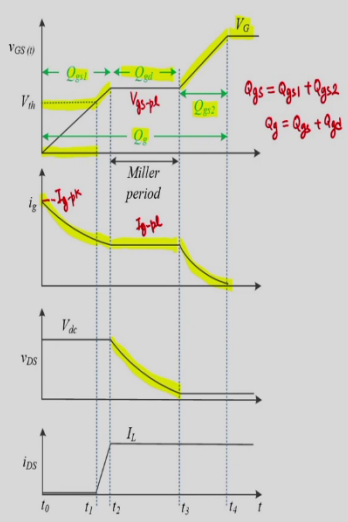
Interval ②: $t_2 - t_1 = C_{iss}\,\frac{V_{GS\text{-}pl} - V_{th}}{I_{g2}}$

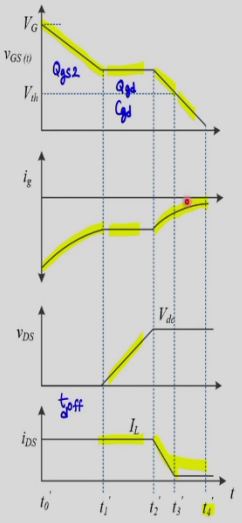
Interval ③: $t_3 - t_2 = C_{rss}\,\frac{V_{DS,off}}{I_{g\text{-}pl}}$

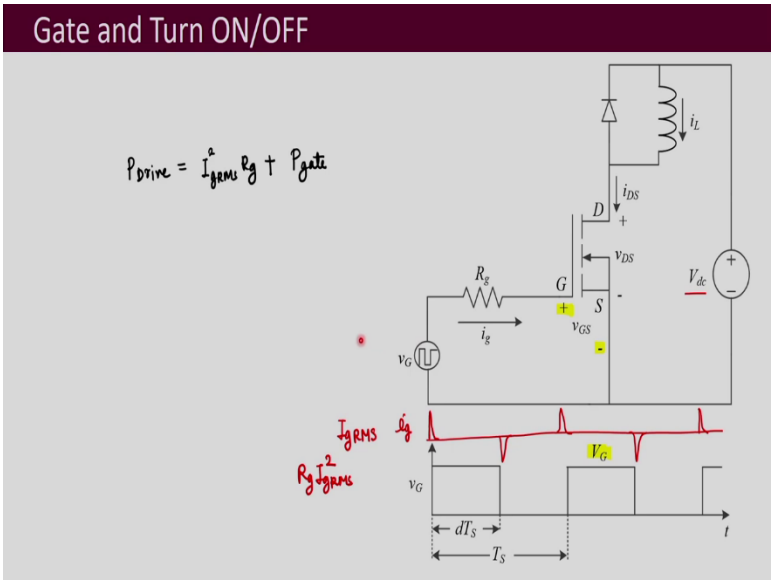
$$I_{g\text{-}pk} = \frac{V_G}{R_g}$$



Gate and Turn ON/OFF (cont..)







So, let us write some equations related to these which will help you in doing some very crude estimation of the requirements of gate driver. Now, do not think that they are correct equations, they are linear approximations and they only provide you crude estimates. So, do not have questions like why this so, it should not be like this, this is an RC circuit and these are not really the correct equations, this is not how it should be, you may be having all these questions. But these are all linear approximations, a very crude very rough way of getting some numerical values which will help you in choosing the gate driver.

So, as we had named some of these, so, this we named as $I_{g\text{-}pk}$ and this current is $I_{g\text{-}pl}$ the Miller plateau and over here also this is interval 2, this is interval 1, this is interval 3, which is Miller plateau period and then you have another interval which is interval 4.

So, during this interval, let us say that in between you have this current which is given as I_{g2}. So, now, if we write some equations, very linear equations,

$$I_{g2} = \frac{V_G - 0.5(V_{gs-pl} + V_{th})}{R_g}$$

And, why it is so? Because you have this gate resistor R_g over here then MOSFET is there and this voltage whatever is gate to source voltage. During this interval 2 this gate to source voltage is equal to V_{th} and here it is equal to $V_{gs\text{-}pl}$. So, in between if we want to find out that will be half of the sum of this two.

So, that is what you can think of the voltage as V_{gs} equal to and here what you have applied is V_G. So, basically the equations that we are writing ($V_G - \frac{V_{gs}}{R_g}$) is the current that will be flowing here. So, that is what I_{g2} is taken as equal to. Then the next we can write Ig during the Miller period or Miller plateau region

$$I_{g-pl} = \frac{V_G - V_{gs-pl}}{R_g}$$

This is very straightforward over there and then during this interval 2 which is (t_2 - t_1) in this case as we have named this will be given as

$$t_2 - t_1 = C_{iss} \frac{V_{gs-pl} - V_{th}}{I_{g2}}$$

Now, why we are writing this? Because we know that during interval 2 what is being charged is the input capacitance. So, this is the input capacitance over here which is going to be charged. So, that is C_{iss} and so, the total charge is the time period multiplied by the current value and that will be C_{iss} multiplied by this voltage difference and voltage difference is ($V_{gs\text{-}pl}$-V_{th}) for interval 2.

And then for interval 3 which is as we have named ($t_3 - t_2$) is equal to

$$t_3 - t_2 = C_{rss} \frac{V_{DS,off}}{I_{g-pl}}$$

and we have also written for peak current of the gate

$$I_{g-pk} = \frac{V_G}{R_g}$$

Now, these are some of the equations which you can use for calculations related to gate circuit. Now, one more thing that you have to observe is that this gate current you can see that this is not continuous current it is there during the turn on process and then it is there during the turn off process in between it is not there. So, that means if we have drawn this gate current over here then this gate current I_g would have been something like this, you would have observed this during this turn on process and again during the turn off process.

So, if you have to find out the I_{gRMS} so that would have been very small value. Because there is going to be some loss associated with it and that loss is

$$P_{Rg} = I_{gRMS}^{2} R_g$$

And whatever is these drivers power requirement if we call it is P_{drive}

$$P_{drive} = I_{gRMS}^{2} R_g + P_{gate}$$

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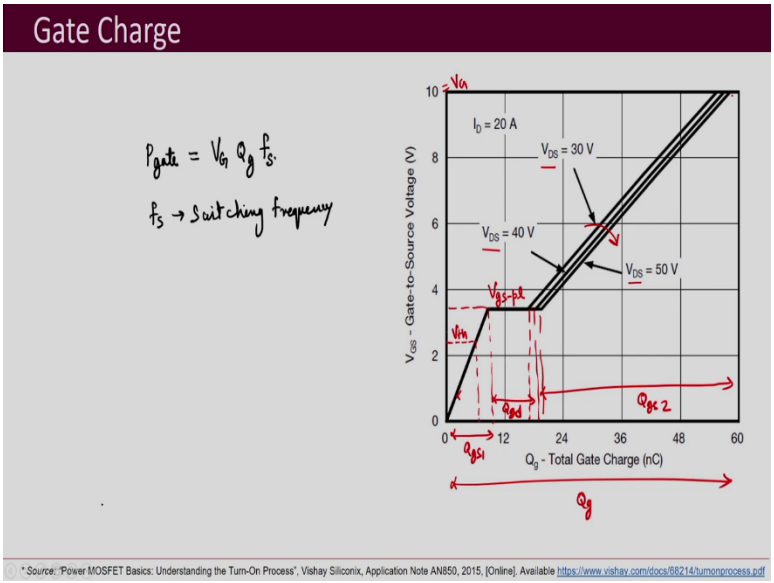

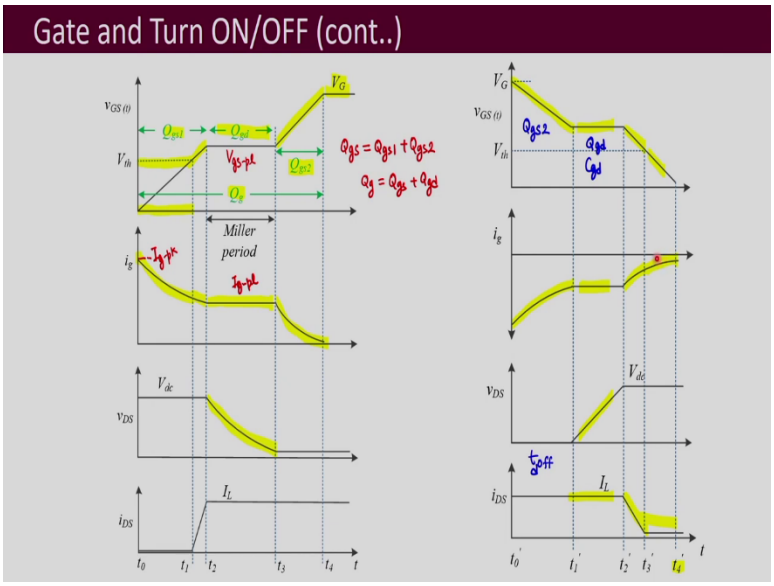

So now, what is the P_{gate} equal to? P_{gate} we can find out from this kind of graphs. This we have seen before also when we discussed the devices, this is gate charge versus gate to source voltage. And this is similar to this kind of graph that we see here, instead of time this voltage can also be plotted with respect to the charge.

So, here it reaches to this threshold voltage. So, somewhere here let us say is threshold voltage V_{th} and then further over here it will reach to Millar plateau voltage which we are naming as $V_{gs\text{-}pl}$. Then after that from here or here depending on what is the V_{DS} voltage the, for the MOSFET the Miller plateau region may change and it may increase.

So, as V_{DS} increases, so, we can see that how it charges in the further the 4th interval and that has got some effect on that. So, this part is Q_{gs1} and this part is Q_{gs2} and this interval in between for the Miller period is Q_{gd}. And the total charge associated with it is equal to Qg and that depends on how much is the V_G that we have applied.

So, let us say if V_G is10 V. So, it has to reach to here. So, then P_{gate} will be written as

$$P_{gate} = V_G Q_g f_S$$

So, f_s is switching frequency here which may be 100 kHz, 50 kHz or 20 kHz whatever switching frequency that you may be using for your circuit.

So, this P_{gate} gives us the estimate of the power required on the gate emitter or the gate source region for the MOSFET or the IGBT. Now, let us look into how do we estimate what should be the gate resistor that should be used and what should be the power level of the driver IC. I have already shown you some equations which you can use.

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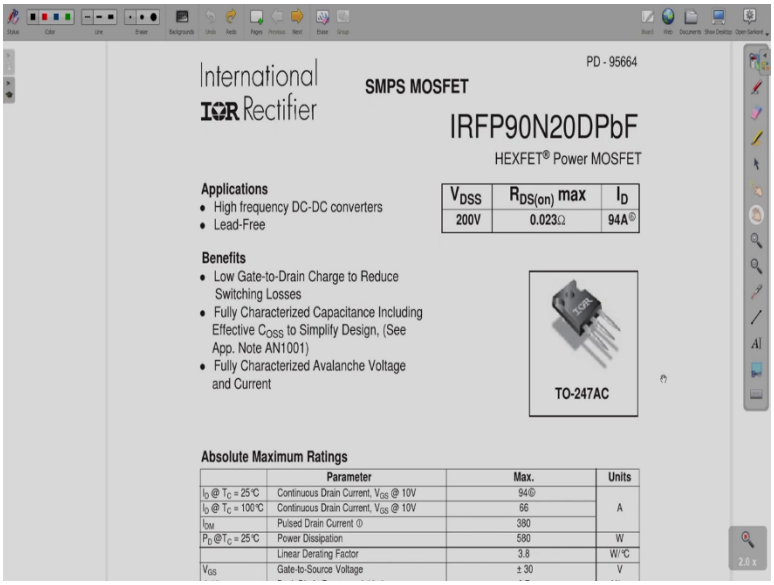

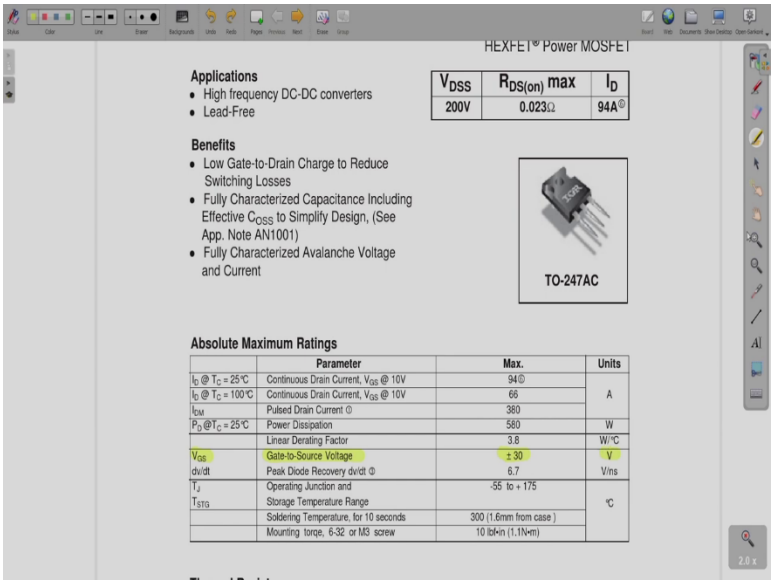

HEXFET® Power MOSFET

Applications
- High frequency DC-DC converters
- Lead-Free

V_{DSS}	$R_{DS(on)}$ max	I_D
200V	0.023Ω	94A⑥

Benefits
- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current

TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	94⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	66	
I_{DM}	Pulsed Drain Current ①	380	
P_D @T_C = 25°C	Power Dissipation	580	W
	Linear Derating Factor	3.8	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	6.7	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torqe, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Now, let us also see the data sheet which are the specifications which you should be noting down for selecting or rather estimating the requirements of the gate driver. This is the data sheet of a power MOSFET of 200 V and 94 A. I have explained this data sheet to you before as well. So, now, again let us revisit it and look into it from the driver perspective. So, from driver point of view what you see here is that this gate to source voltage maximum ratings is ± 30 V.

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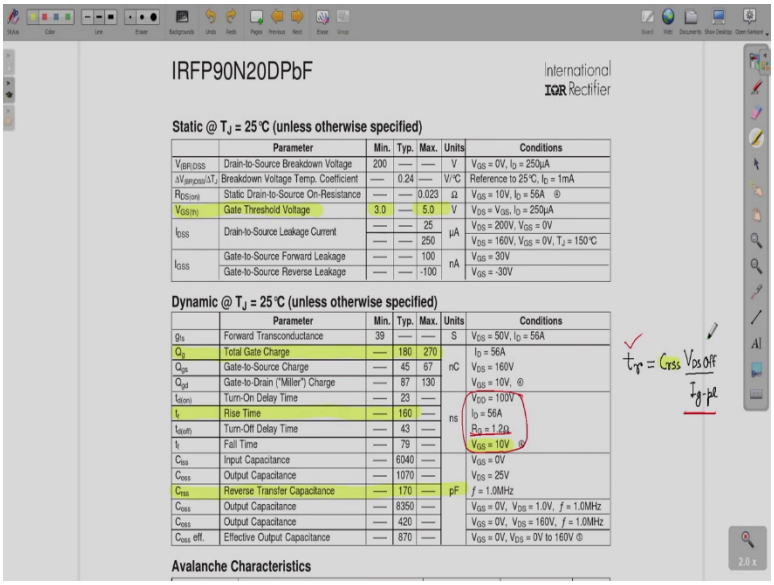

IRFP90N20DPbF

International IOR Rectifier

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.24	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.023	Ω	V_{GS} = 10V, I_D = 56A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 200V, V_{GS} = 0V
		—	—	250		V_{DS} = 160V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	39	—	—	S	V_{DS} = 50V, I_D = 56A
Q_g	Total Gate Charge	—	180	270		I_D = 56A
Q_{gs}	Gate-to-Source Charge	—	45	67	nC	V_{DS} = 160V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	87	130		V_{GS} = 10V, ④
$t_{d(on)}$	Turn-On Delay Time	—	23	—		V_{DD} = 100V
t_r	Rise Time	—	160	—	ns	I_D = 56A
$t_{d(off)}$	Turn-Off Delay Time	—	43	—		R_G = 1.2Ω
t_f	Fall Time	—	79	—		V_{GS} = 10V ④
C_{iss}	Input Capacitance	—	6040	—		V_{GS} = 0V
C_{oss}	Output Capacitance	—	1070	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	170	—	pF	f = 1.0MHz
C_{oss}	Output Capacitance	—	8350	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	420	—		V_{GS} = 0V, V_{DS} = 160V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	—	870	—		V_{GS} = 0V, V_{DS} = 0V to 160V ⑤

Avalanche Characteristics

Now, further what we see here is the threshold voltage is also given which is minimum 3 V and 5 V. So, whatever gate to source voltage that you will be applying has to be greater than 3 V at

least. Then, what we see here is this total gate charge is also given. So, this you can use to do the estimation of gate power requirement.

Then further what we see here is that this rise time t_r is also given. Now, this rise time how we can use it, we just saw that equation for this Miller time period we can write

$$t_r = C_{rss} \frac{V_{DS,off}}{I_{g-pl}}$$

Although t_r is not exactly the Miller period it is slightly greater than the Miller period. But either you can use this t_r itself what is given in the datasheet or you can use something lesser than that also. So, from here you can calculate this $I_{g\text{-}pl}$ or this you can calculate by using this t_r value. So, also what you see here is that all these values are given for which they have given all the specifications.

So, V_{DD} is 100 V, I_D is 56 A, they already have given some R_g value, which they have used for finding out these times experimentally. Now, it is a good thing to use these values as the starting point for whatever design you may be doing. You may use it or you may use something higher than that or lower than that as well.

But that gives you first idea that this R_g is 1.2 Ω, or more than that, or somewhere less than that and that is what you are going to be using. And what is the V_{GS} voltage 10 V that is also what they have used. So, that also gives you an idea of how much is the V_{GS} you can use to start experiments with. Of course, 10 V may be less, you may be wanted to apply more than that, but these are just to give you some starting points to do your design.

So, these are the things that you can note down and further what you can note down is also C_{iss} input capacitance and this reverse transfer capacitance values, which are also provided here and V_{DS} you know it from your circuit. And we have got other equations also that I had shown you which you can use to do the calculation of R_g.

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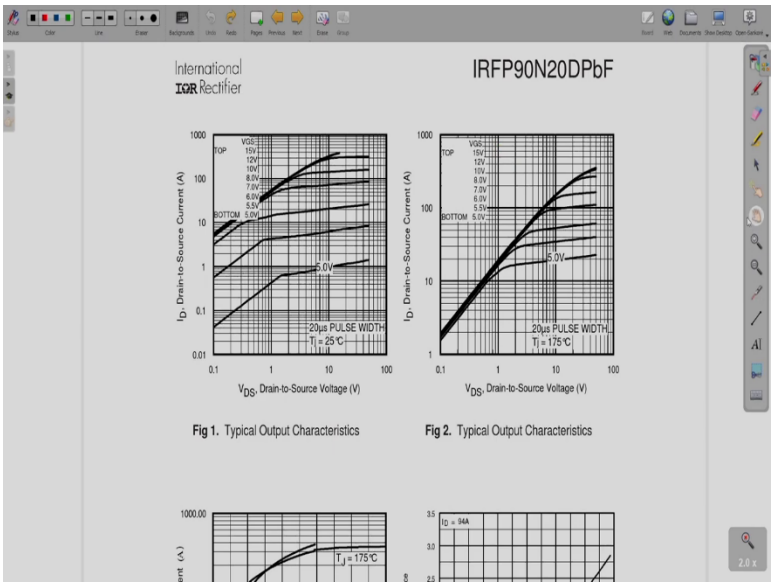

Next, some of the other graphs which are of importance to look into while designing or choosing the gate driver circuit is this over here, what you can see here is the drain to source voltage versus drain current. And what is the V_{GS} that is applied. So, you can see here that above around 10 V or 12 to about 15 V it enters into the ohmic region. So, that is a good point to apply like around 12 V or 15 V as gate to source voltage.

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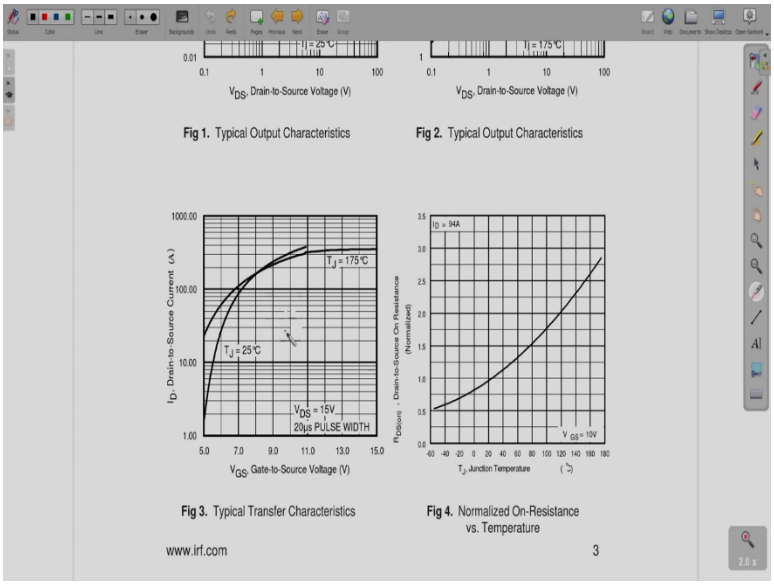

And then you can also see this transfer characteristics V_{GS} versus I_D. And again, what we see here is that this is the threshold and then above as this voltage increases, what is the point when drain

current starts to build up. So, from here also you get an idea of how much is the gate to source voltage that you should be applying. So, you get the idea of Q_g, you get the idea of V_{GS} and some equations are given. Plus, you also get an idea of R_g, what is given in the datasheet. So, from all these different values, you get an estimate of what is the gate drive requirement.

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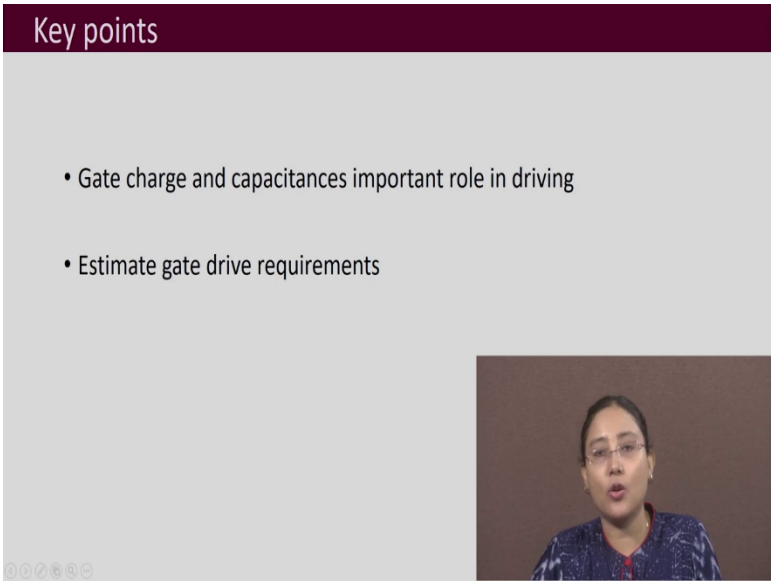

So, what are the key points of this lecture? So, gate charge and capacitances they play a very important role in the turn on and turn off process. And so, you are choosing your gate driver circuit and you have to estimate your gate drive requirements, R_g values and other different current and voltage requirement values before being able to choose a proper gate drive circuitry. Thank you.