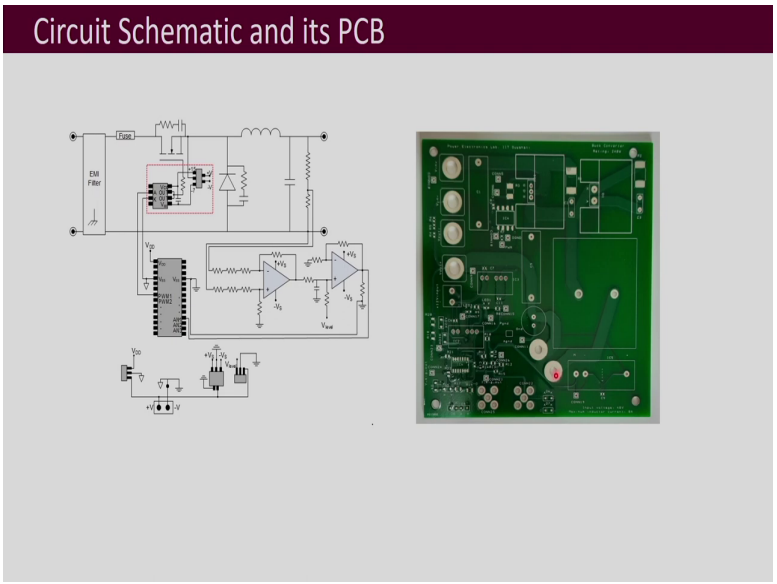
Design of Power Electronics Converters
Professor. Dr. Shabari Nath
Department of Electronics and Electrical Engineering
Indian Institute of Technology, Guwahati
Module: Hardware Design
Lecture 66
PCB - II

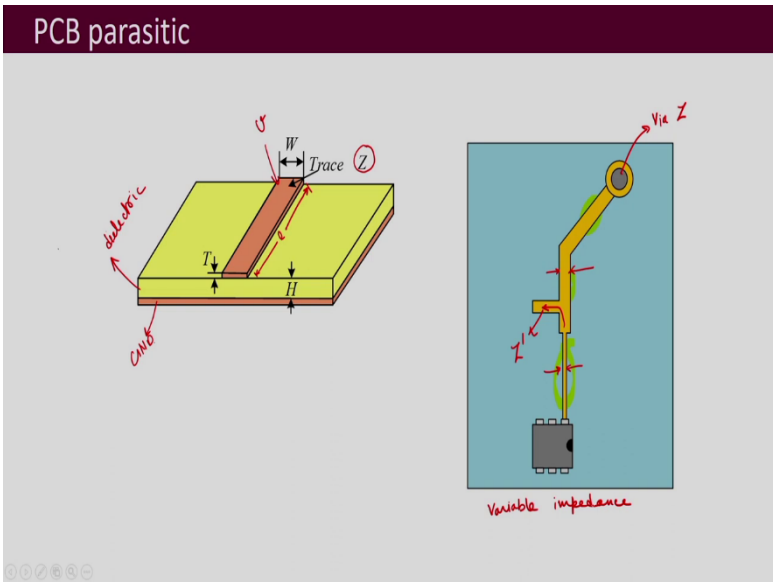
Welcome back to the course on the design of power electronic converters, we were discussing hardware design, and we had started also discussing printed circuit boards. So, the last lecture, I gave you an introduction to PCBs and the PCB making process and the different terms, common terms associated with PCB. Now, let us continue our discussion on PCBs.

(Refer Slide Time: 0:56)



Now, as I told you when we design a PCB, so first, we draw the schematic and then further we do the layout of the PCB. So, let us say if this is the circuit and this is the PCB, I mean this is the schematic of the circuit that we want to do the layout and then this is the layout or the PCB that we obtain. The question is, are these two exactly same? What theoretical circuit you are drawing on the schematic? And what do you are finally getting in the PCB, do they match exactly or are there any differences between the two?

(Refer Slide Time: 1:44)



So, for that, let us look into a very simple part of a PCB, let us say there is one trace like this, which is a copper trace. Now, here, what we see is that this trace will have a thickness that will be whatever the thickness of the copper layer. So, let us say that the thickness is T. And this trace will also have a length. So, that is, let us say the length L. And further, it is copper width W. Now, so it is like a strip and obviously, it will have its own resistance and also it will have some inductance.

So, that means it will have parasitic resistances and parasitic inductances in the trace. Further, let us say at the bottom there is another plane which is a copper plane, it is a fully filled copper layer. So, let us say if that is connected to 0 means that is the reference or it is connected to the ground and there is some voltage V that is applied.

So, now we have our dielectric material in between, becaue we have an insulation material over here. So, that is like two plates. And then there is in between a dielectric material. So, that is a formation of a capacitor. So, this capacitance value of course, is going to be very small, it is a parasitic capacitance, stray capacitance, but it has some value, that mewhichwe will have an impedance of trace which is so simple to look for.

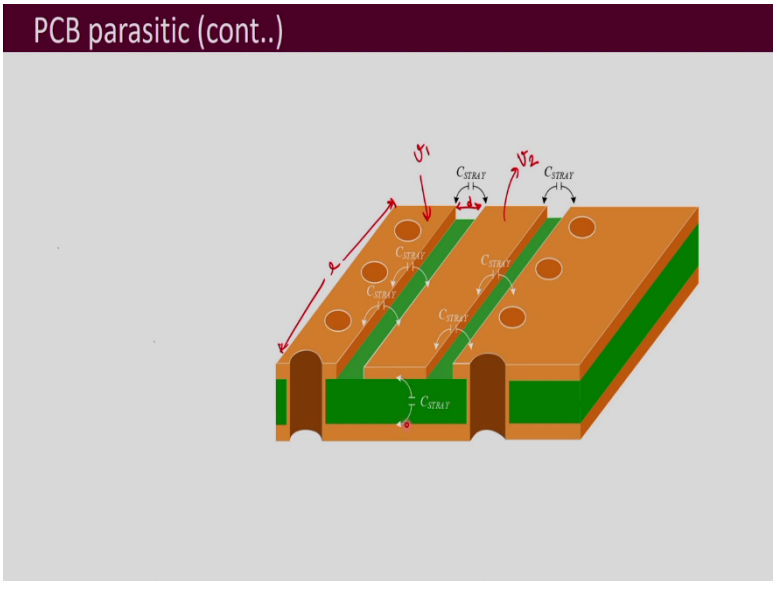
So, what we are connecting by a copper trace or what to which, we thought in the schematic that it is just a simple connection straight connection, ideal no r, l, and c associated with it, when you place it on the PCB that means when you form the layout using the copper trace, then unknowingly you are introducing some impedance in that simple connection. And it is not as simple always as it looks.

Let us say if we are forming a connection between the pin of this IC let us say this pin is supposed to be connected to this point. So, let us say this is a wire. So here, what we see is that the way the layout is performed the thickness of the width of the trace is varying. So, here it is the same as this point, but between this and this over here in here the thickness of the copper track is different. Further, in between you see that there is another track which is emerging and that track may be going somewhere else, which is not shown here.

So, obviously, the impedance of this part the impedance over here the impedance of this part, this part will all be different and ,further this wire also will have its own impedance R, L, C associated with the wire or the through hole whatever we were using. And the impedance over here also will be different.

So, what we see is that there will be variable impedance means at different, different points in the PCB, depending on the placement of the traces placement of components, and their weight and then thickness and their shape, the impedance is going to vary. And so, the performance also will be affected. So, what we thought as a simple schematic, when we had simply drawn the theoretical schematic and what you are laying out and what you are getting out of it, they are not exactly the same.

(Refer Slide Time: 6:28)

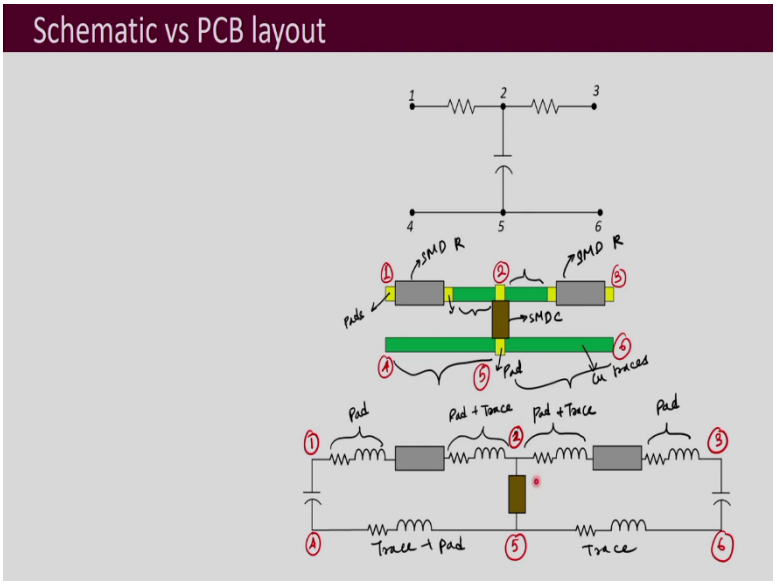


Further to clarify the stray capacitances here in this diagram, what is shown is that you can see that there are 3 traces on this top side and in between them also there will be stray capacitance. And the reason for that is let us say if there is voltage V_1 here, there is voltage V_2 here. These are two adjacent plates, and in between there is air. So, air means that is also

an electric medium. And these are 2 metallic plates, we can say that are copper traces. So, obviously, there is a formation of a capacitance here you will be having whatever is the distance d and based on the length l of these copper traces.

So, when we are placing two copper traces adjacent to each other, then there is going to be some stray capacitance in between them. Further, when those copper traces are on different layers, so, then also, again, we will have stray capacitance there. So, all throughout the PCB, there will be several places where we will be having stray capacitances. And as we are routing it, of course, everything will have stray inductance and stray resistance.

(Refer Slide Time: 8:05)



Now, let us say we want to do the layout of a sim very simple circuit like this, where we have two Rs and one C. And let us give the name of these nodes as 1, 2, 3. And these three, according to theory, these are the same nodes this 4, 5 and 6, they are just short, I could have also just named it as 4, because from your knowledge of basic electrical circuits, and the way we analyze these three are the same.

Now, when we do the layout of it, let us say we are going to use SMDs for these three components. And so, these are your those SMD resistors, two SMD resistors here and this is the SMD capacitor. And these are the pads, the SMD pads, all these ones, the yellow color whatever it is shown are the pads and these green ones are the copper traces. So, here this is the connection between these three components that is formed between two resistors and this capacitor.

And this is just laid out because let us see, if you have an input over here and if our output at this point, so to denote that this is copper trace, which will present this line 4, 5, 6. So, let us give the numbers here. So this is point 1, 2, and 3 points according to the schematic and this is point 4, 5 and 6. And now let us ignore the parasitic associated with the components.

That means I am ignoring the equivalent circuit of the resistor that means the resistor itself will have some parasitic inductance or parasitic capacitances. This capacitor's equivalent circuit also we had seen before, it will also have some parasitic resistance and inductance. So, those things we are ignoring, we are just looking in from the perspective of simple parasitics introduced by the PCB layout.

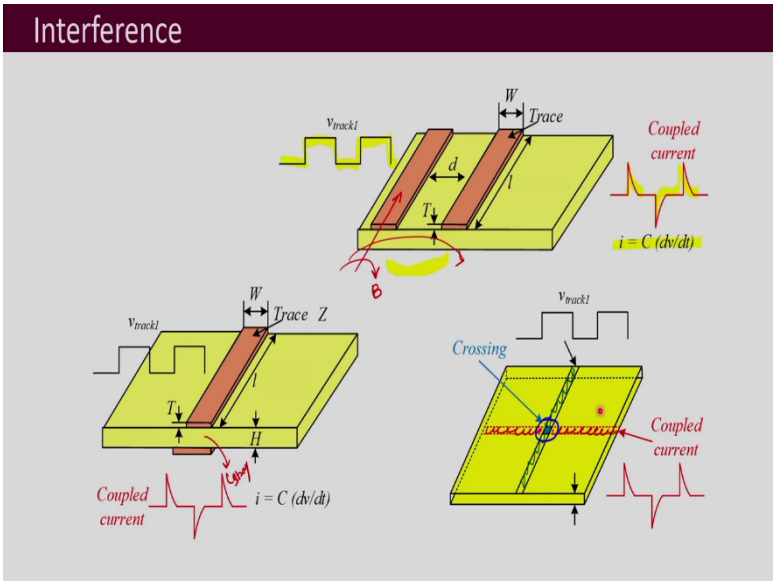
So, what we see here is that this pad will have its own R and L. So, that is of the pad. So, these two are of the pad, then, these two are an R and L for the pad plus the trace. So, this much of the trace and then further again this part is so, he this is point 2 and this is node 1 and this is node 3 according to the schematic and so, this further again this is the parasitic introduced by the pad plus the trace over here this part.

And here, this is the parasitic introduced by the path and then for this part also for the trace plus the pad, we have another parasitic over here, over here and further again this is for the trace this part of the trace and these two are at different potentials. So, there will be capacitance in between them. So, that is the parasitic capacitance that is shown here and also over here whatever is the parasitic capacitance that is shown here.

So, let us write the node numbers. So, this is 4, 5 and 6. So, what we observe is that, that this is what we wish to lay out and when we realized this circuit on the PCB, so, this is what is we have realized. So, this difference you have to note down. Now, sometimes the effect of this difference is negligible and sometimes the effect is not negligible, it can distort the performance of the circuit and these parasitics are what creates lot of noise also means, the deviation of the signal from what it is meant to be.

Obviously, these are parasitics and so, they are very small in value, but not always those small values can be neglected sometimes they become important especially, when the frequencies become high.

(Refer Slide Time: 13:37)



Now, let us see how do these impedances or these non-idealities are also responsible for creating interference? So, now, let us say that there are two traces which are parallel to each other and there is a distance d between them, there is a thickness T and there is length l. And so, air is the dielectric between them, so, there is a parasitic capacitance between them and if this is the nature of the voltage in track one, so, this is the nature of the voltage.

So, whenever this voltage is changing, it is not going to change instantaneously that obviously any practical signal will have some rise time and some fall time. So, during that time, there will be this current associated with the stray capacitance which will be your

$i = C\, dv/dt$

and this is that current that will be flowing. So, this is the coupling that has got formed between these two traces. So, that the current will then disturb, may disturb whatever was originally flowing in these two traces.

Further if, let us say there is a current flowing in it, and that current is alternating in nature. By alternating, I do not mean that it is a sinusoidal alternating it is varying. So, if it is varying it will create its own magnetic field B which will also be varying and that will get further coupled with this trace, this second trace and will induce a voltage and that induced voltage will then create its own current and so, then we will have disturbance created in this second trace.

So, we see that there now there is interference created because of this parasitic capacitance and this change in voltages and currents. So, there is a problem of electromagnetic interference occurring inside the PCB.

Similar phenomena you can observe here also where the traces are on top and bottom you can see that here also there will be some parasitic capacitance and if we have a voltage waveform like this in this trace, then that will have the coupled current which will be flowing according to

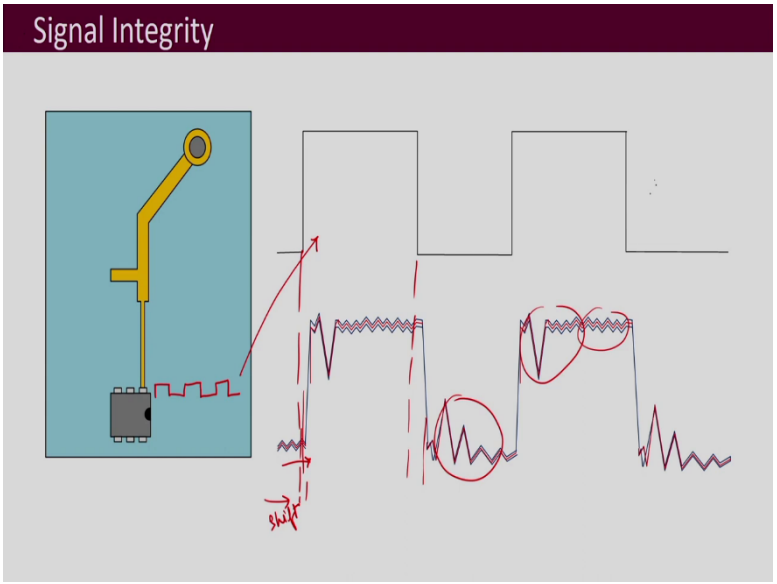
$I=C\ dv/dt$

and similarly, voltages can also be induced if we have the currents which are variable.

If we have case like this where the traces are just crossing, let us say one traces on the top. So, this is the one, one trace, which is on the top layer and there is no other trace which is on the bottom layer and there is a crossing that is getting formed over here. So, this crossing because of it also there will be some stray capacitance getting formed.

And then again if you have voltages like this, which are going to change, so, we will have the capacitor currents because of it. So, what we observe is that at different places in the PCB, because of the very placement of the traces in different ways, there is problem of electromagnetic interference that will be getting created.

(Refer Slide Time: 17:33)



Now, there is another term which is called a signal integrity, which a power electronics engineer should be familiar with, we will not go into the details of this because these are

really wide topics in themselves, we will just get an idea of what it is. So, let us take the example of this where we have an IC pin which is getting connected to a wire. So, here what we saw that the impedances are variable.

Now, let us say that, the signal that was sent at this point was like this, which is what is shown over here, it was a very nice neat and clean signal that was sent by this point. And what you receive over here when you measure it using the oscilloscope is something like this, which is the not exactly same as the one which was sent at this point, one which was transmitted at this poia nt, there is difference between the transmitted signal and the received signal at different points.

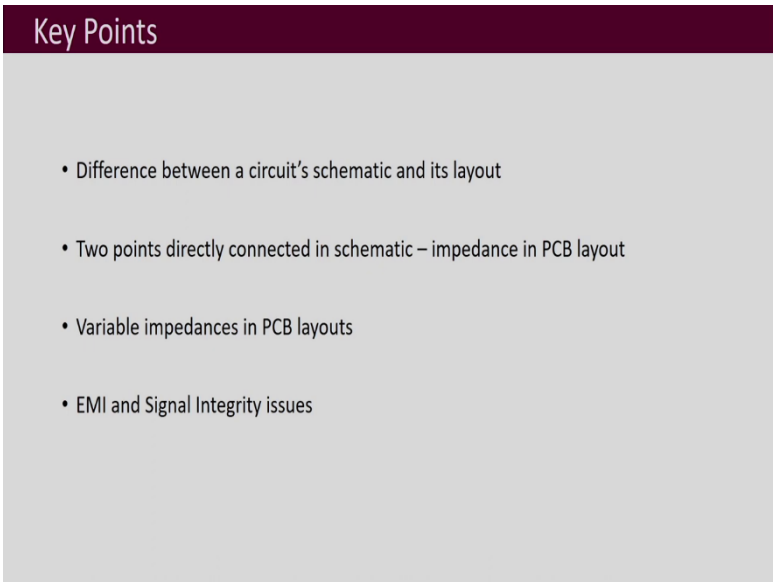
So, the difference is, is what you call as the noise and by now, you have an idea that because of all these impedancthesend all this interferences that are created inside the PCB, where the signal is no more the same. So, the signaa l can have delay. So, this can be delayed this rise may be delayed from the originand al signal, the fall can also be delayed, further there can be a shift also in it and all these noises that we observed means that there is a problem with the signal integrity.

Signal Integrity means that as from the very name you understand that whatever is the signal that we expected or whatever was transmitted we would like to receive it most as the transmitted signal, but that does not happen there is noise in it. So, to what extent the noise is and can from that if we can get the original signal or if we can understand what the original signal is, then we can say that the signal is good enough, there is signal integrity.

So, when you do the layout to the PCB know that while doing the lay out your signal integrity of whatever signals you are sending, that may get affected and then power electronics also, we have to be careful about because these days with better power semiconductor devices coming in like your silicon carbide and gallium nitride new wide band gap devices coming in the switching frequencies and going high.

So, we have to be careful about the signal integrity. So, that the PWM gate pulses that you send and what you receive should be the same, the signal integrity issues are more of a concern in digital circuits.

(Refer Slide Time: 21:13)



So, the key points of this lecture are that, there is a difference between a circuit schematic and its PCB layout. In a schematic or what you show as a direct connection between two points know that when you are laying out in the PCB, it is not a direct connection there is impedance between the two point and these impedances in PCBs, they are variable in nature.

Because of the variable lengths of the traces, their weight and the wires and the holes and many things placed in the PCB, tthe impedance is not a fixed width is not fixed. It is variable it is different in different, different places. And in PCB, you know there are issues of electromagnetic interference and signal integrity. So, while doing the layout of the PCB, one should be very careful about these issues. Thank you.