Indian Institute of Technology Kanpur

National Programme on Technology Enhanced Learning (NPTEL)

Course Title
Digital Switching

Lecture – 13

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Okay, now I have to build up a time switch where number of input slots and number of output slots per frame are different so this can be done using a dual memory system so let us see how this will be done.

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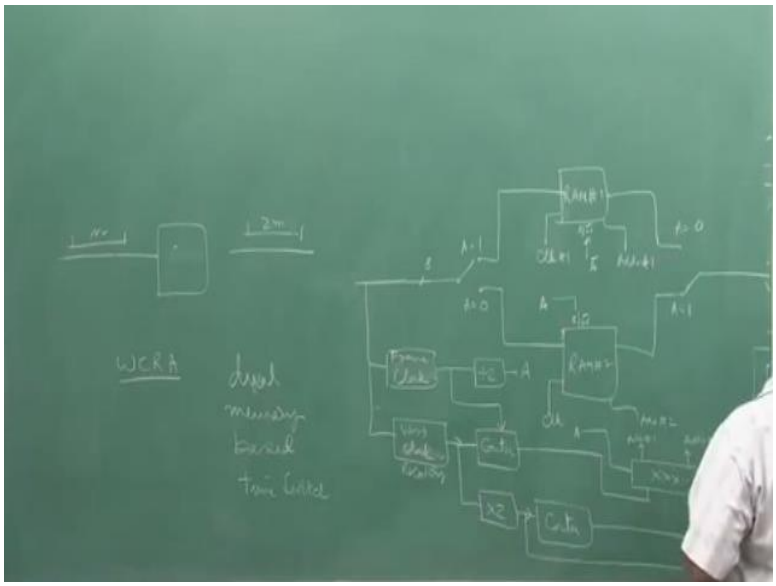

So idea is that I will have a RAM kind of thing and or whatever switch I am slots and outgoing I will now requiring 2M-1 slots but you can see there is a problem here the clock from for reading and writing from the memory has to be derived from the same source so synchronization can be maintained so normally both of these I should be able to both the clocks for reading and writing I

should be able to drive from the same source I can do that if I put it as to 2M so normally to 2M-1 kind of implementation will not be there it will be M/ 2M.

So there will be 2M-1 slots in 125microsecond frame and then it will M slots in125 microsecond frame and the clock will be driven derived from the input and I will actually do the doubling thing a doublers but to create a double rate clock for reading operation so we will be using to ram's here so let us buildup the structure we will have RAM 1 will also have a RAM 2 now in the earlier switch times which I was using only one speech RAM the reason was that in first half of the clock I was writing second half I was reading or other way around also it can be done but will force it.

But here they read is a double the rate how will do it in one clock period so not the idea is that when you are writing in one RAM you must be reading out from the second RAM at faster phase now you will not be reading all the slots remember because number of inputs are only M only M slots out of these 2M will be occupied not all of them except in case if it is a multicast if it is a point-to-point one-to-one connection then only M of these 2M will be occupied.

So other slots will go free so these will be tagged in control memory as a free slots so that you can actually use it them for routing the calls okay but some garbage we will at least will be read out even during that particular period okay so you will have a signal coming up and obviously you will be getting a serial TDMS stream okay.

So you will between paralyzed I am assuming you get a parallel stream out and you have already got the frame clock from here so this is required to reset the counters as we had done earlier there is a word clock recovery and of course you will be now using this word clock and of course you have to know toggle the first frame this has to write second frame this has to write third frame this as to you have to write here four frame and when you are writing here you must be reading here.

So alternate has to happen so I will take this frame clock and U/ 2 so I can multiply as well as divide both will be required so once I divide this will be telling whether value 0 then you will

write here when it is one you will write here when it is 2 to right here when it is three you will write here and so on so this particular clock will be used for toggling between the two control them to speech memories.

Now word clock again I will generate two forms one will be multiplied by two because you have to read out at faster rate twice the rate there is a multiplied way to multiplier and I will use a counter which will generate the address okay I am actually using here a right cyclic and read a cyclic configuration okay so I will have a switch so this will decide the value here will decide whether it will go up or down.

So this can become the input for this or this can become the input for this and this value I call as A so when A = 0 you will be writing in this RAM A = 1 you will be writing in this RAM you will also be reading actually remember so when you are writing here you must be reading from the bottom one so this should be A = 1 and this should be A = 0 so currently I think A must be one that is why this switch has been set there okay.

So I will be also using a this is the cloth one input so remember in one cycle in one frame this will be clocked with the this word clock in the second one will be clogged with double the rate and then flip over when the next frame will come this will now be driven by this clock and this will be driven by this one okay so we will actually do that so this is the clock and this will also tell this A will tell whether the read or write operation has to happen okay so if you call it RW bar here RW bar here.

So when A is one you are writing here so this leaf at by a bar okay and this will be fed by A okay so when A is one you are reading out from here and you are writing there now I also need to give the address so I have address to n I will have a MUX which will have address one and address two as out so counter will becoming all the way here so this will be driven by A and this one will go to control memory out okay so for this which I call it xxx switch so this will be cross bar state when A will be equal to 1.

Okay because when A is one counter thing has to go here so that you can write down while what has to be read out will be coming from address two which is going to come from control memory now this counter value actually you cannot pass on to this control memory you require a different counter okay so this frame clock will be used to reset here there is another counter which I will put this counter will count for twice the number if this will come from 1 to 8 this will count from 1 to 16.

Okay this is double the size actually and this counter is what I am going to use it and this is the input will be coming from the CPU which is acting as a control for this particular system, okay. And I can take this as an input to this and now this one is also because this switch is being derived by A, so this also will be controlled by A. So when A is 1 you are actually sending the reading here so the writing has to come out.

But remember there is also another problem that not only A has to be there but you also have to now ensure that you can write down into this because this will be all the time operating, so one half this will be acting reading out another half it will be you can write into this control memory so in fact I should not connect a here I will be actually using this double rate clock it shall come here.

So in the one half when the clock is positive double date clock is positive I will read out second half I can write into this but this being triggered at double the rate and it is reading all the time, okay. So only thing the flip over will happen between this so the reading signal will be going to this or this will be decided by this particular max and they have been driven by it no different clock.

This is the frame clock divided 2 and this is the word clock multiplied by 2 so there is a difference here so this is a different than the earlier times which in that sense, okay. This I think gives the complete dual memory-based time switch, now the problem is the number of times you are going to read out is twice so which locations will be read so normally whatever locations you are going to read the eight of them will be correct?

The remaining for example you can all set to zero, so out of these slots which will be coming these 2m slots only M of them will contain the exact involve actual information so wherever the information is not there as per the map it will contain information which is duplicated from one of the cells who says 0 the first one, okay. But normally what happens that this will be kept track of by the CPU or the controller.

Which but the slots are being occupied which are not occupied based on that whatever path or the mapping is decided about this particular switch it will decide what has to be written in this control memory, okay. Before I move further I have talked about time space-time switch so normally the addressing there is very important how the control memory actually operates, so I am just going to take a very small example.

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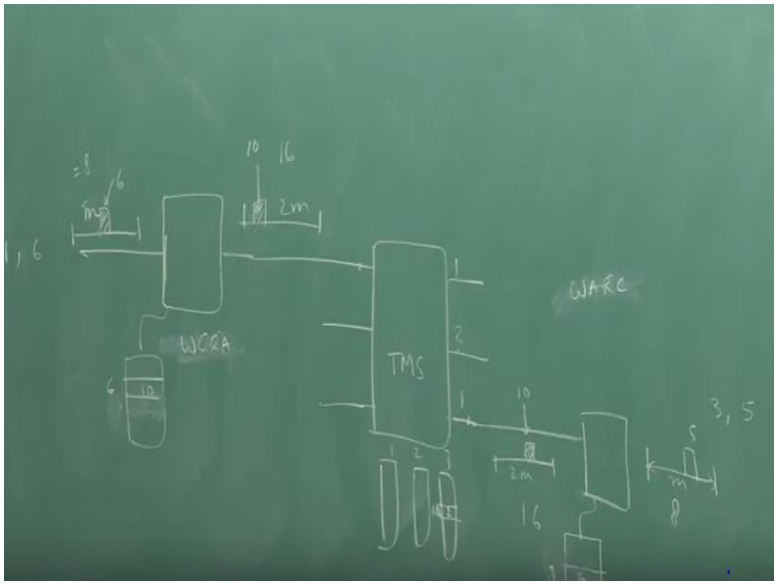

To show and then we will talk about the various properties which are required, so there is a time switch so it is m, 2m then you have a space switch is a multiple of them and then multiple outputs is a time multiplexed space switch and I can have another time switch here you will contain 2m slots and here will be M slots, now if you recall that when we were when we are talking about WCR A& WARC kind of time switches.

I have talked about a control memory of this what I am going to write in the control memory know how I should do it, so it becomes much more cleaner system, so normally if you want to have an scenario you can actually try this thing out you can take WCRA here you can try there is a control memory corresponding to each one of these outputs, okay. So you have to write something in that.

So in this case there will be three control memory corresponding to 1, 2 and 3 so you want to for example this m = 8 so this will be 16 so this will be 16 this will be 8 and this is 3/3and you want to for example take one input number one slot number six you want to map it to output number three I will put a comma here, so input number one slot six goes to output number three slot number five, how this will be done?

There are many ways so most important thing is this six slot has to map to some slot here out of this 16, so you can arbitrarily choose and map it to say n, so in that 10 slot the cross point between this and this should be snapped which will be governed by three, so the tenth lot somewhere here it has to write which particular point so it will be 1 to 3rd step so it will be saying the first cross point has to be snapped.

So this get connected to it in the tenth slot, so in the tenth lot here you will get your stuff your bite which is coming from here from the six slot, so six to ten it will be moved by this so what you will be writing in the control memory here? Remember it is a right cyclic and read a cyclic, so once it is right cyclic six must have been it in the sixth location, so in the tenth location you must be reading out reading assess the tenth location you will be reading from the sixth, okay.

And of course now you want to make it also writes cyclic and read a cyclic I am we can try out all combinations, if I do this what I need to write because I am now mapping from the tenth lot to the fifth slot here and it is right cyclic so it must have been written in the tenth location here so in the fifth location because they read a cyclic fifth location here, I need to write that I need to read out from 10.

All control memories are working in a different fashion, okay. So here I am reading a tenth here I am reading a tenth here I am reading it fifth but remember if I actually use WARC then this will get reversed, I will be now reading from the tenth location, so let us do that. If I do this I am now writing a cyclically so I must be reading out from the fifth location so in the tenth location I should write in the fifth location.

So I will actually have the address 10 and I will decide on the fifth is wonderful actually, you see every time slot is being whatever is happening in the timeslot that is governing the addresses in all the three control memories in all three stages, so whatever the input port comes here whatever the middle slot which I am using comes whatever is the cross point will be used at the 10 slot the middle slot will govern the memory location.

Where the writing has to be done is become far more simpler to handle, if you do it our way around if you want to do it in this fashion and you use it WARC here then it becomes a mess because at the sixth location you will be writing ten, a tenth location you will be writing one, at fifth location you will be writing ten locations are not same, so the main controller it has to remember that at which location what has to be done for where same connection if I use this is what exactly is being done if I use this life is cool for one cut or correction all memory locations are same.

So I can use one single address bus for all addressing all the control memory simultaneously while writing into them okay so because all these control memories have to be communicated from the central controller which will write words into this which will cause a connection to be set up out of this through this digital switch okay.

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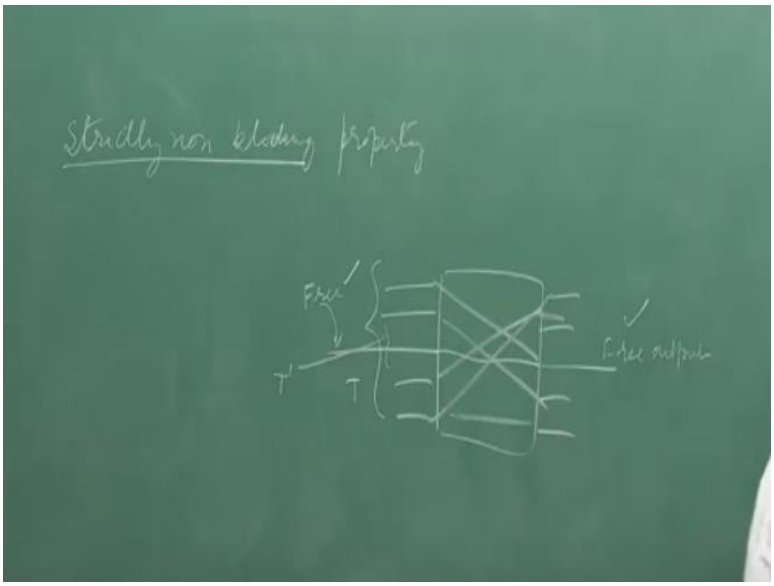

Now let us look at the various properties of the switch generally you would like to analyze all the switch properties these particular properties in any switch configuration so you are very important so first and foremost is the strictly non blocking system and you will understand that wall switches which has two non blocking is a smaller set okay and all these switches so I can keep on increasing my basically I can include this which is if I include more I can have blocking and range every non blocking and so on.

So let me define this and then this set relationship also I will explain for all these combinations now strictly non blocking switch configuration means what if i have a switch is strictly known blocking property if I have a switch I have one free input port i have one free output port then I have inputs so this can be connected in any arbitrary way I wish okay so whatever be the connection pattern in this if the fray input port is there free output port is there and I can without disturbing these connections I can always set up a path between them then the switch configuration is known as strictly non blocking.

Configurations okay so that is kind of a definition in a understanding sense we need to move more formal definition why we read a more formal definition actually remember in this case I

have only talked about one input and one output I have not included the case of multi casting multicasting means when from more input I can connect to multiple outputs okay so I need to include that so let us at the formal definition.

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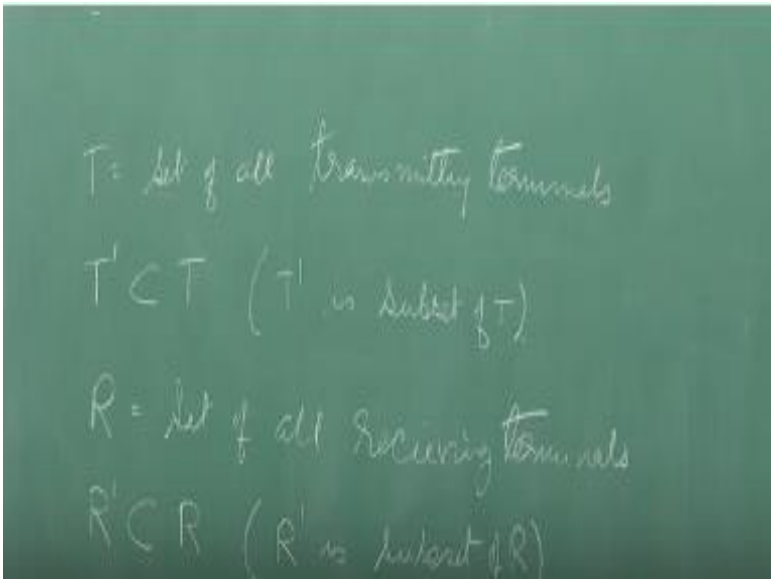

If T will be set of old transmitting terminals which are basically inputs of the switch we have some T‘ which is subset of T so which actually means this whole thing is P I can actually have some small number thing which are t prime so T’ will be subset of this can be any set okay so I can write T’ is subset of T then you have are receiving terminals or ports this corresponds to the output side and whatever is not being used any subset of this will be our prime okay so our prime is a subset of our now.

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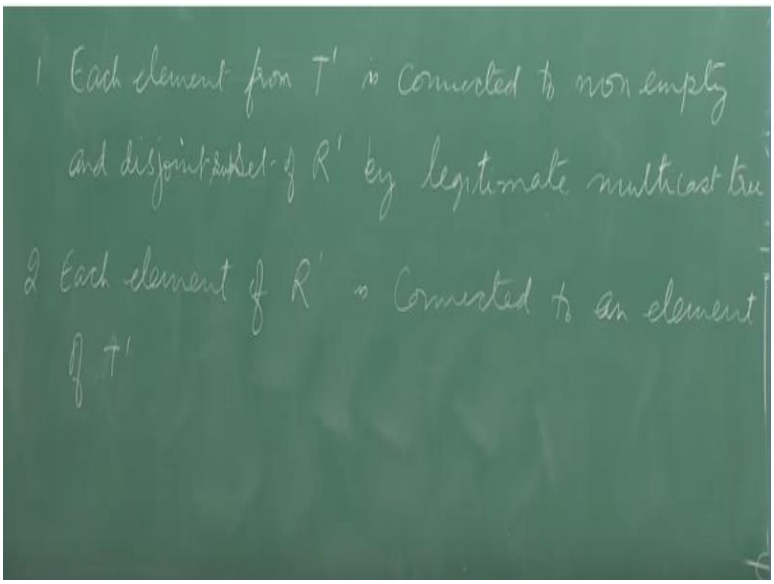

Each element from T' is connected to non empty and disjoint and i am talking about the set of output I will one element from T | of 1 port connecting to multiple ports is possible so this takes care of the multi casting scenario disjoint set of disjoint subset of our prime and we define a very important term legitimate multicast tree okay so two inputs cannot merge into an output that is important here an input can only split into multiple outputs and once it is connected to an output no other input can get connected to that particular output.

So that is a one condition second is each element of our prime is connected to an element it will only connect it to only one element it cannot be multiple of them an element of T' so basically T' is set of all input ports which are already connected R prime is set of all output ports which are already connected.

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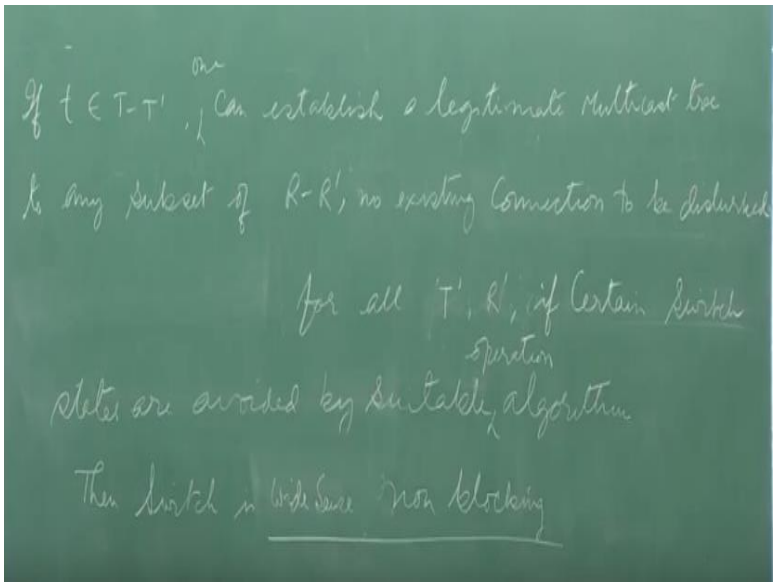

Now t which belongs to T – T' this is a free port 13 port which identifies T - T belongs to T – T' the set subset which is subset of Freeport's if t which belongs to T - T' can establish a legitimate multicast tree to any subset of r – r prime important thing here without changing previously established paths and this should be true for all possible in fact I should not write I can write all t prime R Prime and all connection patterns between P prime in our prime dense which will be strictly non blocking.

So that is a very formal definition of a strictly non blocking property and this is in terms of the multicast tree now we also actually have other definition so second one is the rearranged ability on-blocking property we will formally define these and prove that number what conditions a three-stage closed network can will become a screen on blocking we already know of that but now you will formally prove it for a unique as scenario and then for a multi-car scenario.

Now the next property is rearranged non-blocking property this will formal definition remains as it is intact except now this definition holds if T belongs to t -T prime okay one can establish a legitimate multicast tree to any subset of r - r prime maybe may require dismantling and re establishing the previously established paths and this should be true for all T prime R prime in all

connection patterns between T prime in R prime okay then switch is rearrange able non blocking okay then switch will be rearranged a non-blocking that is a second category so we call it rearranged non-blocking property .

Now the third condition is we call it white since on-blocking so let me modify the same thing itself and we call it white sense on-blocking so again same definition T prime R prime P n R and if I can want to set up one can establish if T belongs to this one can establish a legitimate multicast tree to any subset of r - r prime okay and I will not be actually dismantling in re-establishing thing I will not be disturbing any existing correction and this can be done for all T prime R prime in I will now is the important thing.

Not all connection patterns between t prime in our prime are permitted now important thing is that for example if I look at a switch a four by four I am just taking any example I can set up one two three and four to 12for example 3 and some configuration like this kind of thing this internally in the switch can be done in multiple ways not in more than one possible ways we call it a state of the switch so for this input to output map there can be multiple possible states and that is the connection pattern okay.

So I will not be using all possible states okay if certain switch states avoided by suitable algorithm so there has to be certain operation algorithm which have to be used if it is suitable enough then switch will be wide sense non-blocking switch okay.

And of course the fourth category is the blocking switch when there will be situations when input and output is free whatever you can do it will not be able to set up the connection this will be happening once in a while then it is a blocking configuration okay.

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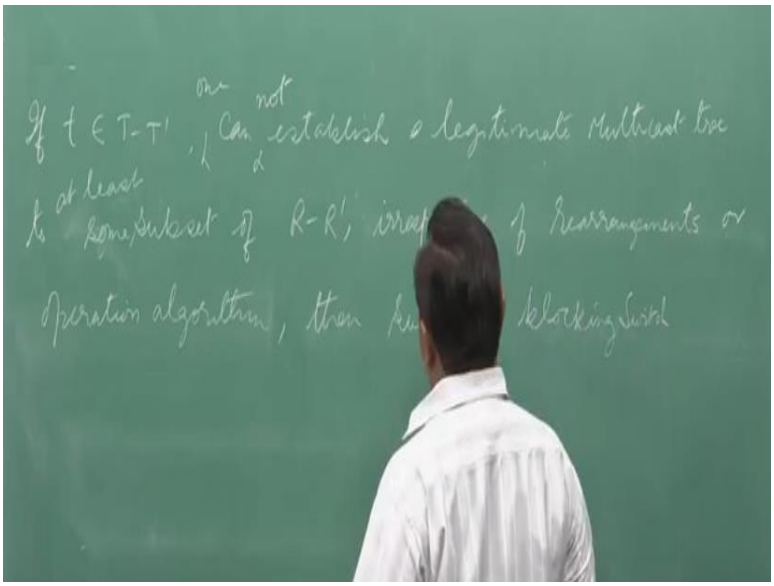

So fourth category is you cannot one cannot establish a legitimate multicast tree any subset of R1 is to say at least one subset irrespective of rearrangements or operation algorithms, then switch is blocking switch.

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