Indian Institute of Technology Kanpur

National Programme on Technology Enhanced Learning (NPTEL)

Course Title
Digital Switching

Lecture – 32

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Okay so let us continue from where we left in the previous video so we had actually done earlier the Lema one and Lema two which in fact defined that what happens in a delta network in general that also happens in a Banyan network so the assumptions which are going to make in a delta network analysis in fact we are more interested in going buffer delta analysis so assumptions will be a as follows so let me.

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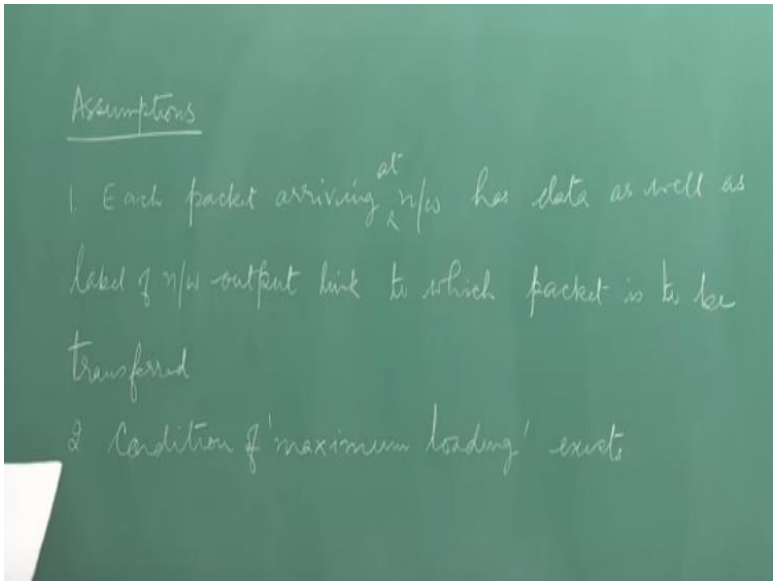

So let me list down all assumptions so assumptions number one will be that which of course is obvious but I am express to writing it that each packet arriving at the network so at the inputs actually will have as the time of course I am also assuming it also has a label which will decide to which network output it has to go it is a label identifier so mostly when the packet comes at the input there is a processor board will actually inserted tag or a label which will be use for self routing inside the switching network we defined as well as a label of network output to which packet is to be transferred.

So that is a first assumption we are also going to when we are doing this analysis we will be talking about condition of maximum loading okay so this will simplify in fact we do actually can use it but we are interested in what is a maximum loading condition and you want to compute for that condition of maximum loading exist what does it mean is that at network input links at the switch so when I talk about a switch.

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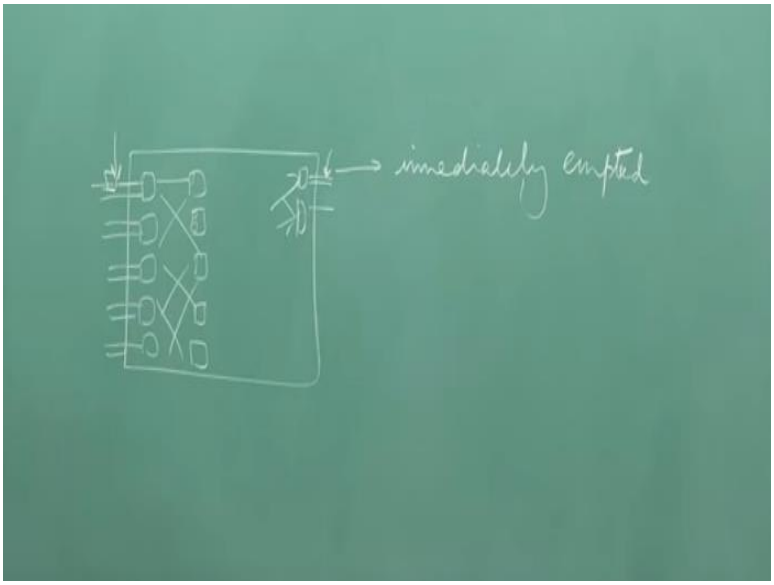

So their multiple switching elements in a buffer in the switch multiple some elements in a state and they are being inter connected okay so each one of these are also going to have a buffered thing in a buffer delta system every switch input every switching element input will have buffer

what I am saying is that this inputs will always have this switch inputs will always have a packet available the movement you push up a packet out to the next stage immediately the packet will be coming into the input that will not be any states when packet is not available so that is a maximum loading condition okay.

So probability that a packet is going to be there in a slot = 1 here condition of course if the packet moves how moves further if packet cannot be move further in the earlier packet will remain there okay so that is a condition of maximum loading so which actually implies there is a single buffer at the network input link for which implies this so there is a buffer here so which in fact is a buffer is a part of the switch filled by an input packet.

Whenever buffer is empty by the network so that is second condition which assumption which we are going to make an of course now what happens to the outgoing links whenever the packet is going to be reaching at the outgoing link it is going to the immediately empty so we need to state that also as part of the second condition so let me continue here.

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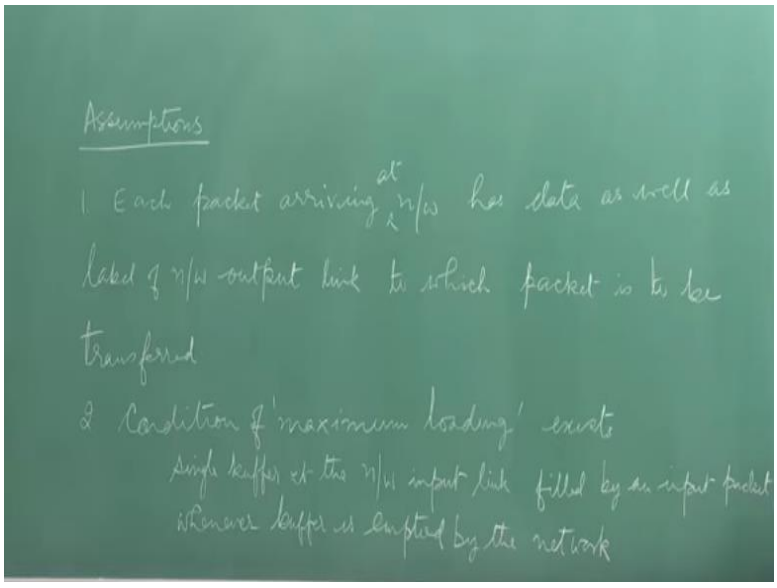

Okay so the second one continues and it says buffers at the network output links are empty is instantaneously so there is no weighting okay in fact I should write instantaneously that is assumption okay the third assumption which goes is I call it a uniform loading condition all input packets independently.

And equal probably directly to each network output link so this implies whenever the packets are coming in irrespective of which is the input they will be actually with they will be all will be independent of each other and with the equal probability they can be directed to anyone of the outgoing port so take any input output where they will actually have the same amount of traffic so that is what actually this is a independent an equal probability distribution we call it n common terms uniform loading condition.

Okay so fourth assumption which we are going to make here for this analysis model is delay at every 2/2 we are taking 2/2 cross bars at 2/2 switching elements consist of two time intervals so this is required so that I can do recursive come I can do attractive computation so depending on so we call it these two time intervals will be known as one of them is known as t pass this a time which is required so if a packet is lying here in this buffer it has to be transferred here so there is aline rate at which the packet can be transferred on to this side so we have consist of one thousand bit.

So whatever is a line rate I divide by that one thousand bytes divided by number of the bytes per second at which will transfer that will give me the time in which the whole packet will be moved out to the next stage so that transmission rate will define the t pass okay so this is the time taken time needed to pass that are to selected output so this one fragment second fragment second one will be what we call T-select, so what happens when two packets are going to come here there is a local processor inside the switching element which will analyze the tags or the labels and will identify which packets has to go to which outgoing port, now this decision making time is what we known as T-select.

So first of all when the packets are there, there will be T-select it will be decide which packet will go to which output or whether it will not go it has to be kept in the buffer and that T-select

face will be over and then T-pass will start, okay. So this is that particular time T-select is the time needed to select a switch output, okay. So in fact the minimum delay which will be encored so in first stage it will actually take T-select first T-pass.

And if there are n such stages n stages so total time in which a packet will move from input to output link in the best case when it is not going to offer in step by step it is going to move so the minimum delay which it will incur I call it min D, so this should be n x T select + T-pass, so we define this as a Min D, okay. So this will be required as a bench marking because that is the minimum delay.

So on an average whatever is a delay which is being suffered by a packet because of buffering we divide by this and we get a normalized delay actually in that case. So when there is no buffering then what is going to happen, so when there is no buffering the packet cannot be buffered packet ahs to come and it has to be routed all through in one single stage, so in fact the selection will be done here itself at the input.

Of all the packets all the stages all of them will be connected in one single go and then the packet will be transferred all the way from input to output in one single short so only delay which will be suffered by a un-buffered system will be Min D, okay. So that actually means now that is one case when we do actually the single processor has to set up everything, okay. This case that not Min D but that in that case will be T-select + T-pass.

So that is like a everything is being controlled by one single processor headers are being analyzed everything has been switched and then routed, so T-select will be required here and T-pass in one single going through which is going to be also true for a single cross bar system but if you have this kind of system and there is no buffering so packet comes here it is been selected passed out.

Packet analyzed passed out if there is a conflict packet is simply dropped, in that cases un-buffered system the packet will be requiring T-select x n Min D amount of time for reaching from input to output, so un-buffered system the minimum delay will be Min D in fact the only

delay will be Min D or infinite either packet will be delivered or it will not be delivered, okay. So but in case of a buffered system packets can get buffered.

So it will not be between two choices of either Min D or infinite it can be somewhere intermediate also, okay. So when the network is going to be buffers what you are going to do, so the fifth thing let me write it down, so that is what I where stated so fifth assumption is about this for an un-buffered delta, for network without buffering output data is delivered in Min D, so switch will be attempting to transfer the packets input packets to a corresponding output throu8gh a unique path, okay.

And if there is clash one of some of them will be actually dropped only one of them will be going to an output port the remaining will be a drop, okay. So there is no priority any one of them if there is a two packets are contai9ning at a 2/2 cross bar in intermediate stage one of them will be equal probability will be a drop actually, so that is with buffering without buffering so 6 one what happens with a buffering actually.

So here I have to give the till the paternity model which is technically can represent 2/2element with buffering, now remember I am going to do back pressure mechanism is going to be implemented when the network is with buffering if buffer is occupied here then the packet cannot move from this to this it is not possible this will also remain buffered, only it is possible if this packet gets emptied then the next packet can go in, okay.

So this if for network with buffering. So if this can be modeled as a paternity net so it is a time paternity actually so paternity is basically used for finite stage machine modeling so what is it actually means in general let me just explain what the paternity is and then I can draw the model. So here the idea is if we actually have something call.

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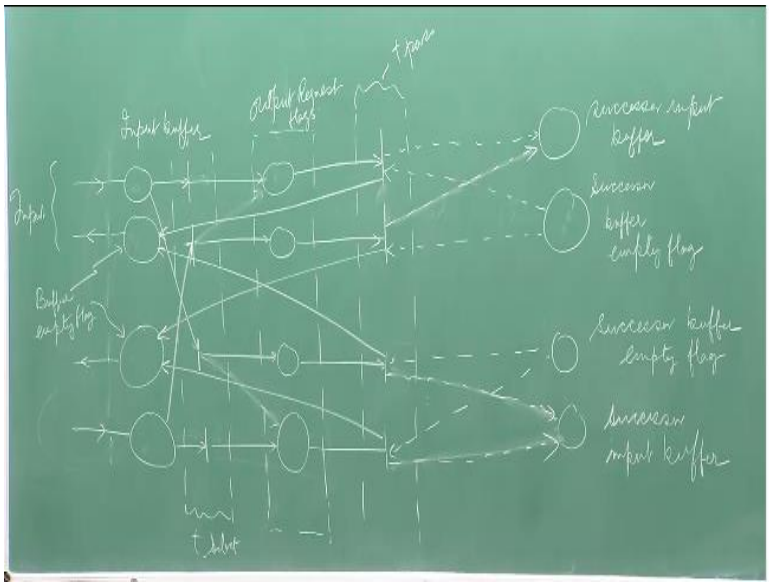

Token buffers so these tokens will be there and whenever a token is present I can trigger any event, okay. And when the event when both tokens are present in both the pre conditions the event will be triggered and this can be true tokens into one of these on a there can be another condition so when these two tokens are consumed I can actually generate two more tokens, I can generate any one of them depending on the condition which is specified on this decision threshold.

I can also put a timer so if these two are available after that it will take some time T after which only this firing will happen, thee tokens will be consumed and new tokens will get generated, okay. So essentially the idea is this thresholding mechanism or decision thresholding and the this token holding buffers and token holding buffers on the outgoing side, so using basically this element we can actually create a model for a 2 x 2 cross bar.

So let us do for 2 x 2 cross bar which is buffered that is what we are using, so we actually will have an input buffer so packet can be hold there, so this is the from one side now I am also going to inform to the previous switch whether I have the buffer is empty or not empty, so we call it a

buffer empty flag, okay. And there will be another buffer empty flag because the 2 x 2 so this is the input one.

So to whichever actually previous stage output it is connected this buffer empty flag will be giving a signal there and the packet when it will be transferred this input buffer flag will also get occupied, okay. So we will have another one which is going on this side and then there is a input buffer, okay. Not here sorry now whenever the packet is there in these two then I can come to a decision.

So this decision actually takes time T-select so this is the T-select which we have defined earlier in assumption if packet is available it will take some time T-select before it6 can make a decisions that I need to move the packet to the outgoing buffer, okay. So if this happens then I will have what we call output request flag, so the two packets which are trying to contain to the same outgoing port so there is a outgoing port 1 and outgoing port 2, then they will contain and one of then will be selected within time t select and they will end up in, so if this one is being selected then this will be empty and this will be occupied and this will remain as it is, so that it can be transmitted in the next time slot, and if this is selected this is not this will be triggered and this will get occupied this will empty this remains as it is, okay.

So similarly we will have on this side, so because this packet can go on 2 also, this side also and I will have another output request flag which will go in this fashion so one of the two. Sorry I think, I will be fitting them, okay so only one of them will get selected it will come here and then we will have the packet which ever will be selected for passing out so token comes in and there is a pre condition that there is a successor, the next switch from where we will have a successor buffer empty flag, this is basically this buffer empty flag or the next switch.

So this has to come and this has to now get, so I am putting it test line because it belongs to the next one, but it is connected here so if the buffer is empty output request flag is on, so whichever one get selected one of them will be selected at any point of time, so either this is gets occupied or this gets occupied or this or this so one of the two always will be occupied not both of them. So and the buffer empty flag is also there, in that case triggering will happen and it will cause the

packet to actually move to the next buffer so in that case this is what we call input buffer will be there which will get triggered so packet will be passed into the next buffer and this buffer empty flag has to be triggered so I will now create a link from this place, okay. So the next now switch will be knowing that they can push in the packet here.

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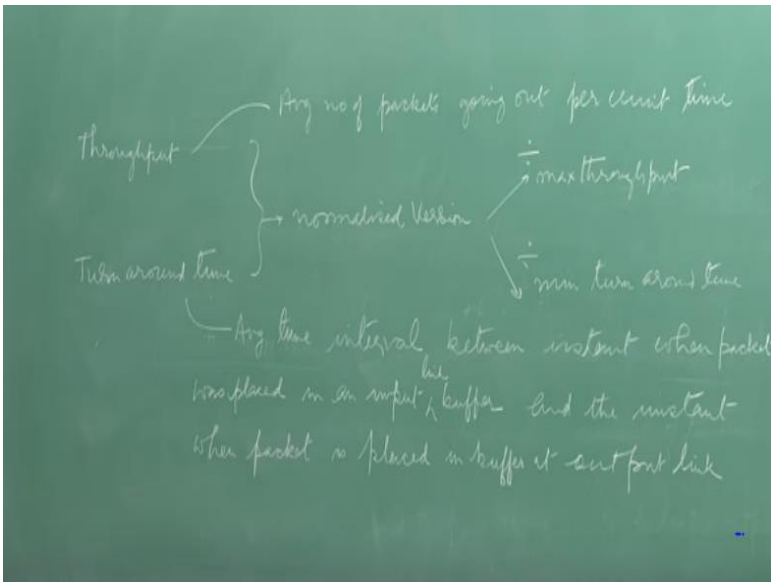

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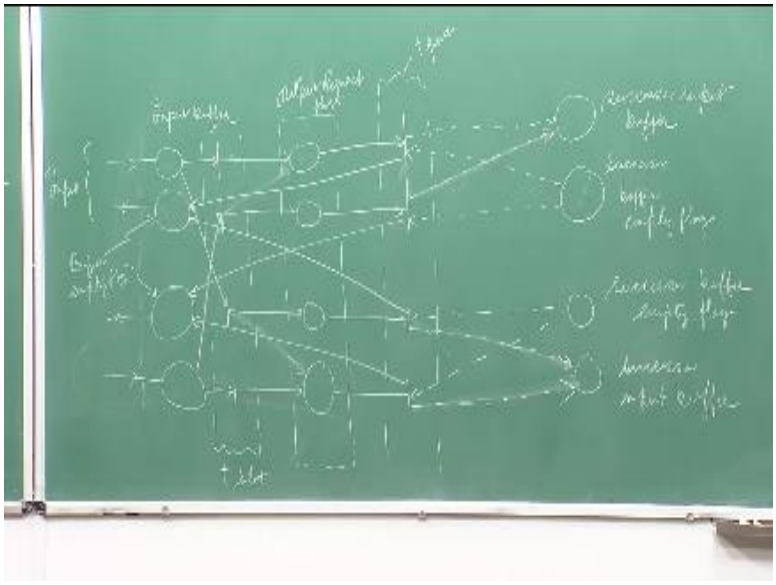

Now this will actually take time call t_{pass} so in this time the packet will be moving out from the previous buffer to the next buffer, okay so same is going to happen here, and of course if this particular thing is selected and this gets triggered because this buffer was empty in that case the actually from the lower buffer the tramp packet transfer will be happening so this buffer empty flag has to be triggered, okay. So similar logic applies on the bottom side and I will have again whichever is this can be for a different switch this can be for a different switch, remember these two are main these all four may not be belonging to the same switch, okay.

So this goes in this fashion, this also successor buffer empty flag and this is successor input buffer, this is also successor input buffer, okay so in fact know, I should keep in trash because this belongs to the next one, and if this one is selected so this input flag goes this one is selected then this input flag, so this is what will be the patternate model for the 2/2 cross bars which we are using for a buffered system, okay and remember that there is a backward back passion mechanism being maintained by this buffer empty flags, so unless a buffer is empty you cannot actually move a packet from the previous stage to the current stage.

So as the packets are being delivered at the output port side this there is going to be reverse flow of this empty flags and the more packets from the input side can be pushed into the system. So

what we will be doing is for unless purpose we will be now analyzing everything in terms of so these are the assumptions which will make for analysis.

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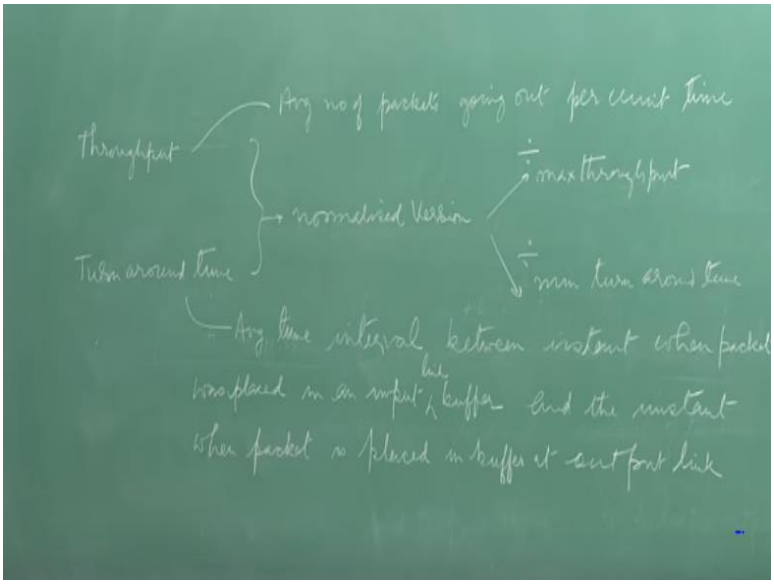

The performance criterion will be throughput and of course the turner round time, okay and we can also create the normalize versions of these, so turner round time will throughput will be the average number of packets going out per unit time, and turner round time will be average time interval between instant when packet was placed and input buffer input link buffer actually and the instant, when packet is placed in buffer at output link.

So if there is multiple stages so how many packets at the output port are going out per unit time per port that will be the throughput total switch throughput multiply, you multiply using you will find out total number of packets going out per time for the whole switch, per round time is the actually delay average delay from input to output that is what it means and we can create the normalize versions for normalize versions the upper one will be divided by the maximum throughput which is possible you divide by maximum throughput you get a normalize version for the turner round time you will find out what is the minimum turn round time which is possible you divide by that.

So which is mean d actually and then that will give you the normalize versions of these two matrix. So now what we can do is for doing for the analysis I can actually take two assumptions and under two assumptions each of these assumptions I can do the analysis, so let us do that. So one of the assumption is that in fact there is a choice about. What I do about the t select and t pass so there is a possibility I can assume that t select is 0, and then complete slot period is being go for a passing out the packet, packet does not go in one go itself, second thing is packet the whole time is required for doing the selection the packet can be transferred almost instantaneously, so in finite bit rate is there in the internal network. So t pass can be 0 so or, so one of these two can be taken and hence for we will left two models through which we can do the computation.

So t delay will now be given as so that is the one slot delay, and of course we will assume a time t=0 there is no packet in the system, and at every t delay I am going to put the packet at the input buffers, if those buffers are going to get empty if they are not empty then I will simply push them so before we come on to this particular model let me just quickly go through certain pre equators switch will give me better understanding when we will do the modeling so this I will do in form of a lama and this proof which is obvious of course. So you have to just remember what was these assumptions and from there we can decide them.

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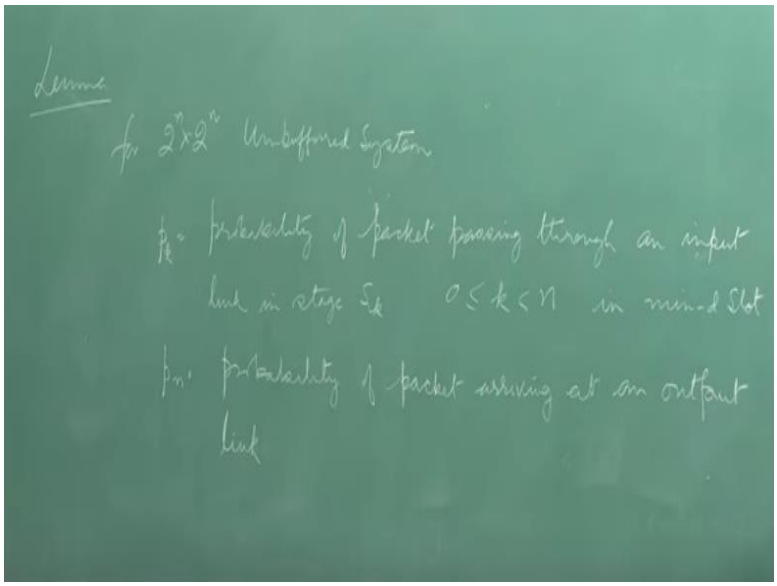

So the lama actually goes so this is the second lama you can call it lama 2 but now this is for an un buffered system I think I should do it before we move to the buffer dyestuff for $2^n/n^n$ un buffered system and with of course all the assumptions which have been taken we can define pk has probability of packet passing through an input link in this stage sk so here this actually goes from 0 to stage 2.

Because I am counting from 0 so it has to be n so I am not making equal to it is less than n and this will happen in a mind D lot okay so this I have explain why mind D lots will be required because at every inter mediate stage in delta system there is a the packet has to be hold for a small time and then transferred immediately so in fact there is no technically no buffering if there is a conflict you simply drop the packet let the earlier packets keeps on coming in.

Oaky that is a buffered system and pn be the probability of packet arriving at an output link, okay now important thing.

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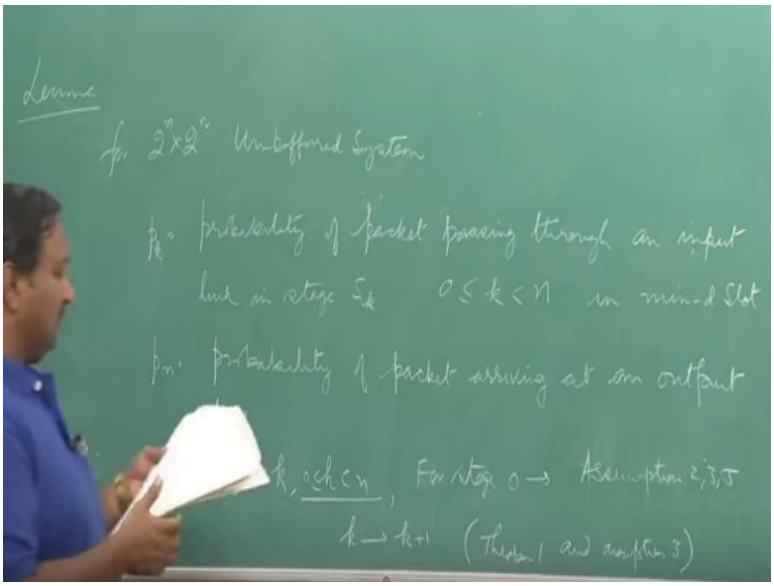

That pk for 0<k<n same for all input links in same stage so what does it mean if I have lot of switches so I estimate some pk here so this will remain same and this will be same for all links which are all input links all of them which are there to this particular stage, so pk will remain same respective of which link I choose okay, and similarly pn will be same for when look at the outgoing link in the outgoing stage.

So pn whatever you measure you take any one of these output links pn will remain same there okay so pk same for input link in the same stage pn gives going to be same or all network output links second what is going to happen is arrival of packets at an input link of a switch is independent so arrival of packet set input link of a switch is independent of arrival of packets at any other input link.

So what does actually it inter potation is if there is a switch there many input link which can be there so the arrival of a packet on this is a independent of arrival of packet on this these are independent of arrival of packet on this so all this input will be have independently there is no coordination between the packet arrivals okay. And of course for any delta network is not a set for certain a specific one pk for 0>k>n is same for all delta networks.

All delta networks of size $2^n/2^n$ so far size is same whatever be the inter connection pattern the pk value will remains same so whatever is the result is true for all kind of delta networks, so the proof actually is going to a very simple in this case this can be done so I am not doing it formal here but I am stating how this actually can be done you do it by induction so you prove it for 0 and n for 24 k = 1 okay and once if it is true for 0 it is a true for 1 we just prove if it is true for k it is going to be true for k+1 so n is for by induction it is actually true for all values of k.

So that is a way it is going to be done induction of k where k will go from 0 to n so you will actually use this so a statement is true for a stage 0 because of assumptions 2, 3, and 5 for a stage 0 it is true because of the assumptions which we have add it an earlier, 2, 3, 5, for a stage k if it is true for a stage k it is going to be true for k+1 this will come from the assumptions theorem 1 and assumption 3.

So theorem 1 which we have done earlier and assumption 3 so once you do it this actually can prove 1 and of course from there it can compute we can actually build up the theorem this in fact is the same result which we have done earlier, so we can identify theorem from here and this for all delta network actually.

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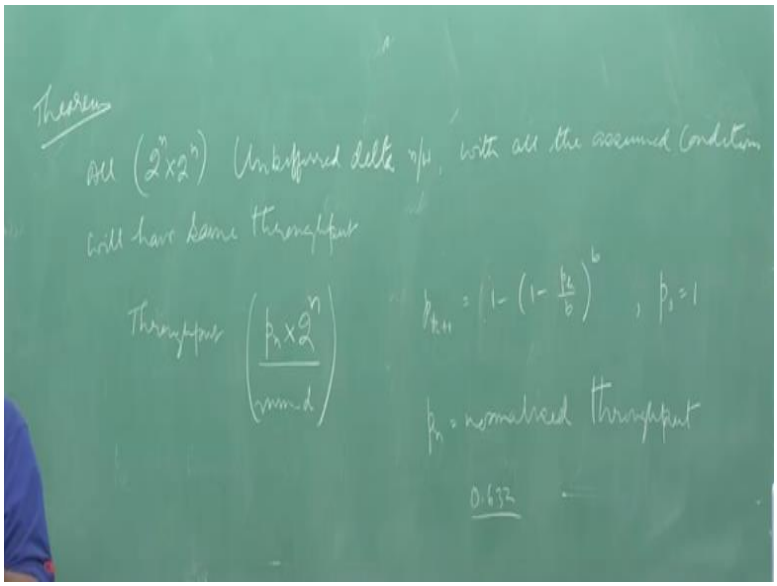

So for this is the second one I am taking about you can all it theorem 2 you says that all $2^n/2^n$ now this is for unbuffered delta with all the conditions which we have assume will have same through put so this actually through put will turn out to be nothing but p(n) total number of outgoing port is this and these packets goes out in mind D is lot okay so through put is going to be same because pn is same for all kind of switches.

Okay is that simple has that in fact we have done this analysis earlier and the result was that I can always estimate through recursion I can get pk + 1 will be coming has 1- pk /b^b k so this b is in our case will be 2 because a 2/2 network and p0 will be one we are assuming the maximum loading condition and hence forth we can compute whatever is the value of pn and we can put the value n compute the through put okay and of course the normalize through put will be whatever is the maximum possible through put so when pn is 1 there is a (max 2^n/mean D),so Pn will become the normalized throughput ,okay, so this a normalized throughput which will be there ,and of course using similar formula we had earlier done something a cross bar ,and for the maximum loading condition when P0 is 1 ,our throughput was 0.632 which we have already compute.

Okay, so let's now move to the buffered delta system analysis, as I was mentioning that the packets will be put into the system input at every T delay so

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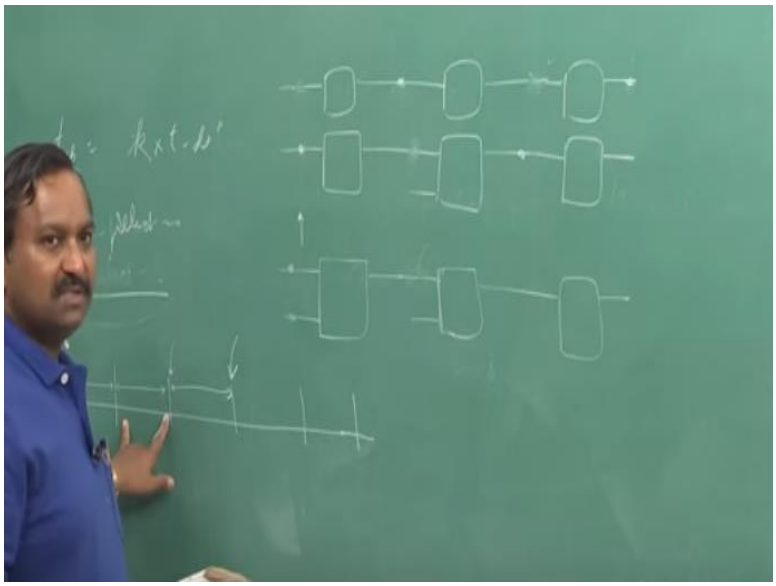

At every instant T k which is going to be K times T delay packets will be put in ,so K can take a value from 0,1,2,,3....∞ ,when the switch is operating ,and we actually can build up with a single buffer in for every intermediate switch ,I can actually build up a Marco chain and do the analysis to that, okay, that will be very comparison because you will have almost a large number of states which can be there in the switch operation.

So we will not do that we will actually use alternative trick, we will try to use minimum number of state for each switch and then we will write it, so we actually going to use the assumptions that all switches in N stages are all most same, almost similar, so let's take with first condition we will take is when T passes is 0, so packets can be transferred almost instantaneously.

But before we move I need to tell you that what's the different between T pass and T select ,what's the consequences of that so that you can appreciate ,so when T passes 0 typically a switch will be having some connection like this ,let me show you what happens ,so let's these

two packets which are there have to go here ,so this is happened at some instant, in some time slots .Each one of them is equal to T delay now T passes = 0 it actually means T select= T delay and N is plot =T delay so, selection process itself actually takes complete full slot.

And packets are transferred instantaneously, so when both packets actually arrive here it will take this whole period for the selection to happen and then the next buffer which is available here for this switch, only one of the pocket can be pushed out all most instantaneously at this point, but the packet has to be held up here because again it has to go through it selection process.

So what will happen in the next step is? Let me draw it half of this, so once we move here, so only one packet will be able to move to this outgoing packet, this buffer and this will be the situation now, and then the next complete slot will be required for again doing the selection process, by the time new packet can actually can come in will not be able to come because of K this buffer was not empty.

Now this buffer is not empty so this signal will not be coming back, remember what we have build as a patronage model unless this buffer is empty there is no use of doing any selection here, this buffer has to get emptied first, so there will not be any selection for this outgoing port in this time slot, this buffer is freeze so this will get selected and assuming that there is no contentions from bottom one, there is no contention here.

This either might be going to this second port or this is packet itself is not there one of the two conditions ,if there is going to be contention then of course one of them will be going out. So assuming this is going to go on to this side ,so at the end of the next slot this will not be selected because buffer was not empty, this can get selected and then will be this system packet this packet can move out move to the next location .So you will have this situation now ,okay.

In the third time slot the selection will be again happening here as well as here as well as here, so this buffer is empty so selection will takes place in this time slot for this the buffer is immediately being emptied out at the output port so this will be also selected,in this terms same time slot at the end of this position these will be actually now moving on to this place okay.

So there has to be a one buffer which has to be empty here then only at this thing can happen ,so this is the consequence when i am going to use T-passes equal to 0 ,when i am going to use T-select equal to 0 then how this same figure will look like ,so let's put T select is equal to 0.

Oh! I think I have made a mistake, we need not actually have let me just repeat it when T select is T passes 0 what i have done is T select =0, so unless the buffer is emptied you cannot push the packet out, so but when T passes 0 packet can move all most instantaneously, so we don't worry about the buffer being emptied or not.

So when these two are there this is empty, so in the next time slot you will actually have a packet moving on to this side, one packet here in the next time slot both of them can get selected, so this get selected to move where this get selected to move here in the next time slot this is what is going to happen, okay, so they can synchronously keep on moving further.

Okay but when we have T select =0, then this will not be happening because one of the packets get selected it is here second one is here, now you cannot move this packet on to this side till, this actually packet becomes empty then next slot, so in the next slot this packet will be transferred then this will get emptied and next to next slot this packet can move. So this packet will be, there will be intermediate stage when this goes to this location .And the next time both of them will be moving simultaneously, so that's what will happen when T select=0.

So now in order to actually simplify we need, okay we will actually continue with the next stuff in the next video where we will discuss ,how they will be actually moving from we will be using ,will be creating this time and bifurcating three separate events so that we can easily now model this hole show.

One model when T passes 0 how to model the computational procedure when T select = 0 it's for more its simpler, but for T passes =0, I need to break up this in three separate consecutive events which has to happen at every switch.

Acknowledgement

Ministry of Human Resources & Development

Prof. Satyaki Roy

Co-ordinator, NPTEL, IIT Kanpur

NPTEL Team

Sanjay Pal

Ashish Singh

Badal Pradhan

Tapobrata Das

Ram Chandra

Dilip Tripathi

Manoj Shrivastava

Padam Shukla

Sanjay Mishra

Shubham Rawat

Shikha Gupta

K. K. Mishra

Aradhana Singh

Sweta

Ashutosh Gairola

Dilip Katiyar

Sharwan

Hari Ram

Bhadra Rao

Puneet Kumar Bajpai

Lalty Dutta

Ajay Kanaujia

Shivendra Kumar Tiwari

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