MEMS & Microsystems
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Lecture No. # 12

Etch Stop Techniques and Microstructure Fabrication.

Today we will discuss on etch stop techniques and microstructure fabrication. Etch stop is a very important aspect in making microstructure. I have told you earlier that in MEMS in many cases we need membranes and flexures or cantilevers of certain thickness and that thickness varies in case of surface micromachining may be 2 micron, 3 micron in case of bulk micromachining. Sometimes we need membrane of 10 micron, 20 micron or 30 micron and thus, those 10, 20 or 30 micron is coming from the bulk thickness of the wafer which is nearly 300 to 500 micrometer depending on the wafer size. If it is a 2 inch diameter wafer, the thickness is nearly 280 to 300 micrometer. If it is a 4 inch diameter wafer, the thickness of the wafer is nearly 500 micrometer. If it is a 6 inch or 8 inch then you will get further more thickness of silicon wafer. So from that thickness it has to come down to 10, 20 or 30 micrometer. So somewhere we have to stop the etching process. Then there are two ways. One is the mechanical process, that means you observe the time, if you know the etch rate of that film basically silicon, here if you know the etch rate of silicon in that particular etching solution, then you can note down time how much time you will etch.

Then after that you take out the wafer and then you 8 inch then it is further we will get more thickness of the silicon measure the thickness you can get it. The other way is automatic stopping. So you see automatic means it will continue etching. But after certain point, that point has be has to be decided by electronically or electrically. So automatically they will stop. So out these two techniques obviously you go for the second one which is automatic. There reproducibility is more and error will be less. Because in the first method if you go for time stop time etching, basically it is known as time etching after certain time you will automatically stop it manually. So there you may do some error in stopping etch or you have to continuously monitoring the etching process. So there, lot of error may be introduced in the process. As a consequence of that, you can have different thickness wafers, different thickness membranes or flexures, etcetera. So that is why there are certain techniques I will discuss now which will give you automatic etch stop mechanism. So those are basically two kinds.

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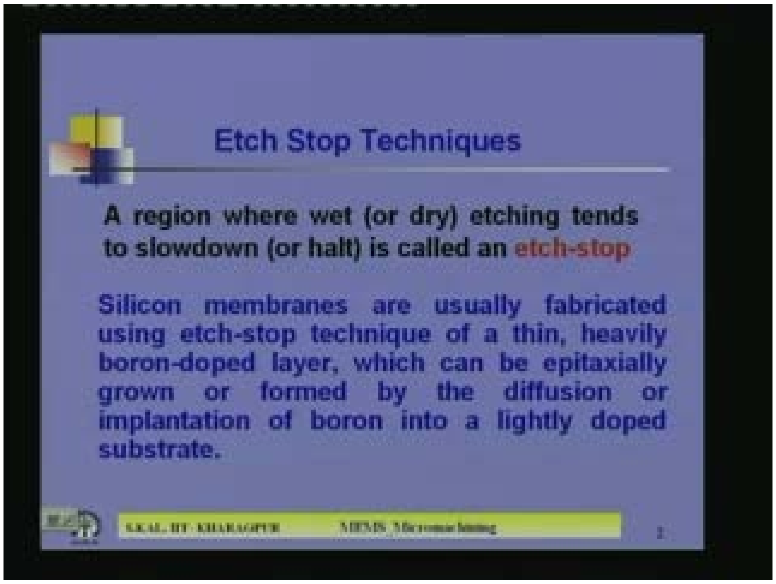

Etch Stop Techniques

A region where wet (or dry) etching tends to slowdown (or halt) is called an etch-stop

Silicon membranes are usually fabricated using etch-stop technique of a thin, heavily boron-doped layer, which can be epitaxially grown or formed by the diffusion or implantation of boron into a lightly doped substrate.

One is a bias dependant etching and doping selective etching, so that I will discuss now. Then etch stop basically which will defined as a region where wet etching or dry etching tends to slowdown or halt is called is etch stop. So it may not be completely stopped but slowdown in a drastic way so that is also called etch stop. Silicon membranes are usually fabricated using etch stop technique of a thin heavily boron doped layer which can be epitaxially grown or formed by diffusion or implantation of boron into a lightly doped substrate. You see for there it is written epitaxially grown or formed by diffusion or implantation of boron. That means the layer which is not be etched its conductivity has to be changed by diffusing boron or implanting boron to a certain limit or you can create that particular layer by epitaxially grown epitaxial technique epitaxial grown layer etch much more efficient compared to boron doping or implanted layer. Because in case of epitaxial you know the uniform growth of epitaxial layer, so that total layer thickness will be uniform to a great extent.

But if you go for diffusion or implantation, so the interface is not throughout the wafer or throughout the area of the membrane may not be at uniform depth. So there is a spread because diffusion profile you have seen is basically Gaussian profile you get it and in Gaussian profile the exact interface you will not get it. There is some kind of slow change is there from doping concentration. Isn't it? But epitaxial is soft from p type to n type of in throughout the entire area you will get from p to n or n to p soft interface you can get compared to the diffusion technique. In that way that etch stop layer if you create by epitaxially grown p-type layer then that will give you good result compared to the diffusion or diffused or implanted layer.

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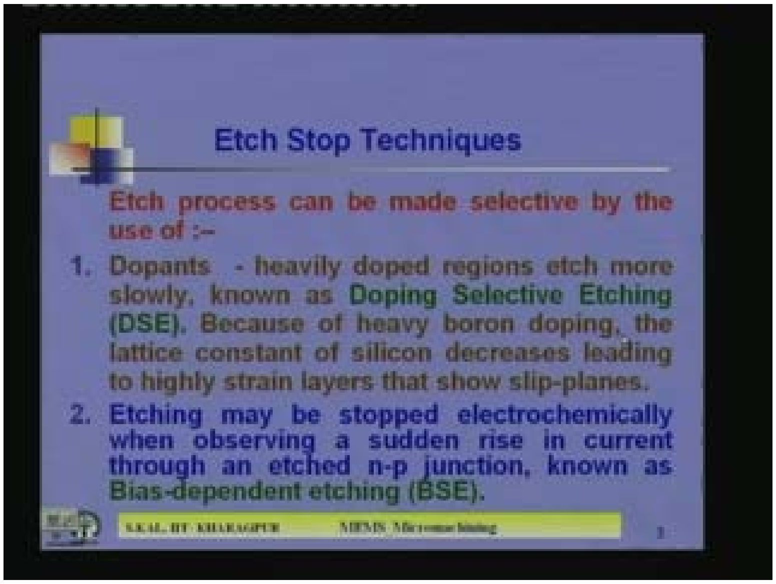

Etch Stop Techniques

Etch process can be made selective by the use of :–

1. Dopants - heavily doped regions etch more slowly, known as Doping Selective Etching (DSE). Because of heavy boron doping, the lattice constant of silicon decreases leading to highly strain layers that show slip-planes.
2. Etching may be stopped electrochemically when observing a sudden rise in current through an etched n-p junction, known as Bias-dependent etching (BSE).

Now etch process can be made selective by use of two techniques. One is known as DSE as I mentioned doping selective etching and the other one is bias dependent etching BSE. So now what is doping selective etching? In short it is known as a DSE. That is heavily doped regions etch more slowly, that is the basic principle of doping selective etching. Why heavily doped region etches more slowly? The reason is heavily boron doping, if you go doping level for boron of the order of 10 to the power 19, nearly then the lattice constant of silicon decreases. If the lattice constant of the silicon decreases, then automatically a strain will be developed inside the lattice. So the layer will be strained layer and because of that it will show some sleep planes. That is one kind of defect. So because of that introduction of strain inside the crystal, those atoms cannot be etched. That is the basic principle of the DSE, means doping selective etching and that strain or reduction of lattice constant will occur.

If you select the doping level to a certain point, that is nearly 2 or 3 into 10 to the power of 19 or something like that I will so that card and the second method is a etching may be stopped electrochemically, when observing a sudden rise in current through an etched n-p junction. That principle is known as bias dependent etching or bias selective etching. So first one is a doping, means you have to dope p-type with a certain concentration. Second one is known as electrochemical etching. So electrochemical etching basically etching will be chemical. But some electrical current is there in the etching bath and if this current suddenly rise or suddenly decreases, then some etching stop or etching start will take place. So in that case you have to have a p-n junction. PN junction the diode characteristics similar current voltage characteristic you will get. There the current will rise suddenly, then after passivating, it will stop sharply and then the etching will be also be stopped. So that is the electrochemical etching or ECE etching.

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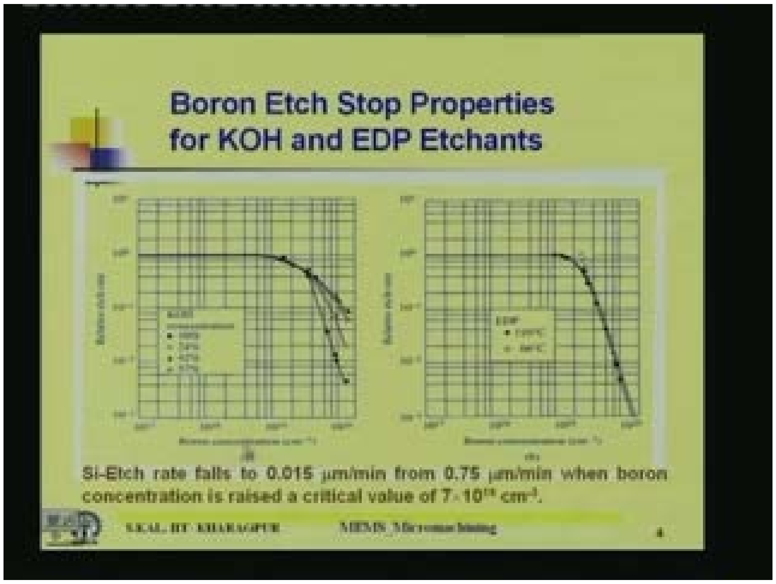

Boron Etch Stop Properties for KOH and EDP Etchants

Si-Etch rate falls to 0.015 µm/min from 0.75 µm/min when boron concentration is raised a critical value of $7 \cdot 10^{19}$ cm^{-3}.

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So here in this particular plot you can see the boron concentration and relative etch rate. The plot of relative etch rate with respect to boron concentration in case of KOH and in case of EDP, both are plotted here. So you can see that nearly 10 to the power 19 part cc if you dope boron, then silicon etch rate drastically falls. Similarly in case of EDP also, if the doping level is nearly 10 to the power 19, then it starts falling and after some time there will be no etch if it is a 10 to the power 21 or more. So this show that by proper doping of boron into silicon we can get etch stop property. It has been observed that silicon etch rate falls to 0.015 micrometer per minute from 0.75 micrometer per minute. When boron concentration is raised a critical value of 7 into 10 to the power 19 per cc. 7 into 10 to the power 19 is nearly here you can see at this point or nearly in this point. So here you can see it will reduce point seven point 0.75 micrometer per minute 0.015 micrometer per minute. That means of the order of more than one order less. So automatically there will be no etching. So this technique is used in many cases. But there are certain benefits of this technique as well as certain limitations of those techniques.

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Doping Selective Etching (DSE)

Benefits:

- High boron etch-stop are independent of crystal orientation
- Smooth surface finish
- Possibilities of fabricating released structures with arbitrary lateral geometry in a single etch step.

What are the benefits? Benefits is that, high boron etch stop are independent of crystal orientation because, if you dope the layer with high concentration of boron the reason of stopping etch is only the formation of strain inside the crystal. So that is independent of the crystal orientation. So either its layer is 1 0 0 or 1 1 1 or 1 1 0, see after that the etching automatically will stop. Second is smooth surface finish. You will get surface finished very smooth, there smooth surface finished. Third is possibilities of fabricating, a release structures with arbitrary lateral geometry in a single etch step. That means arbitrary lateral geometry, you can have some release structure which can hang using the boron etch stop layer. So these are the benefits, but there are also certain limitations of this particular technique. What are those limitations?

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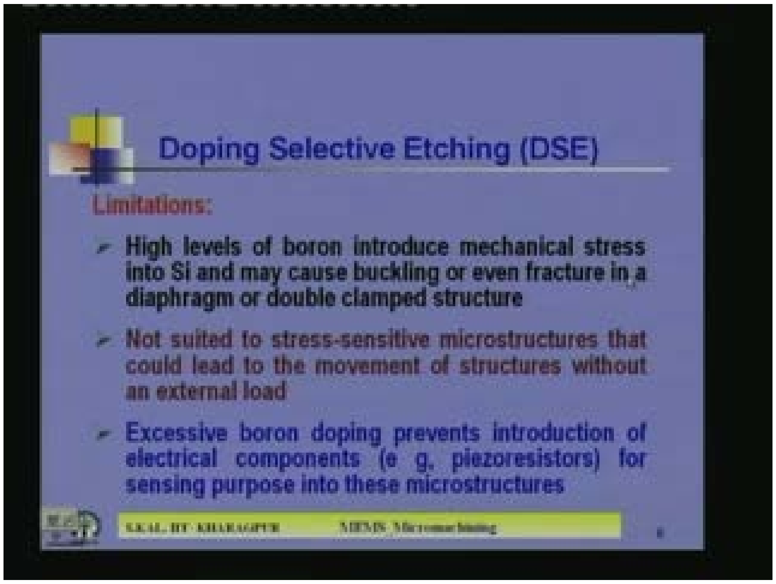

Doping Selective Etching (DSE)

Limitations:

- High levels of boron introduce mechanical stress into Si and may cause buckling or even fracture in a diaphragm or double clamped structure
- Not suited to stress-sensitive microstructures that could lead to the movement of structures without an external load
- Excessive boron doping prevents introduction of electrical components (e g, piezoresistors) for sensing purpose into these microstructures

Number one limitation is high levels of boron introduce mechanical stress into silicon and may cause buckling or even fracture in a diaphragm or double clamped structure. As a strain is developed in the layer, so then because of developing strain in some cases if you go for very thinner membrane, fracture may occur and as a result of of the strain a stress also will be developed and because of that particular membrane or the flexure, there may be a buckling effect. In some cases fracture also and fracture means that particular structure you cannot go for micro sensor. You cannot use for micro sensor. The second limitation is that it is not suited to stress sensitive microstructures that could lead to the movement of structures without an external load. If your sensor is stress sensitive then that kind of sensory cannot make using membrane which has formed by highly boron concentration doping. Because of high boron doping concentration there is a strain there. But if it is sensitive to strain your sensor, is strain sensitive sensitive then this kind of structure, this kind of technique is not normally useable.

Third limitation is that if you dope the layer with high boron concentration, in that layer is very difficult to fabricate. Some resistances which we need for piezoresistive effect or piezoresistive pressure sensor or piezoresistive accelerometer. Highly doped boron layer you cannot make resistance because whole membrane is highly doping, then you cannot get p-diffused resistance you have to go for n-diffused resistance, n-diffuse resistance piezoresistive coefficients is less compared to p. So that is why those particular layer membrane or flexure or whatever you call it, so those structure, in those structure you cannot have any circuit, small circuit or any resistances. Because they need n epilayer on p substance. But if already whole layer is doped with p, they are very difficult to make some circuits or may be some resistance you cannot fabricate. Clear. So these are the limitations of the doping selective etching. So because of that nowadays people are using some other technique.

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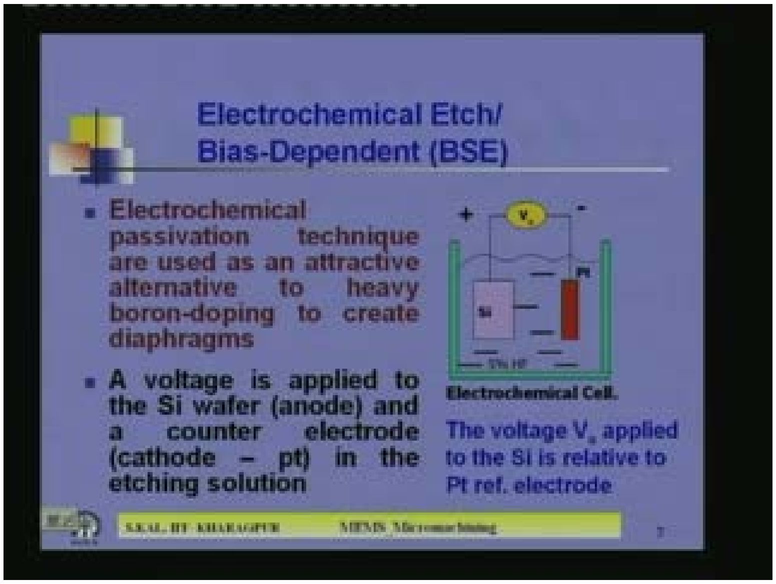

Electrochemical Etch/ Bias-Dependent (BSE)

- Electrochemical passivation technique are used as an attractive alternative to heavy boron-doping to create diaphragms
- A voltage is applied to the Si wafer (anode) and a counter electrode (cathode – pt) in the etching solution

Electrochemical Cell.

The voltage V_a applied to the Si is relative to Pt ref. electrode

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That technique is known as the ECE technique. Electrochemical etch stop technique, it’s another name is bias dependent etching or bias selective etching. Let us first discuss how the bias is going to influence the etching process. Now is an electrochemical cell the picture is shown here and in electrochemical cell, this is one should be the cathode, another will be anode. So here silicon is anode and the platinum is a cathode and you have applied a voltage V_a here. So if you apply voltage V_a and this is the hydrofolic acid solution. So this forms an electrochemical cell. Now in this particular case, we use the passivation technique and this is an attractive technique compared to the boron doping for creation of diaphragm and membrane. Then what will happen in this particular cell? If you apply the voltage V_a then that will happen. The silicon layer surface will accumulate holes in this particular region, it will accumulate holes.

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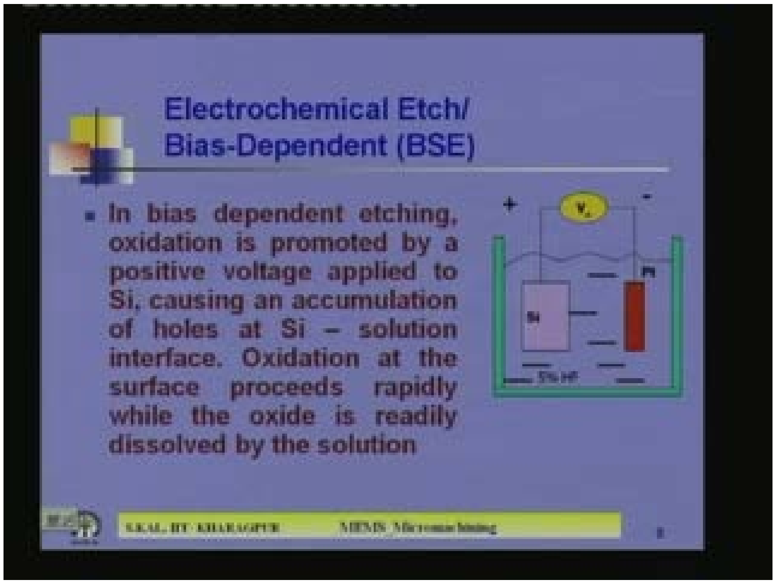

Electrochemical Etch/ Bias-Dependent (BSE)

- In bias dependent etching, oxidation is promoted by a positive voltage applied to Si, causing an accumulation of holes at Si – solution interface. Oxidation at the surface proceeds rapidly while the oxide is readily dissolved by the solution

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So if it accumulate holes, here in this particular case, so because this is positive, this negative. So positive mean it will supply holes here. See if it supply hole then as a result of which in this etch of solution if it is, this is electrode positive or negative so automatically the negatively ions which is oxygen ions tech H plus plus OH minus, so OH minus will be attractive towards that and as a result of which silicon and O minus they will form at a layer. A thin layer of the silicon dioxide and those thin layers of silicon dioxide will be etched by hydrofolic acid when it is etched. Because already holes are there in this particular region then again here the layers are coming, this O minus answer coming from a thin layer of oxide again this is etched by hydrofolic acid. So this, that means if you apply a positive voltage in the silicon it will, initially it will form an oxide and that oxide is dissolved in the solution, clear. So that means bias voltage at the silicon has some control on etching process even only silicon.

Because the hydrofolic acid will not etch silicon, it will etch silicon dioxide you know. Isn't it? Silicon dioxide so the silicon first automatically converted into layer of dielectric silicon dioxide then it is etched by etching. The normal etching etching of silicon is done in this way. So it is a bias dependent etching, means the whole process is depending on the bias. Application of positive bias voltage on the silicon. As well as how much voltage you are applying, how much holes are accumulated at the surface, it dependents on that. So that is known as the bias depending etching. But we know another always the hydrofolic acid is not never used hydrofolic acid is basically we know is an isotopic agent. It is not crystallographic dependent agent. So normal in micromachining or MEMS we use the anisotropic crystal etching which is crystallographic dependent etching that is a KOH. So now we will see how KOH etching is done using the electrochemical technique.

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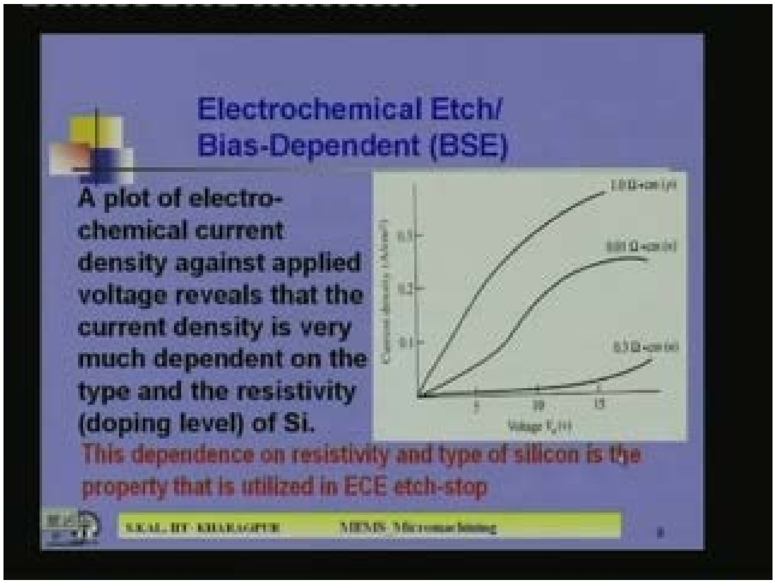

Electrochemical Etch/ Bias-Dependent (BSE)

A plot of electro-chemical current density against applied voltage reveals that the current density is very much dependent on the type and the resistivity (doping level) of Si.

This dependence on resistivity and type of silicon is the property that is utilized in ECE etch-stop

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So now the electrochemical etch in case of the KOH, we can see here. Before that let us see the voltage and current density, how it affects. Now the electrochemical current density here is plotted with the applied voltage and this particular plot it shows that current density is mass dependent on the type and the resistivity means doping level. So here you see V_a applied voltage in the last, what electrochemical cell diagram I have shown it. So there the current density is plotted ampere per centimeter square verses the applied voltage. Now you see if the voltage changes like that, current density also will change. Because whole electrolysis process deposition process are what is it is dependents on the current density in the electrochemical cell. Now if the current density increases, automatically the etch it will have strong influence of etch process and etch rate also will change.

So for p type and n type and for different doping level is a point 3 ohms centimeter and 1 ohm centimeter. 0.3 ohm centimeter means here doping level is very high, here doping level 1 ohm centimeter means doping level is relatively low. Here is 0.01 ohms n- type. So we found in the p-type the etch rate a current density with applied voltage is more compared to n type and nearly 1 ohm centimeter, it will be almost linear up to certain extent, then it gradually saturates. This effect that means from this data it is confirmed that this, since the current density is dependent on the type of the silicon wafer as well as the resistivity or on other way is a doping concentration dependent. Resistivity means it is doping concentration dependent.

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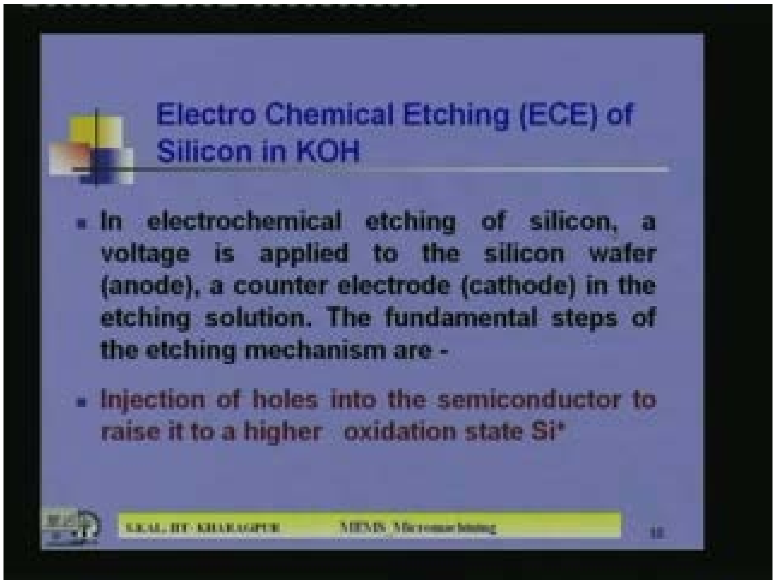

Electro Chemical Etching (ECE) of Silicon in KOH

- In electrochemical etching of silicon, a voltage is applied to the silicon wafer (anode), a counter electrode (cathode) in the etching solution. The fundamental steps of the etching mechanism are -
- Injection of holes into the semiconductor to raise it to a higher oxidation state Si^+

So that property is utilized in the electrochemical etching. That means silicon etching in KOH solution. So here if voltage is applied to the silicon wafer which is anode, a counter electrode cathode in the etching solution will be there, that is platinum electrode. The fundamental steps of the etching mechanism are mentioned here. First is injection of holes into the semiconductor to raise it to a higher oxidation state. So just I told you in case etch similar to H also. If you apply the silicon as a positive silicon with positive terminal means anode, then injection of holes will be there and the semiconductor will raise to its higher oxidation state Si plus.

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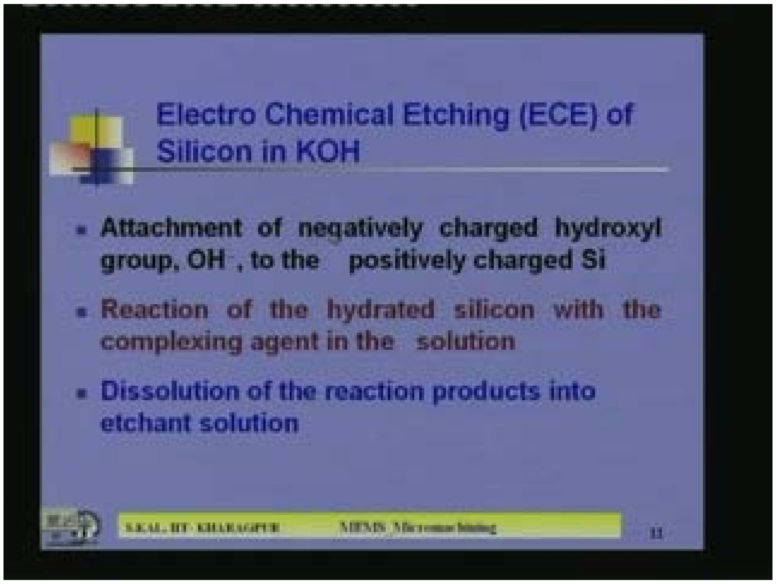

Electro Chemical Etching (ECE) of Silicon in KOH

- Attachment of negatively charged hydroxyl group, OH^-, to the positively charged Si
- Reaction of the hydrated silicon with the complexing agent in the solution
- Dissolution of the reaction products into etchant solution

So, after the attachment of negatively charged hydroxyl group OH minus, because in KOH solution K and OH, both ions are the K plus OH minus, so the negatively charged hydroxyl ion, then will be attached with the Si plus. The electrode to the positively charged silicon, reaction of the hydrated silicon with the complexing agent in the solution, then silicon OH along with the K potassium ion they will form some complexing agent and that complexing agent will dissolve into the etchant solution. That is this the whole mechanism in KOH.

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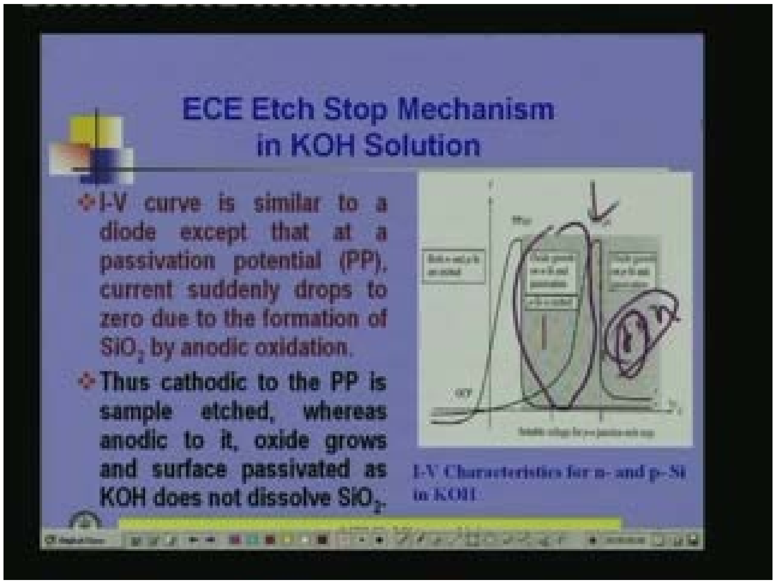

ECE Etch Stop Mechanism in KOH Solution

- I-V curve is similar to a diode except that at a passivation potential (PP), current suddenly drops to zero due to the formation of SiO_2 by anodic oxidation.
- Thus cathodic to the PP is sample etched, whereas anodic to it, oxide grows and surface passivated as KOH does not dissolve SiO_2.

I-V Characteristics for n- and p-Si in KOH

Now I told you etch stop technique, how the etch will continue, but how the etching will be stopped. So that is very important, so for that let us look into the scarp and here again IV characteristics of that electrochemical cell is plotted for n-type and p-type. Now this IV characteristics is similar to a diode except that at a passivation potential which is known as a PP. Current suddenly drops to 0 due to the formation of SiO_2 by anodic oxidation. Now you see here that the voltage, this particular, this is the reverse bias, this is the forward bias, this is the reverse bias, this is forward bias current. So after certain point if the voltage is applied here or here then we found suddenly current drops. Currently drops means in the surface of that anode obviously some dialectic layer has formed. So if dialectic layer is formed, so there is no current path. So automatically the current drops. So that dropping current drops mean it is not favoring etching.

You see one point as silicon dioxide is formed there is a direct current will be stopped. That silicon dioxide will not be etched in KOH. It is not in etch up, the first electrochemical cell which I showed you. That is an etch up solution. There what is happening, silicon is converted into silicon dioxide, that silicon dioxide is etched by agent. But KOH it is not true. Silicon dioxide cannot be etched in KOH. So if you increase the potential of IV type voltage to a value where there is a chance of formation of silicon dioxide at the surface, then that is the killing effect. Silicon dioxide form there means what happens the current density falls drastically and if the current density is not there. There is no etching because basically it is favor by the positive ion accumulated at the silicon surface and because of that OH ion along with the potassium

potassium OH and silicon, they will form a complexing agent and that complexing agent dissolves in the KOH solution.

That is the basic mechanism. But here you can see, for example this particular is a OCP, open circuit potential. Now gradually in case of this particular region both n and p silicon is etched. Now at this particular point the n type layer oxide growth on n silicon and passivation. Try to understand when you are increasing the voltage in this direction. So at the voltage reaches at that particular point, so what happened? So oxide has been formed here at that particular voltage, so because of that the oxide h or n silicon and the n silicon etching is stopped because sudden drop of the current. But in this region what has happened? P silicon is etched because here is the p that means passivation potential for n and p silicon is different. At that particular point it will stop etching of n silicon. But p silicon will continue etching. That means if you have a p-n junction so you see that the p silicon will be etching. But n silicon has been stopped etching. So that means one layer will etch other layer will not etch. So you can get the entire membrane. Isn’t it?

So here you see in this particular region, here what is shown this particular region, so here what is happening? The p silicon is the etching n has stopped. But as soon as as it reached at that point, the passivation potential of p, so they are in this line up, line you can see here. So there p also stopped, that is in this region p silicon layer converted into oxide and it has been passivated so it has been stopped. So in this region this region both p and n no etching no etching of p and n. But in this region the p will be etched p silicon is etched n has stopped here. So in that way just by adjusting the potential you can etch either p-layer or n-layer electrochemically and the p-layer and n-layer has been formed by epitaxial technique or some diffusion or implantation technique. That means you can passivate n-layer which you can passivate p-layer also. So this is one biggest advantage here.

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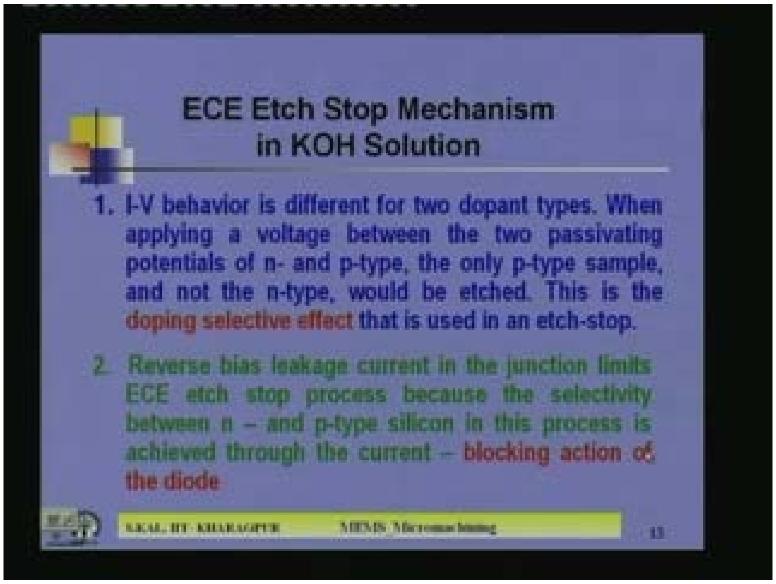

ECE Etch Stop Mechanism in KOH Solution

1. I-V behavior is different for two dopant types. When applying a voltage between the two passivating potentials of n- and p-type, the only p-type sample, and not the n-type, would be etched. This is the doping selective effect that is used in an etch-stop.
2. Reverse bias leakage current in the junction limits ECE etch stop process because the selectivity between n – and p-type silicon in this process is achieved through the current – blocking action of the diode

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Now here, so using this technique, lots of microstructures have been fabricated. So in a nutshell we can say IV behavior is different for two dopant types which are has been shown in the card.

When applying a voltage between two passivating potentials of n and p type, the only p type sample and not the n type would be etched. You remember I showed you only p type sample will be etched not the n type. This is the doping selective effect. This is known as doping selective effect that is used in an etch stop. Second point, reverse bias leakage current in the junction limits ECE etch stop process because the selectivity between n and p type silicon in this process is achieved through the current that means blocking action of the diode. That is another point so reverse leakage should be as small as possible.

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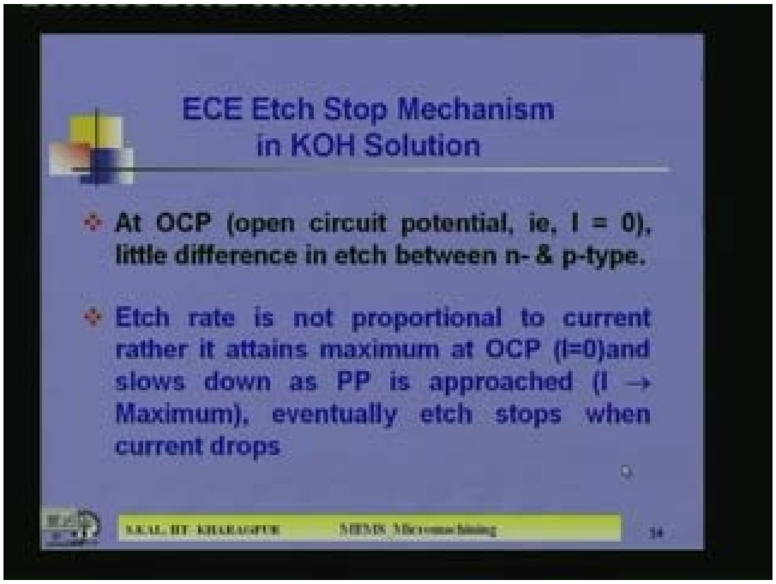

ECE Etch Stop Mechanism in KOH Solution

- **At OCP (open circuit potential, ie, I = 0), little difference in etch between n- & p-type.**
- **Etch rate is not proportional to current rather it attains maximum at OCP (I=0)and slows down as PP is approached (I → Maximum), eventually etch stops when current drops**

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Now next is at OCP which is open circuit potential. There I equal to 0 little difference in etches between n and p obviously, so at open circuit potential where current is 0 there. So there is almost no difference of etching between n and p. Etch rate is not proportional to the current rather it attains maximum at OCP I equal to 0 and slows down as PP is approached I is maximum eventually etch stops when current drops.

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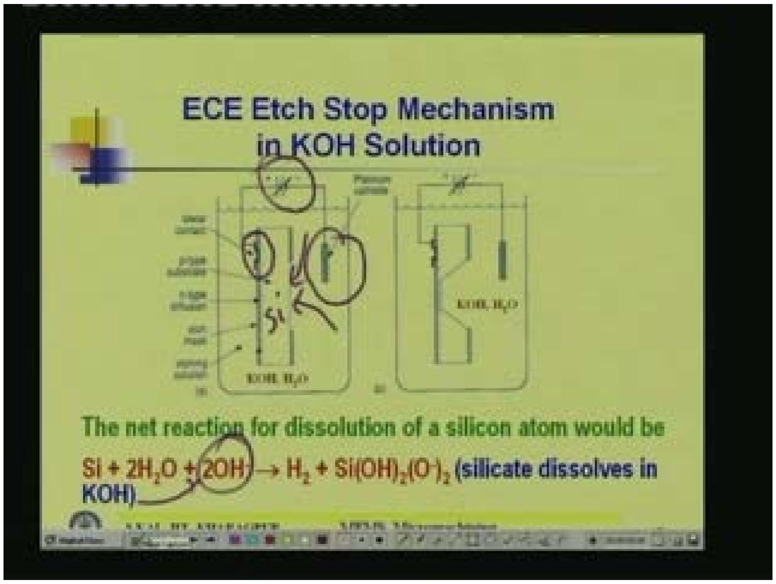

ECE Etch Stop Mechanism in KOH Solution

The net reaction for dissolution of a silicon atom would be

$Si + 2H_2O + 2OH^- \rightarrow H_2 + Si(OH)_2(O^-)_2$ (silicate dissolves in KOH)

Now this, some kind of the reaction what is taking place? This is etch stop mechanism, this is a basically platinum electrode you can see here this is a platinum electrode here and this is the anode and here the problem is the silicon which you etched that has to be a you make a contact. There is I have another problem, ohmic contact. Because if you apply potential to the silicon, this is basically silicon, if you apply the potential to silicon so you have ohmic contact has to be there. So before starting the etching process you have to make a contact which has been formed here in this particular region metal contact. So now is a positive here, so negative is the platinum. So this is the p type this is the n layer this n diffuse layered this region is a n diffused layer. So now p will be etched from that side p will be etched from that side and it will take the form like that.

As soon as the p and n type so n will be stopped because I have soon if we apply the potential in a certain value n type will not be etched. But p type will etch you select that potential. Then it will continue etching the p type. So as result of which when it reaches the end it will automatically stop. In that way you can easily make a thin membrane of control thickness and that will be decided by the n layer which has been formed epitaxially or implanted or diffused it. Diffusion process net reaction for dissolution of silicon atom would be like this. Silicon plus 2H plus 2 minus H2 plus SiOH volt wise O_2 minus. This silicate dissolves in KOH. This OH minus is basically coming from the KOH KOH wise. This is the total reaction process.

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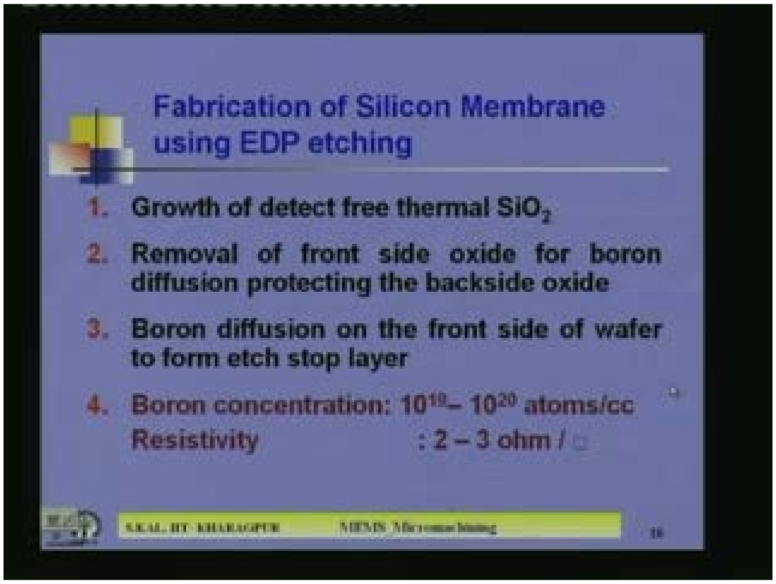

Fabrication of Silicon Membrane using EDP etching

1. Growth of detect free thermal SiO_2
2. Removal of front side oxide for boron diffusion protecting the backside oxide
3. Boron diffusion on the front side of wafer to form etch stop layer
4. Boron concentration: 10^{19}– 10^{20} atoms/cc
   Resistivity : 2 – 3 ohm / □

So now next is the silicon membrane fabrication using EDP etching. Now I will discuss little bit on fabrication of the microstructures. So how do we proceed? What are the steps? First the growths of defect free thermal silicon dioxide. The thermal silicone dioxide will act as a masking material. A removal of front side oxide for boron diffusion protecting the back side etching. So that is, in this technique we are going to use the not EC but the doping selective etching. So highly doped boron layer will not etch. So that principle is used here. So that is why first you have to go for lithography and open windows and there you diffuse the boron atom to get a highly doped region boron diffusion on the front side of the wafer to form etch stop layer. Boron concentration 7 to 10 to power of 19. So that is why I wrote it 10 to the power 19 to 10 to the power 20 atom per cc and in that doping level the resistivity will be 2 to 3 ohm per square. So that is resistivity in that doping concentration.

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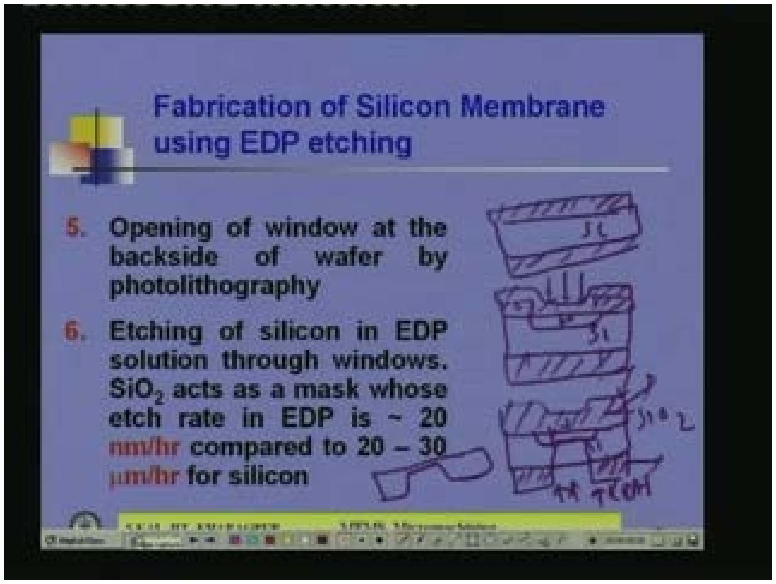

Fabrication of Silicon Membrane using EDP etching

5. Opening of window at the backside of wafer by photolithography
6. Etching of silicon in EDP solution through windows. SiO_2 acts as a mask whose etch rate in EDP is ~ 20 nm/hr compared to 20 – 30 µm/hr for silicon

Now next step is opening of window at back side of wafer by photolithography. Front side, you have diffuse boron. First you do photolithography for the front side, open windows and diffuse boron, diffuse layer will be formed. That mean here if you structure is like that, so that means initially it will be oxide here. See oxide layer is formed like that. Now go for front side lithography, then what will happen? After front side lithography you will get this like this. Then you diffuse boron. So if boron is diffused like here. Then when after p diffusion then you go for driving. During the driving again a thin layer or oxide will formed here. That means this is completely covered, this is oxide. Now you go for back side lithography. When you do for back, go for back side lithography, then it is to be aligned from the front side also. Because you have to open window here from this region to this region. So you have to know from the back side where p plus region is there. After that alignment then you open window here, that mean total thing will be like that now. So you open window here, this is silicon, this is silicon, this is silicon.

Now from here you can just etch, this is a KOH. KOH so you can etch here so that it will because here is a diffused layer. This diffused layer p plus is here. So it will etch here. So it will ultimately etch here and then you will get, then you remove the whole thing. Whole thing oxide is removed, this is removed. So ultimately what you will get? You will get like that. So this is the ultimate and this will be the membrane. Isn't it? So here you can use the EDP etching, etching of silicon in EDP solution through windows. This window SiO_2 acts as a mask. This SiO_2 will act as a mask whose etch rate in EDP is nearly 20 nanometer per hour. This oxide, it is 20 nanometer per hour. Compared to 20 to 30 micron per hour for silicon, so here it will etch 20 to 30 micron per hour. But here the silicon dioxide with 20 nanometer per hour, high selectivity of a silicon dioxide, so in this way you can get the membrane.

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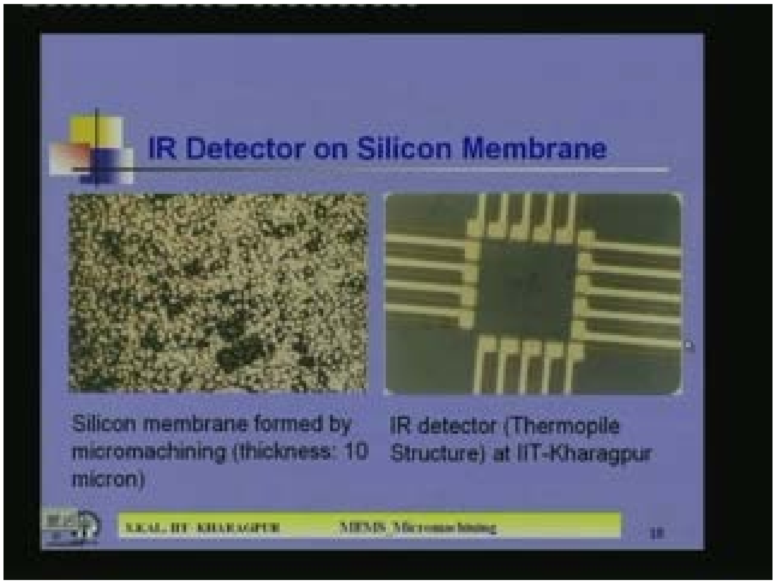

IR Detector on Silicon Membrane

Silicon membrane formed by micromachining (thickness: 10 micron)

IR detector (Thermopile Structure) at IIT-Kharagpur

Now next is using that process we have made some IR detector in our laboratory. What is that you see this picture from the back side, the membrane after etching, the black region here, this portion, this portion or this portion is may be some etch pits. You can see some colored blue colored portion the etch pit. So as a whole the back side SEM micrograph of the membrane is this one. Front side it looks like this, front side is the silicon. The silicon on silicon silicon dioxide is there as I showed in earlier view graph silicon dioxide. On silicon dioxide what we have done we have made some thermocouple. You see the white regions are basically aluminum and the radius line is polycrystalline silicon, doped poly silicon. So that means doped poly silicon and aluminum they will form a junction. Isn't it? Is a thermocouple basically about 19 junctions are formed. You know the D junction of two material will form, if you connect together it will form a thermoelectric junction and that will it temperature difference is there.

So it will form, it will develop the thermo EMF. Isn't it? And that is basically a sensing mechanism for temperature measurement. So now that means there you have to have 2 junctions; one is the cold and there is a hot junction. So this particular the junction which is connected serially, so that total thermo EMF or EMF produced because of the temperature difference it will be added together. Because if you add serially, so 13 or 14 or 19 or 20 junctions together, so total voltage produced will be more. So that the sensibility will be high. So that is known as a thermopile. In single junction is known as thermocouple. If you go on in series connection of the thermocouples, then it is known as thermopile. You are piling up numbers of junction. Isn't it? So in the thermopile total output voltage will be more compared to a single junction. Now this particular junction is formed on the membrane and cold junction is another junction has to be there.

Because for thermocouple you need to 2 junctions; one is hot junction another is cold junction. The cold junction is formed on the rim where thickness is 250 or 500 micrometer. As a result of which where there is a membrane, so the absorption of and on the top of the membrane, here we put some absorbing material, that is a black material which can absorb the radiation. So automatically here the thermal mass is less, so quickly the heat will be absorbed in this particular location. As a result of which here this particular junction will be hot and other junction will be cold because that will because thermal mass is more there. Transfer of heat into the junction will be less so temperature difference will be there. As a result of which we will get the thermo EMF. So that is the basic principle of infrared detector. So infrared radiation is absorbed in the junction, then you will get therm. This is this kind of the detector can easily be formed using the the micromachining technology using the on top of the silicon membrane.

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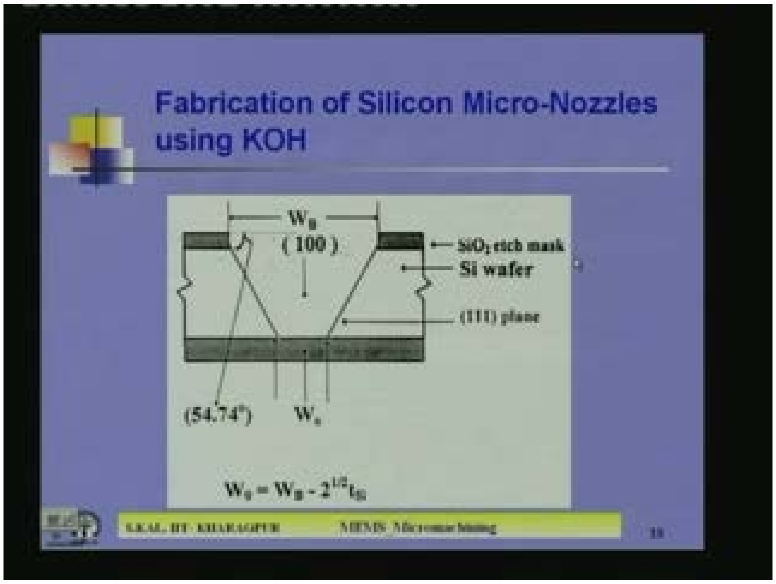

Fabrication of Silicon Micro-Nozzles using KOH

$W_0 = W_B - 2^{1/2}t_{Si}$

Now I will discuss on my fabrication on micro nozzles using KOH. So this picture I have shown you earlier. So this is the silicon dioxide, etch mask and this is silicon wafer and this is again oxide. Now you window here depending on that, this is the relation W_0 equal to WB minus root under root t tSi, tSi is the thickness of the silicon. Now you see this is the WB the W_0. This is the 54.74 degree. Now depending on the WB the W_0 can be decided. So that slanting surface is one 1 1 1 plane. So in this way you can mask design, the mask mask opening and if you make an area of that mask, so automatically it will be etched. But here etch stop is where silicon dioxide. You are not going to create silicon membrane you want to have through hole so complete silicon can be etched. After that the silicon dioxide and silicon dioxide easily you can see this silicon and silicon dioxide easily you can remove it and then if you remove it so complete the hole will be formed here. Isn't it? So in that way if you make an array and if you etch like that you can have an array of micro nozzle.

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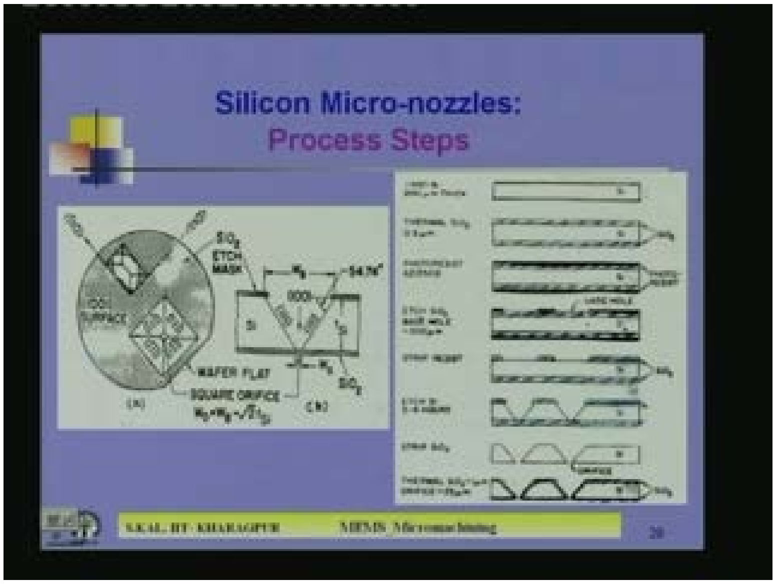

Silicon Micro-nozzles:
Process Steps

So here is the process step. This picture is shown again. So now here you can, this is a the same relation is shown here is W_0 equal to WB minus under root 2 tSi, tSi is the thickness of the silicon layer. Now what are the steps? Silicon you oxide meet oxide both side then about 0.5 micrometer silicon dioxide has been formed here. After that, using photoresist coating, then go for the front side lithography opening of here. This particular in the centre portion, then the oxide is removed you are getting window. Here you are getting window here, this porion and this portion then go for etching of silicon. You can go for etching of silicon here and here and here. Then you can get the v group and if further etches it will end of with the holes. Now this silicon dioxide and silicon dioxide from top and bottom are removed. Then you are getting whole here orifice here orifice. So you were basically, if you want to passivate this particular, again silicon dioxide 1 micrometer is a grown here. So that, this whole thing is covered with silicon dioxide dielectric layer so you are getting the holes.

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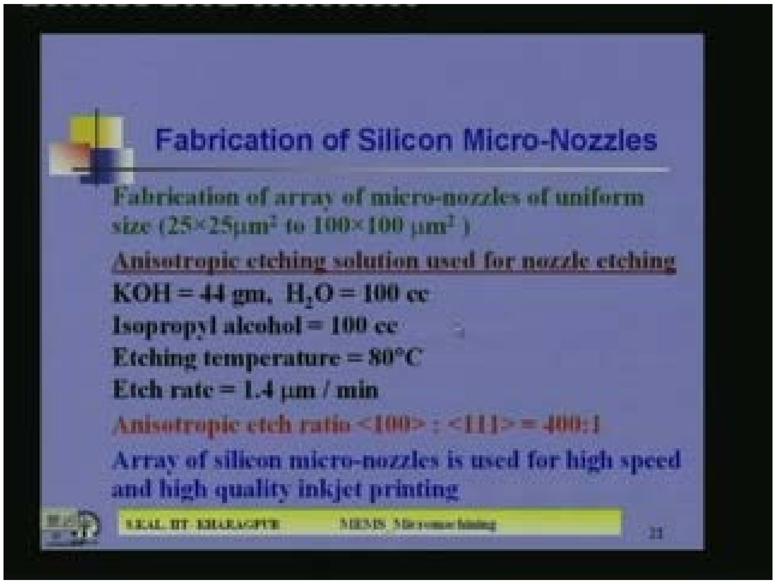

Fabrication of Silicon Micro-Nozzles

Fabrication of array of micro-nozzles of uniform size (25×25µm² to 100×100 µm²)

Anisotropic etching solution used for nozzle etching

KOH = 44 gm, H_2O = 100 cc

Isopropyl alcohol = 100 cc

Etching temperature = 80°C

Etch rate = 1.4 µm / min

Anisotropic etch ratio <100> : <111> = 400:1

Array of silicon micro-nozzles is used for high speed and high quality inkjet printing

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So you will get, for micro nozzle, the chemical etching composition you have used in the laboratory are like that. The size varies from 25 by 25 square to 100 microns by 100 microns square. Anisotropic etching solution used for nozzle etching is this one. KOH 44 gram, H_2O 100cc, isopropyl alcohol 100cc, etching temperature is 80 degree centigrade to etching. Etch rate is 1.4 micrometer per minute. That is the laboratory test result which we did in our laboratory. Anisotropic etch ratio 1 0 0 and 1 1 1 is 400 is to 1. So that is why you are getting this slant surface 1 1 1 will not be etched and the 1 0 0 will be etched and array of silicon micro nozzles is used for high speed and high quality inkjet printing is one of its application.

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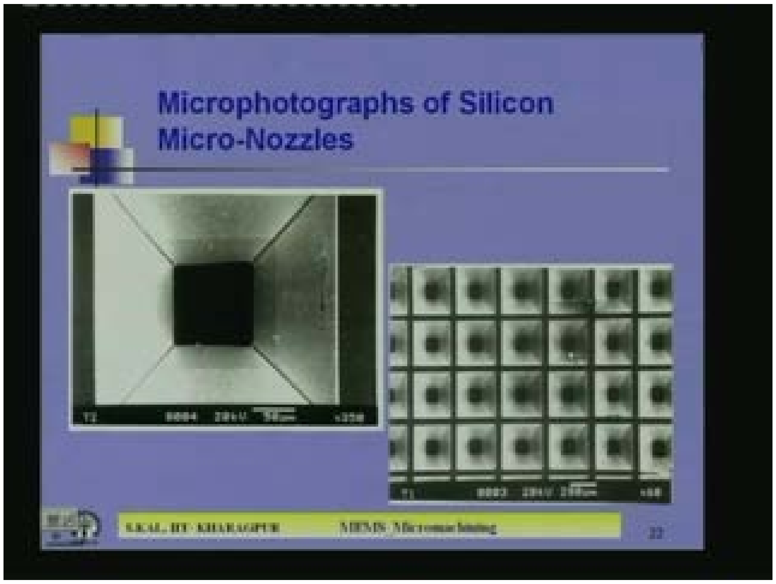

Microphotographs of Silicon Micro-Nozzles

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Now this is the picture, a same photomicrograph of the single nozzle is here that is basically fabricated in all laboratories. In all laboratory you can made, you can see the whole size. This is the 2200 micron. So is basically nearly 50 micron by 50 micron, nearly the whole size here. The area of whole size will form and that is applied in high quality, high speed inkjet printing and other application you can use those nozzles for any short of the dispenser, perfume dispenser you can use these kinds of the micro nozzles.

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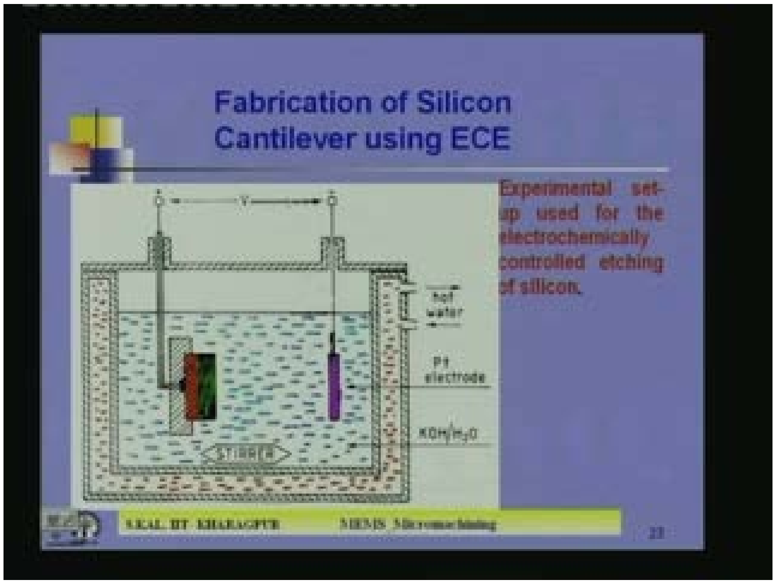

Fabrication of Silicon Cantilever using ECE

Experimental set-up used for the electrochemically controlled etching of silicon.

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So next I will show you then EC etch setter ECE electrochemical etching setter. So this is one electrochemical etching setter and basically this is the KOH solution on starting arrangement will be there magnetic siren so that you can continuously agitate the liquid for uniform etching and this is the platinum electrode, this is a negative this is a silicon has to be n and p junction and that is a positive you apply. The V_a potential, the passivation potential we apply, that is nearly 0.6 to 0.7 volt nearly. So now contact has been made here and the end layer has been protected here by insulating layer and this is the p side, so it will etch from p side and here another arrangement has been made here for hot water circulation. So that the etch bath can be kept at a constant temperature. I told you in earlier nozzle fabrication there, that etching has been done at 80 degree centigrade. So you have to heat that complete the chamber. So if you heat the complete chamber so you have to have an arrangement of uniform heating. So for that hot water circulation is we have used it and continuously agitating the inside KOH solution KOH plus $H_{2.}$ So that uniform temperature ,the etching will start and it will etch p type and as soon as they reach n type so etching will be stopped. So that is the silicon cantilever can be made using this ECE etching.

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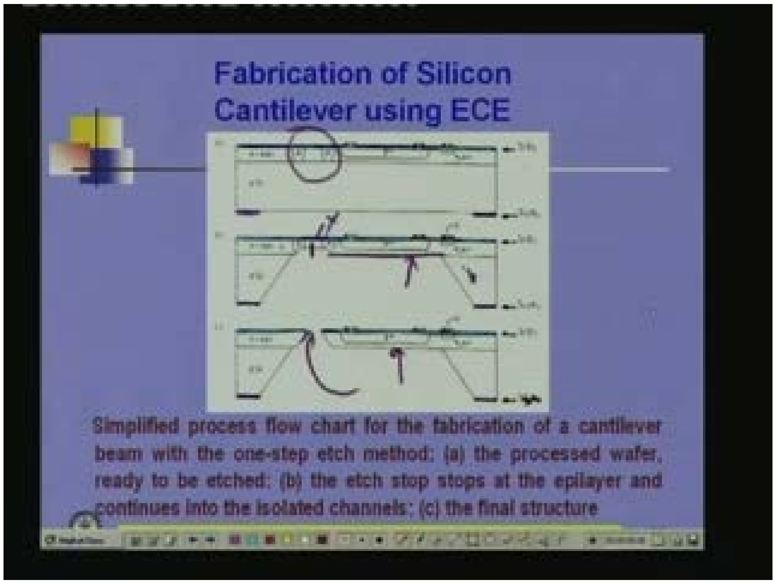

Fabrication of Silicon Cantilever using ECE

Simplified process flow chart for the fabrication of a cantilever beam with the one-step etch method: (a) the processed wafer, ready to be etched: (b) the etch stop stops at the epilayer and continues into the isolated channels: (c) the final structure

I will show you know the process steps how it has been done. Now you can see here, so step by step how it has been done. First this is the silicon p silicon wafer is n epilayer. Normally in case of any of the IC fabrication we use n on p silicon wafer is the conventional. Because in n layer we make all the devices. Now here you see the p layer has been p is diffused here. This p-n-p is isolation diffusion. Here you see, you are not making membrane, you are making cantilever. What is the different between membrane and cantilever? The difference in cantilever in somewhere it will be stopped and somewhere through hole will be there so that total structure will hang. Isn't it? Wherever the through hole, so there is no connection between the frame and that thin membrane. So that is in membrane or diaphragm there is no through hole in any of the side places. But in cantilever or flexures you have to have some places through hole.

That means you have to have the passivation selectively. You will see how intelligently this can be achieved in this kind of structure. So here for that region this p-n-p diffusion is isolation diffusion has moment. I mean this particular region where you need a through hole, we have isolated that particular region by the isolation diffusion. Then here n plus is diffused for taking contact. Because in ECE etching I have to apply certain potential that potential is a passivation potential I have to apply there. So for that one contact has been formed and this p plus diffused here and the end layer is a below. Now after that you go the silicon nitrate masking layer is from the bottom silicon dioxide at the top. Now the contact potential is applied through that contact with respect to the substrate. Then what is happening you see from the back side it is the etching. Now as soon as this particular etching will reach at that particular point, then what is happening?

You see here this particular, here is a p and here is n. So in that case the passivation potential it is getting. So automatically etch stop but what about here? In this particular location will it bias? No. Because it is isolated by p-n-p, this particular region will form if you apply plus V here that plus V will not be applied here. Because this p and n will be a junction, this p and n will be a junction. But in this particular region there is no junction. Because this particular region has not biased. So that is basically isolated region. If it is isolated, so etching will continue in this particular location but here, this particular region is biased. So here stop it cannot go further but this particular location. No bias, so etch it will through etch, so that you can get, this is a cross sectional view you can get easily. This cantilever, so this is some of cantilever for that you took an extra pain. What is that? You have to have the isolation diffusion, have to have the isolation diffusion. Now in this way you can make the cantilever beam by using ECE etching.

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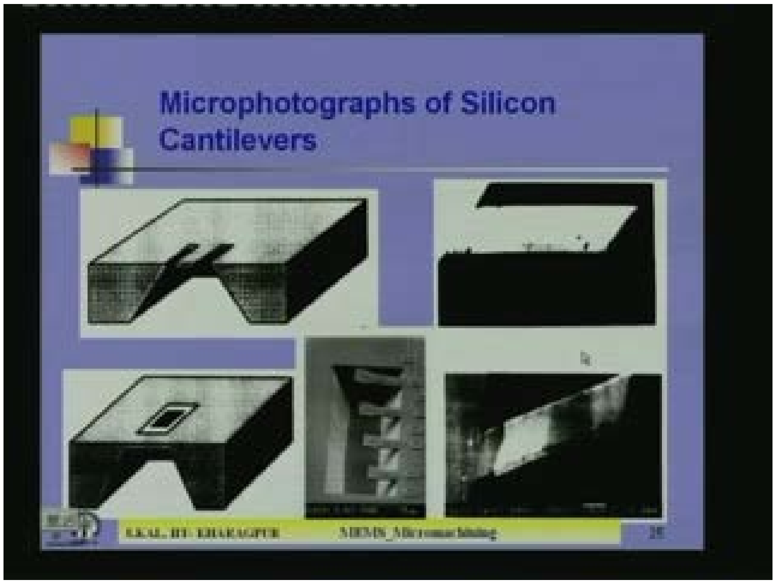

Microphotographs of Silicon Cantilevers

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Now, so these are the some pictures, viewgraphs of the cantilevers formed using the ECE etching, microphotographs. So this is one cantilever, this is one, this is the 3D view is there. So here thorough hole has been made, so some structure has been made.

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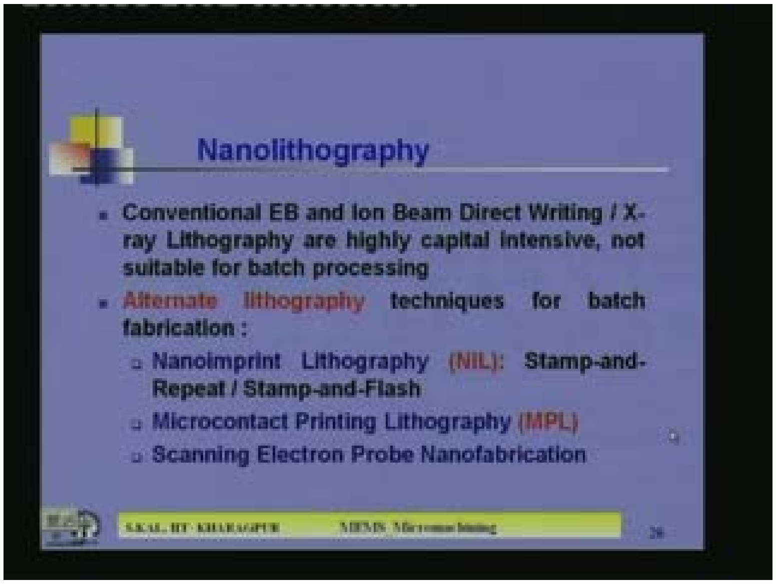

Nanolithography

- Conventional EB and Ion Beam Direct Writing / X-ray Lithography are highly capital intensive, not suitable for batch processing
- Alternate lithography techniques for batch fabrication :
  - Nanoimprint Lithography (NIL): Stamp-and-Repeat / Stamp-and-Flash
  - Microcontact Printing Lithography (MPL)
  - Scanning Electron Probe Nanofabrication

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So another two things, that one is the nanolithography conventional electron beam and ion beam. Direct writing or x-ray lithography are highly capital intensive. Means you need very expensive equipments for that, not suitable for batch processing, x-ray lithography or say ion beam. Writing one by one we were able to do. Alternate lithography process has been evolved which is favorable for batch processing that had two techniques. One is known as nanoimprint lithography which is known as NIL. NIL technique stamp and repeat and stamp and flash method other are micro contact printing lithography which is known as MPL micro contact printing lithography. Third is scanning electron probe nanofabrication. These are some new techniques which are coming under nanolithography. How this process follows it is shown like that.

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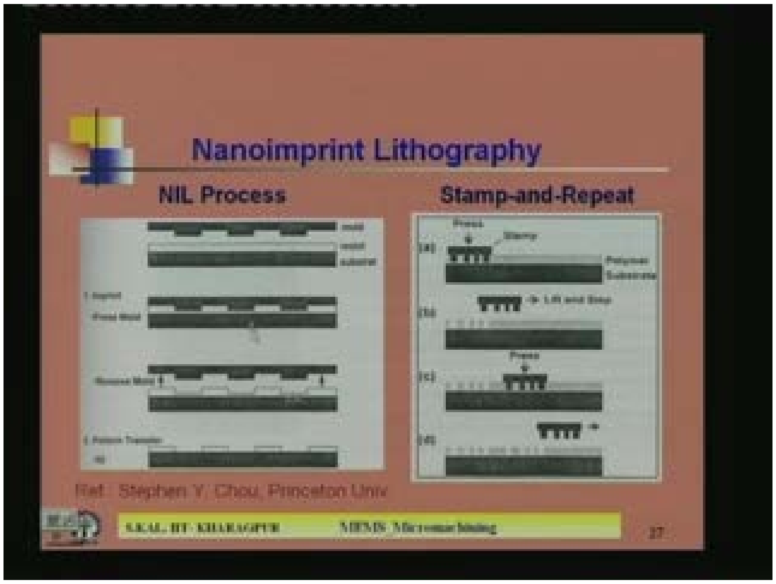

Nanoimprint Lithography

NIL Process

Stamp-and-Repeat

Ref: Stephen Y. Chou, Princeton Univ

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NIL process, nanoimprint lithography process. You just try to concentrate on this figure. What has been done? You see this is the substrate and this is a photoresist coated and this is the mold on the top. On the top is the mold. Now you imprint, that means the mold is pressed, photoresist is soft. Now you press it then what will happen? It will compress in this particular point these and this then you remove the mold, after pressing you remove the mold then what will happen? Here this particular is pressed because is soft, this is pressed and this is the pressed portion impress. Then you see whatever in the mold that pattern has been transferred here. After removing at it, you etch little bit. If you etch because here thickness is small, here thickness is large, something will be erased here and here completely erased. So the pattern has been transformed here. That is known as nanoimprint lithography, very easy technique. Another is stamp and repeat. If you want to repeat that process, repeat the structure like that. Press it here stamp, if this is the substrate, is the polymer then you lift and step in this direction then again press it then again move in this direction, again press it. So in that way stamp and repeat you can get the structures like comb like structure you can get it. That is known as stamp and repeat for both combined is known as nanoimprint lithography.

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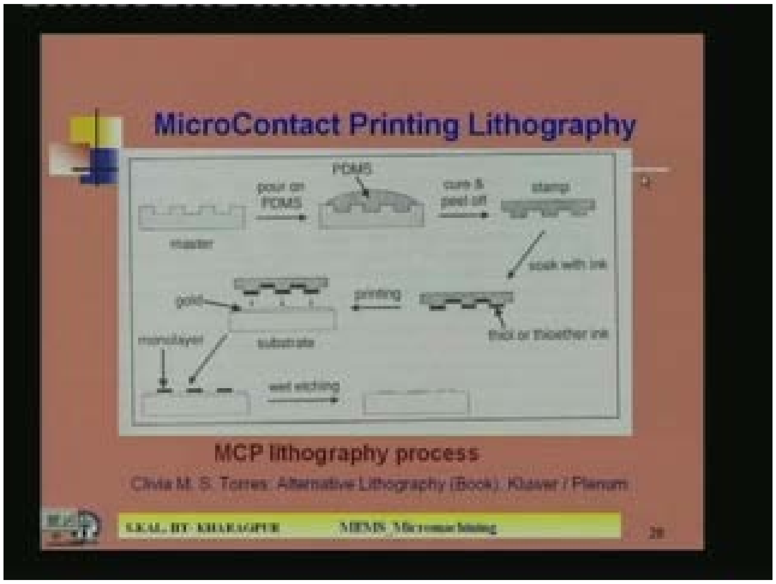

MicroContact Printing Lithography

MCP lithography process

Clivia M. S. Torres: Alternative Lithography (Book): Kluwer / Plenum

Next is microcontact printing lithography MPL. What is that? Is a muster in this pour on pd of this particular because some these are some muster structure. On that structure, that group is there then PDMS which is a polymer you pour the polymer on this structure. So it is spread. After that, cure and peel off, so you cure it then this bottom thing is taken out this bottom thing is taken out. So you will get the form, this stamp the top side you is like that top side is like that. After that you soak it with ink. What is the ink? Thiol or thioether ink. This particular is stamp has been formed, this stamp now coated with ink. That ink is a thiol or thioether ink. Now you go for printing, just like your stamp you use it. You are printing here and this is the gold coated. This substrate is the gold coated. Now if you print here that thiol or thioether ink will make some passivation layer, monolayer and after that go for wet etching. This particular portion will be stopped and here etching will be done. That is basically microcontact, we no lithography no exposure no machine nothing required very simple technique. Isn’t it? Is not at all the high expenditure equipment required nothing required.

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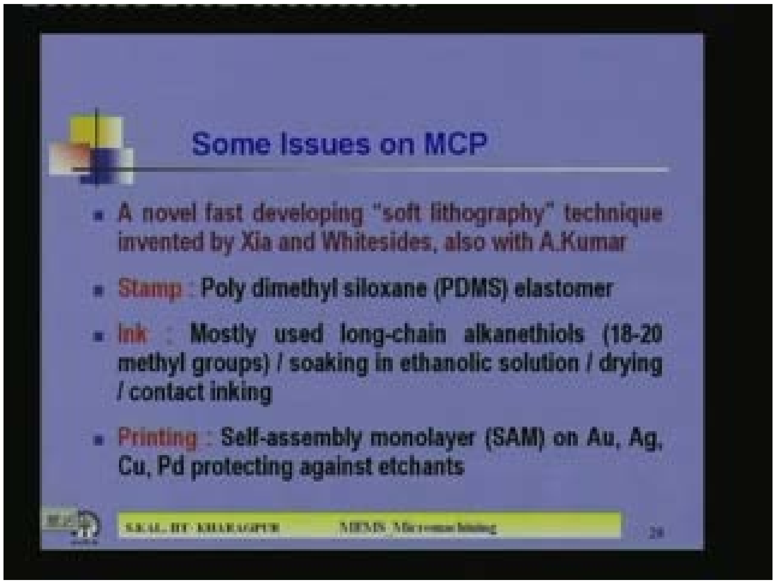

Some Issues on MCP

- A novel fast developing "soft lithography" technique invented by Xia and Whitesides, also with A.Kumar
- Stamp : Poly dimethyl siloxane (PDMS) elastomer
- Ink : Mostly used long-chain alkanethiols (18-20 methyl groups) / soaking in ethanolic solution / drying / contact inking
- Printing : Self-assembly monolayer (SAM) on Au, Ag, Cu, Pd protecting against etchants

So next some issues I will just, these are known as soft lithography. The novel fast developing soft lithography technique is invented by these people. This is NPL or stamp and repeat process, stamp poly dimethyl siloxane and PDMS elastomer that are the stamp material. First stamp material has been formed then you are going to use the ink, mostly use long chain alkanethiols 18 to 20 methyl group soaking in ethanolic solution drying and contact inking, that is the ink. Printing self-assembly monolayer SAM on gold, silver, copper, palladium, protecting again etchants what I just showed you. So that technique is getting importance. Now a days that does not have a lot of money lot of capital equipment is not required so easy technique you can get some microfabrication using these two methods. So let me stop here today. We will continue in the next class on the micromachining surface micromachining basically. Thank you very much.

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Preview of Next Lecture

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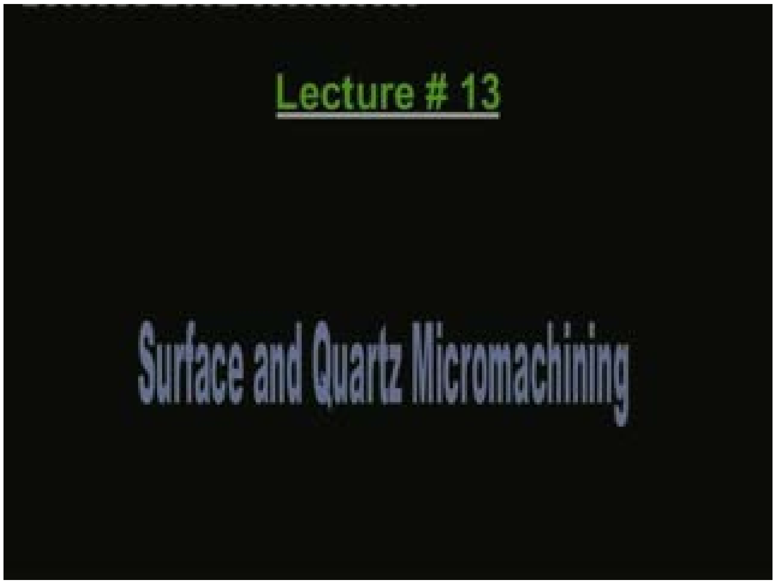

Lecture # 13

Surface and Quartz Micromachining

Last class we had a discussion on the bulk micromachining of silicon.

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Surface and Quartz Micromachining for MEMS

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Today we will discuss on surface micromachining of silicon as well as quartz micromachining. As I told in my lecture on MEMS materials, that quartz is also an important MEMS material. Lot of sensors is fabricated using quartz because it is a very good piezoelectric material. So if you use quartz in MEMS sensor, you have to have some technology on micromachining of quartz. So that part also I will discuss in today's lecture.

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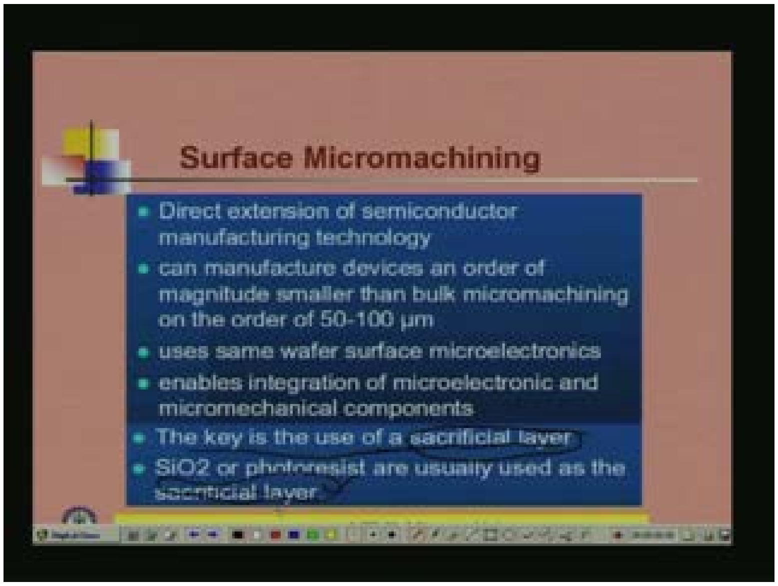

Surface Micromachining

- Direct extension of semiconductor manufacturing technology
- can manufacture devices an order of magnitude smaller than bulk micromachining on the order of 50-100 μm
- uses same wafer surface microelectronics
- enables integration of microelectronic and micromechanical components
- The key is the use of a sacrificial layer
- SiO2 or photoresist are usually used as the sacrificial layer

Now surface micromachining is a direct extension of semiconductor manufacturing technology. Direct extension means it is coming from the normal etching which is used in VLSI processing. Bulk micromachining is not a direct extension because in normal VLSI processes do not require the etching up to 300 micron, 400 or 500 micron. But surface micromachining here etching is in the range of few microns 1 micron or 2 micron in some cases may be 500 angstrom also. So that is why they mention that this surface micromachining phenomena is a direct extension of semiconductor manufacturing process.

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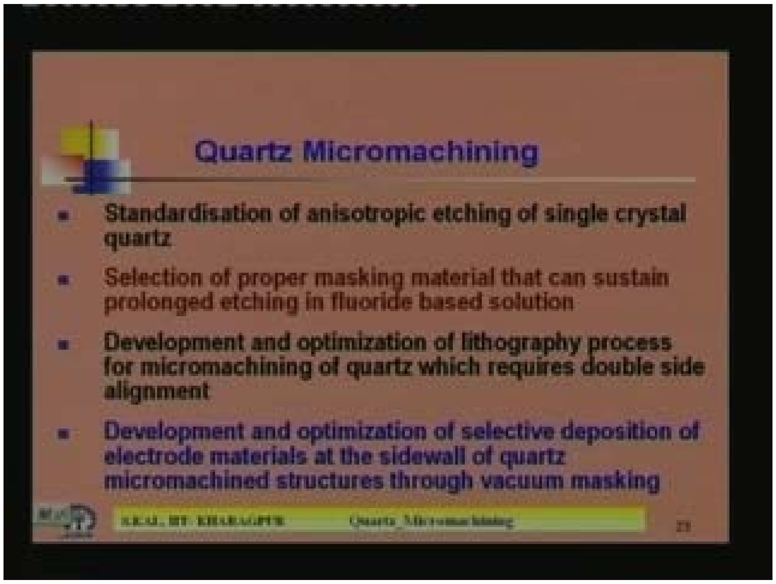

Quartz Micromachining

- Standardisation of anisotropic etching of single crystal quartz
- Selection of proper masking material that can sustain prolonged etching in fluoride based solution
- Development and optimization of lithography process for micromachining of quartz which requires double side alignment
- Development and optimization of selective deposition of electrode materials at the sidewall of quartz micromachined structures through vacuum masking

Quartz_Micromachining 23

For that you need a special kind of technique which is known as the vacuum masking technique and that will help you to get side wall electrode as well as convention techniques can be used for bottom and top side electrode.

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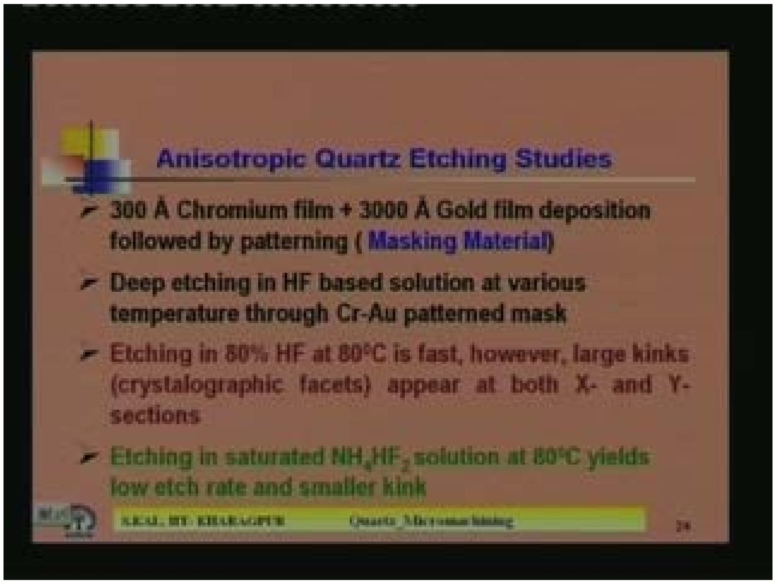

Anisotropic Quartz Etching Studies

- 300 Å Chromium film + 3000 Å Gold film deposition followed by patterning (Masking Material)
- Deep etching in HF based solution at various temperature through Cr-Au patterned mask
- Etching in 80% HF at 80°C is fast, however, large kinks (crystalographic facets) appear at both X- and Y-sections
- Etching in saturated NH_4HF_2 solution at 80°C yields low etch rate and smaller kink

Quartz_Micromachining 24

Now in the anisotropic quartz etching what are the materials you use? Chromium gold is used to as masking material. 300 angstrom chromium film, 3000 angstrom gold film followed by patterning, it will get the masking material. Deep etching in HF based solution at various temperature through chromium gold patterned mask. What is then etching solution? Hydrofolic base solution is the etching solution. 80 percent hydrofolic acid at 80 degree centigrade is the fast however large kinks crystallographic facets appear at both X and Y sections. So some crystallographic facets will be created and those facets will create some problem in your structure. Etching in saturated ammonium fluoride HF_2 solution at 80 degree centigrade, its low etches rate and smaller kinks. So this part of the quartz etching and how to get regular structure that I will continue in my next lecture also. Thank you very much.