# MEMS & Microsystems

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**Lecture No. # 24**

## Piezoresistive Accelerometer Technology

We are discussing on a case study that was the development of MEMS accelerometer. That is piezoresistive accelerometer and in my last two lectures I have discussed in detail on the design aspects of the accelerometer along with the external circuits necessary for characterization the accelerometers.

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Technology Development of
Piezoresistive Microaccelerometer

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Today's lecture is on the development of the technology of the MEMS piezoresistive accelerometer. How the accelerometer is designed, that has been told already. Now the technology development as well as packaging and characterization, how it can be done, that will be discussed in today's lecture. Then the case study will be completed.

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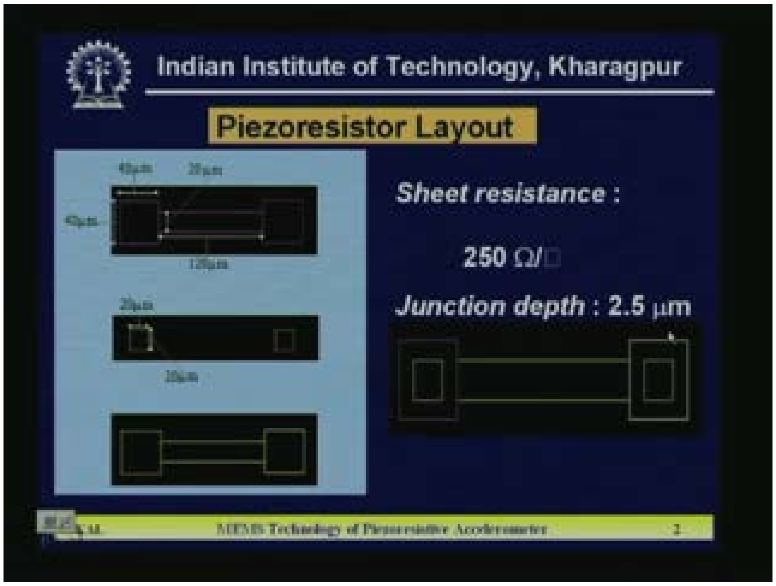

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Piezoresistor Layout

Sheet resistance :

250 Ω/□

Junction depth : 2.5 μm

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So for designing accelerometer the end of the design process is making the mask. Mask was not discussed in my last lecture, today I will first initiate the discussion on the fabrication of mask and then we will switch over to the technology development. Now for the layout of the mask; here first you have to design the resistance, piezoresistance and so far the design is concerned is same as the design resisted design used in integrated circuits. Already you know how in IC the resistors are designed; it is you have to know the sheet resistance of the layer which will give the desired resistance value. Now if you know the sheet resistance, then you have to select how many number of square are required to get that resistance and in our design we found that our resistance value is nearly 1.5 kilo ohms in that range. But one thing I would like to mention that in any diffusion technique the resistance variation after fabrication is nearly 10 to 20 percent.

In most of the IC's, are designed in such a fashion that even 20 percent variation of the resistance values will be accepted by the designer, that mean design should be low so that with that resistance chain the performance of your circuit will not hamper a much. Similarly here also we assume even 10, 15 percent variation the complete circuit should work. And in our case so far the IC's concerned that is mainly the resistance bridge and interface electronics will separate at outside the chip, because we are not going to have this marked piezoresistive accelerometer sensor, acceleration sensor rather the multi chain module we are thinking. So first if we discuss on the resistance we have you remember the sheet resistance value we have assumed is a 250 ohm per square and junction depth is 2.5 micrometer. So there you can see the diagram in the left side. So there the width of the resistor we assume it is a 20 micron.

So accordingly length we have decided 120. So 120 by 20, so it will be 6 and then it will be approximately 3 kilo ohm type and the contact pads on both the side will give 0.5 square also. So in the total resistance value will be should be nearly say 2.1, it is nearly 1.5 kilo ohm, I think 1.5

kilo ohm. So now if we connect two resistances in series it will be 3 kilo ohm. So now this is the contact area in the second diagram, it is 20 micron by 20 micron. It depends on your technology, but here we have taken the robust values of 20 micron by 20 micron so that in future we will not have any problem. So the contact is the second diagram is the contact pads and the overall the structure looks like that.

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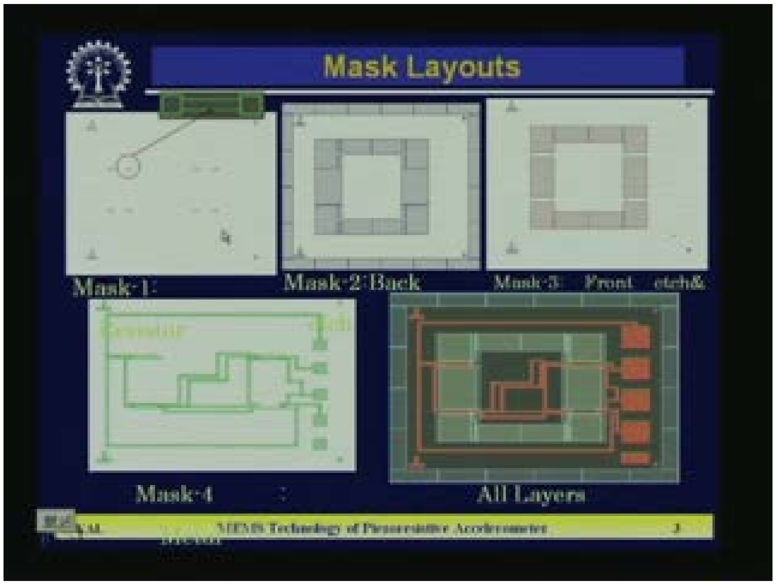

Mask Layouts

Now after the piezoresistance layout, then we will go for other layouts that mean etching. You are going to etch and metallization so here basically it will be nearly in masks are nearly 4 but another 2 mask are required. So that is for the glass etching mask is required as well as some passivation mask is also required, that is not included. Fabrication of the middle layer which is the sensor, for that you need the 4 layers. That is mask number one is the resistor mask, mask number two is backside etching mask, mask number three is front etch and contact window, mask number four is metal line and these are the four masks and if all the fours masks are overlapped, then it looks like that all the layers together. So resistance mask one resistance looks like here it is shown here and backside means one front, one backside mask is required because you are going to etch the complete thickness of the silicon by bulk micromachining technology.

So here initially from back some of the layer is etched, so that is using the TMH and the front also if we remove the silicon dioxide from selected portion. So when will you put in the etch bar, then completely the from some for the reason it will attract from front side and backside and thorough hole will be there and in the frontage mask where it is protected. So particularly in the flexure region and the proof mask region which is at the center, so that portion we have to protected so that from the front those regions will not be etched but from the back it will be etched and it will stop somewhere. Somewhere means the flexure, thickness so just by deciding how much time required will give you for front etch and back etch. So your flexure thickness will be determined from that time management. And these are the interconnection layer because Wheatstone bridge you have seen there are 8 resistances. So you have to connect 8 resistances as that you can get very low off axis sensitivity.

So here the resistance lines are moving from one end of the bridge to one end of the frame to other end of the frame and there the lines are routed in such a fashion that there should not be any overlap. So we have not used any underpass resistances here and we have used single level of metallization. So some tricks we have to follow, so that the metal lines will move in such a fashion; two lines will not touch each other or it will not overlap and there are 4 bond pads required you know; 2 are for power supply and 2 are for output and here you can see there are 5 bonding pads. One extra bonding pad has been given here, that is for substrate contact. So the substrate should not be floated substrate should be grounded otherwise if it floats, so there may be problem of stability during the measurements. So that is why 4 bond pads, 2 are meant for power supply, 2 are meant for output and 1 is for substrate contact. So these are the complete layout and along with the bonding pad this shown here.

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Fabrication Process

**Wafer specifications:**
Si <100> , n-type, 4-6 Ω-cm, thickness 275µm, DSP

**Oxidation:**
20-120-20 min @1100°C
thickness ~ 1µm

**Lithography Mask-1**
Oxide patterning for boron diffusion

**Boron Pre-dep:**
15 min@ 950°C
Rs ~ 90 Ω/□

**LTO:**
30 min@750°C

**Boron Drive-In:**
100 min@ 1125°C
Rs ~ 250 Ω/□

**Lithography Mask-2**
Oxide patterning for back side Si etching

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Now the fabrication process. So fabrication process first step you have to specify the wafer and we are going to use silicon 1 0 0 n-type. Because we are going to make resistance p-type diffusion and resistivity of the wafer is 4 to 6 ohm per square, thickness of the wafer 270 micrometer, plus minus 5 or 10 percent variation is there and this is a double side polished and this is 2 inch diameter wafer. In 2 inch diameter wafer you know is the thickness is roughly 280 micrometer plus minus 5 micrometer already tolerance is there. So this is the basic wafer and then after taking that wafer you go for oxidation and that is called initial masking oxidation. That is 20 minute to dry oxidation; 120 minute weight oxidation, another 20 minutes is again dry oxidation. You know normally any sort of masking oxidation will follow dry weight and dry sequence. So that quality of the oxide is good as well as it will not take much time and it has been done at 1100 degree centigrade and if you follow this sequence the thickness is expected to be 1 micrometer. Now after masking oxidation you we are going to use mask number 1. Mask number one is oxides patterning for boron diffusion. That means first step is to fabricate the resistances and the resistance location already found and accordingly mask has been designed maximum stress region they are located resistances are located.

So oxide patterning for boron diffusion for resistance we are going to use the boron diffusion, solid source diffusion, source is boron nitrite cake and from there has 2 step we will follow. First is pre deposition and then is drive in and boron pre deposition diffusion we follow 15 minute 950 degree centigrade and there the sheet resistance is approximately 90 ohm per square. So with that step next is LTO. LTO is low temperature oxidation; in particular boron diffusion normally in between pre deposition diffusion and drive in diffusion we follow a step which is known as a LTO low temperature oxidation. What is the requirement of that particular step? We use this because we have to remove some boron stain. During the pre deposition diffusion using the boron source, boron nitrate cake, a boron stain that is borosilicate glass a very thin layer of borosilicate glass will be deposited along with pre deposition diffusion. This thin layer of borosilicate glass is very difficult to remove afterwards. Means after drive-in and in drive-in we know there should not be any source of boron from external side. Only whatever has been inserted into the silicon that will redistribute, that is the objective of drive-in step.

But here if you do not remove that stain layer of boron, then they will act as a source during the boron drive in process also. So in that case the sheet resistance will change, it will not tally as per your simulation results. So that is why in between the pre deposition diffusion and the drive in diffusion whatever the boron stain is formed, that has to be removed and that can only be removed if that borosilicate glass is completely oxidized. That means we have to go for a very low temperature weight oxidation. 30 minutes, 75 degree C, so with that whatever the borosilicate stain layer is formed on the surface of the silicon, that will be converted into silicon dioxide and after that you give in buffer hydrofluoric acid a dip. That mean etch that these boron stain by buffer hydrofluoric acid, then clean it will be the surface boron source from the stain will completely be removed.

After that you go for boron drive-in and that boron drive-in we follow here 100 minute of drive-in and 1125 degree C. That is basically the oxidation and annealing together and because of that you know the impurity which has been inserted by boron pre deposition will reduce to and it will further go along the depth of the silicon and junction depth will be decided by the boron drive in process mainly. And after drive-in is completed, the expected sheet resistance is 250 ohm per square. Now next step is the again lithography. During the drive in process you know we normally fabricate a thin layer of oxide. That thin means is not thick as the initial masking oxidation. That is why I am calling it thin and that is nearly 5000 to 6000 angstrom unit and that is adequate for subsequent the lithography step and there we pattern the oxide for backside silicon etching. That is the mask number 2 is for backside silicon etching.

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**Fabrication Process**

**Lithography Mask 3**
Oxide patterning from front for CW, and front side Si etching

**Metallization:**
Aluminum deposition
Thickness ~ 1 μm

**Photolithography Mask 4**
Metal patterning

**Anisotropic Etching:**
Etching in 5 wt% dual-doped TMAH @ 70°C from both side to release accelerometer structure and define flexure thickness
Etch rate ~ 0.8 μm/min

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So after that, again we go for lithography with mask number 3. Mask number 3 is oxide patterning from front and CW is contact window and front side silicon etching. So backside lithography we did it but after that in mask number 2, in the previous slide after that we did not go for the complete etching. Then subsequently go for because it has double side polished wafer, we go for the mask number3 and lithography there and after lithography then front side silicon is etched little bit. Oxide is removed in the lithography then the silicon is etched. That means you define where the holes complete holes thorough holes is to be made and here it will protect the proof mass region as well as the flexure region and you should not go for longtime etching because then the surface will be completely irregular. Means there will lot of ups and downs and then metallization may be a problem. So few 100 angstrom or say at the most 1 micron or 2 micron you etch it, after that you go for metallization and there aluminum is deposited and patterned and aluminum thickness is 1 micron.

Then this aluminum will remain on the top and in the top and bottom both places we have defined the regions where silicon is to be etched by using lithography mask number 2 and mask number 3. Then after metal pattern is over that is the mask number 4 then you go for anisotropic etching. This etching in 5 weight percent dual doped TMAH at 70 degree centigrade, dual doped TMAH etching has be explain in detail in my micromachining lecture. So we used the 5 weight percent and temperature we use 70 degree C from both side to release accelerometer structure and define flexure thickness and flexure thickness is we design for 20 micrometer. But exactly 20 micrometer you may not get it; after etching you have to again measure the thickness of the flexure, it will be nearly that thickness. So that whatever thickness after etching you are getting it.

So with that thickness you have to recalculate or re-estimate again how much will be the output voltage of the bridge and it so obviously whatever the stress values we have defined earlier during the design, it will not be the same the flexure thickness is different. And exact flexure thickness you cannot get until or unless you go for this doping selective etching or electrochemical etching. Here we what we follow here is a time etch. So time etch disadvantage also I mentioned in my lectures on micromachining. Then here all the flexure whatever you need the thickness that may not be available. If you go for time etching, some variation will be there because of uncertainty in recording time of etching. Anyway so the etch rate of the TMAH at 5 weight percent dual doped is a 0.8 micron per minute and how much thickness you have to etch, how much silicon thickness you have to etch, so that you can determine and accordingly you can dip the complete thick wafer into the TMAH solution for that time.

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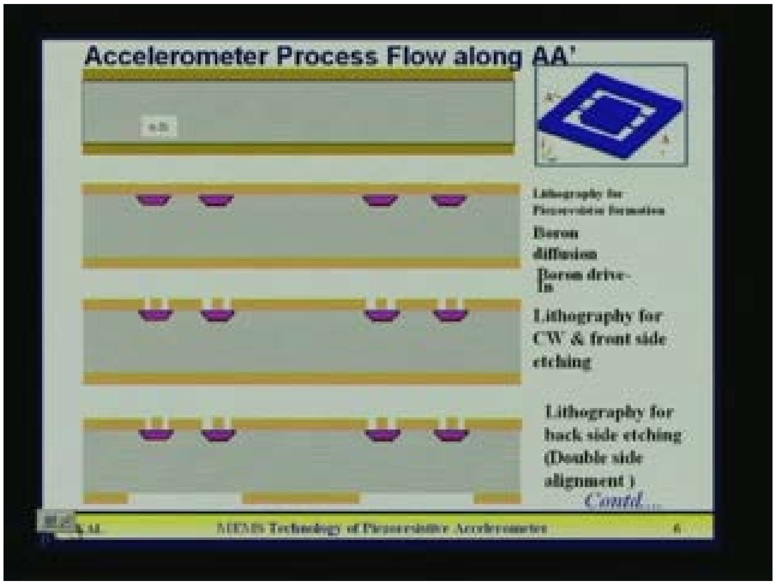

Accelerometer Process Flow along AA'

Lithography for Piezoresistor formation

Boron diffusion

Boron drive-in

Lithography for CW & front side etching

Lithography for back side etching (Double side alignment )

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So now how the process flows, then that I will show you. That will give you a complete a full-fledged idea of how these things is going on. Now you know this left side is you can see here the structure of the in the left sided structure of the accelerometer and along AA dash we are drawing here, the cross section diagram process flow. Now initially the end silicon wafer. Now what is done? If the oxide is grown, when you grow the oxide it will be from top and bottom both sides oxide is there, that oxide is grown. In the next step we just lithography for piezoresistive formation. That means front side lithography you have made so that you have open the windows from the top side oxide where the boron is to be doped. Then the boron diffusion pre deposition and drive in deposition we made. So you can the pink color regions are the boron atoms which has already inserted into the silicon wafer.

Then we go for the boron drive-in. Initially the pre deposition and drive-in. During the drive in process whatever the groups followed and that will again cover. So that means oxide both front and backside will cover this silicon bear silicon. So that is after boron drive-in it looks like that. Next step is the lithography for contact and front side etching that you can see here the contact as will open and the oxide was etched and it is the front side is defined. Next we go for the lithography for backside etching using double side alignment. So wherever the resistances is there and you have to see those regions because it all the diagram which you can see here is cross section along AA dash which is shown in the right side of the middle sensor structure. So the bottom side also the oxide is removed.

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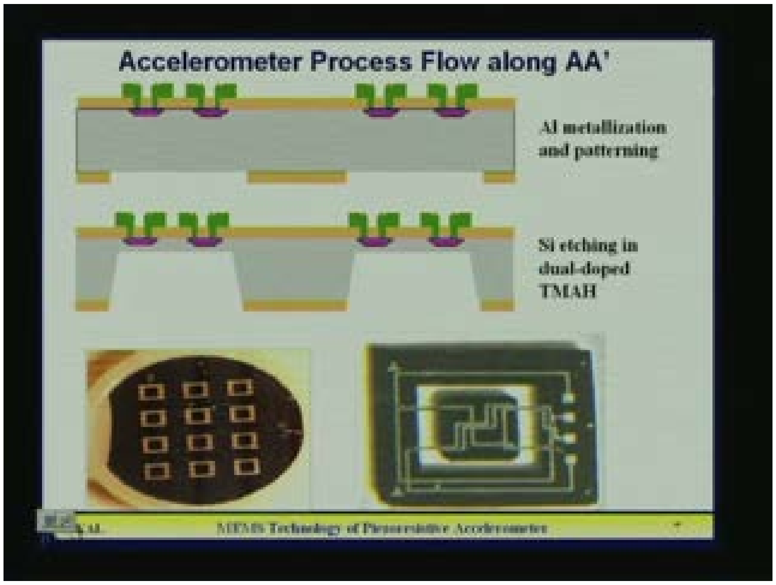

Accelerometer Process Flow along AA'

Then in the next step you can go for the aluminum metallization and patterning. So aluminum metallization the green levels are aluminum the along the cross section diagram it is again. So now you can go for the silicon etching in dual doped TMAH. So it will look like that. Since the structure is only along a AA dash. So the front side the etching front side, particularly the periphery of the proof mass is not shown here, that whole diagram is along AA dash. That is why you can see only the backside etching. Only front side etching part is not shown here in this diagram. So with that you can get the cross section along AA dash like that and this is a 2 inch wafer in the about 12 pieces you can see the accelerometer, the front view of the complete wafer is shown here and one individual structure in magnification it is here. You can see the metal lines how it is moving over the flexure and the bond pads are also shown. The individual wafer is individual piece of accelerometer is shown in the right side diagram and the complete wafer is shown here in the left diagram.

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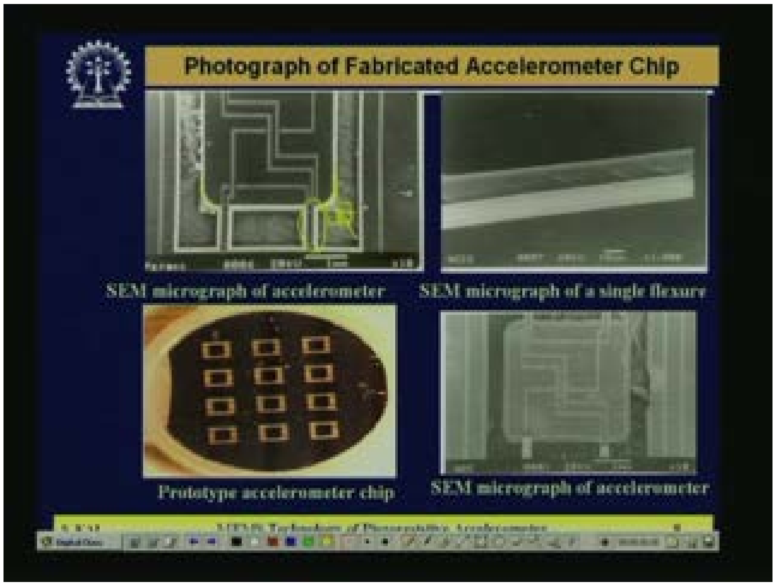

Photograph of Fabricated Accelerometer Chip

SEM micrograph of accelerometer

SEM micrograph of a single flexure

Prototype accelerometer chip

SEM micrograph of accelerometer

So this is the thing, so here some photomicrographs are shown on different places. So you can see this is the CM micrograph. So the picture one shows the aluminum metal line how it moves and the flexure. Particularly this picture is shown to show you how the flexure has been made and another thing is to be in one important point is when you are make the design particularly the proof mass design, then you can see the corner I have mentioned you earlier that at the corner etch rate is faster. So that is why you have to in all such design you have to allow corner compensation. That means since corner etch rate is more compared to the lateral or vertical etch rate in the side. So what normally is done, you can see here. So this is basically the flexure. Now this corner you have seen that it has been etched and ultimately it is rounded here. Similarly here also rounded. But if we need the perfect square structure then what is normally done on a mask side, you have to make a corner compensated structure something like that.

So if you make that so it will attract from this side, it will attract from this side, that side. So ultimately it may end up in a complete square. So that corner compensation is given so that here you can see that is the almost nearly perfect you have got it. Otherwise if you do not give the corner compensation, then it will look like that because it will etch more at the corner, this corner, this corner and this corner. But the complete square structure you cannot get it. So that is one point I am not mentioned earlier. But during mask fabrication that we have to add and this is the flexure dimension how the flexure has been made that is shown in a CM micrograph also. This length is 10 micrometer, so from there if you scale it so you can easily measure the thickness of this flexure and this is the width of the flexure you can easily measure. So this is a micrograph of the flexure and this is the 12 pieces and 1 piece is shown and this along with the metal lines.

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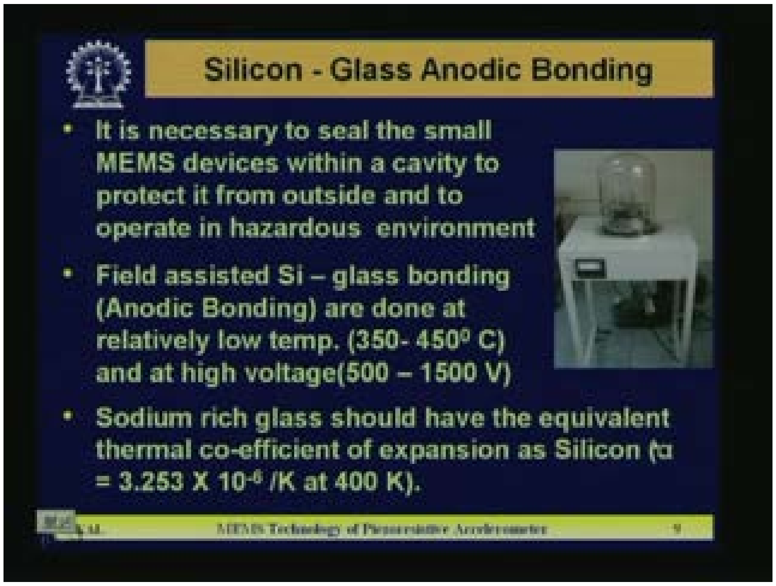

## Silicon - Glass Anodic Bonding

- It is necessary to seal the small MEMS devices within a cavity to protect it from outside and to operate in hazardous environment
- Field assisted Si – glass bonding (Anodic Bonding) are done at relatively low temp. (350- 450$^0$ C) and at high voltage(500 – 1500 V)
- Sodium rich glass should have the equivalent thermal co-efficient of expansion as Silicon ($\alpha$ = 3.253 X $10^{-6}$ /K at 400 K).

Now so is a first you have fabricated the middle sensor. But accelerometer structure we have seen there are 3 pieces, 2 cap layers are there. For your damping analysis you need upper cap layer and bottom cap layer has to be delineated. So that during the moment of the middle proof mass, so the proper damping is to be made by allowing certain gas or air with certain pressure, certain viscosity in between the gap between the proof mass and the bottom and top cap layer. So next step is to design and fabrication of the top and bottom cap layer. So top and bottom cap layer normally we make out of the glass, Pyrex glass is normally used and how the glass is again micromachined and structured. So that it will be just cover top as well as bottom and from the top cover the bonding pad is to be separated out. Because if you cover the bonding pads there are 2 input and 2 output and 1 substrate contact.

If you want to connect those things, so those portion is to be left when you are going for the substrate to glass bonding. So for that you have to again design the mask for the glass etching and a bonding technique is used silicon glass anodic bonding technique which will help you bonding of silicon and glass and the substrate bonding and details of the mechanizing of bonding will be discussed in some other lectures. So here what we follow and basically that follow for etching the glass that only I will discuss. So in all MEMS devices we need that except say few cases most cases means like thermal sensor. You may not require top and bottom glass covering but most of the inertial sensor we need some cover plates either from top and bottom both or only from the bottom. In some cases not from the top; in pressure also you need if you need the absolute pressure or relative pressure. Accordingly you have to select whether you will cover both top and bottom using the glass plate or either bottom or top.

Now again glass tool, this is 2 purposes, it serves one purpose is protection of the sensing element from outside and hazardous environment. So this cover not only this in accelerometer, particular it is for damping it is required. There are in other cases also we use some encapsulation or the passivation layer that we know that is used only for the reason. What is that reason? Reason is protection of the chip from the environmental hazardous. So here the glass and silicon bonding has been done using the anodic bonding technique and that basically if you apply a voltage of the order of say 500 to 1000 volt and increase the temperature of the glass and substrate to 350 to 450 degree C, then the silicon and glass will be bonded together which we cannot separate. That is known as the field assisted bonding or anodic bonding. And this is very sensitive technology in the respect that when you bond the silicon and glass so surface of the silicon and glass is to be extremely clean.

If it is not clean, contamination is there or not smooth enough so bonding will not be proper and it cannot be shield. Another point is to be noted the matching of the thermal expansion coefficient; that is also a problematic thing. And sodium rich glass should have the equivalent thermal coefficient of expansion as silicon which is 3.253 10 minus 6 per K at 400 Kelvin. So if you go for 400 Kelvin temperature, during the bonding so there the matching of the expansion coefficient is also important because after that when you cool it will crack. The bonding regions will be crack and sealing will not be the proper. So these are the 2 points; one is matching of the expansion coefficient and other is the cleanliness of the surface of both glass and silicon where you are making the anodic bonding.

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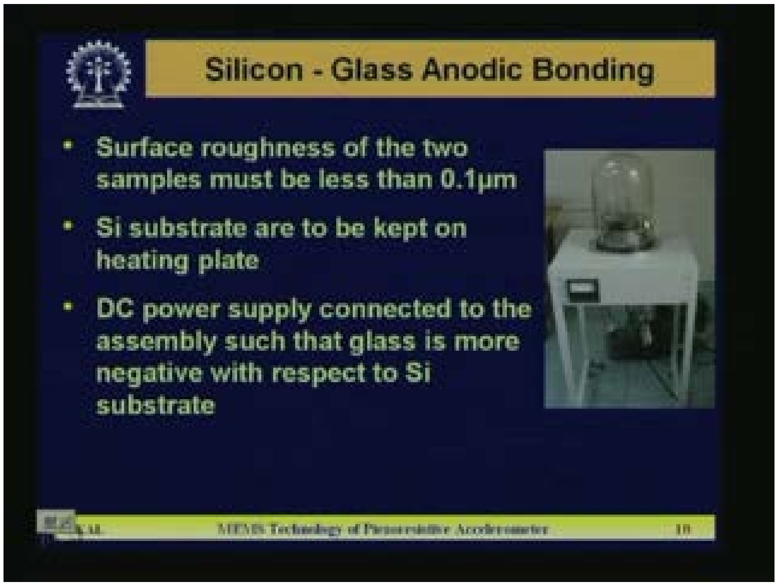

## Silicon - Glass Anodic Bonding

- Surface roughness of the two samples must be less than 0.1μm
- Si substrate are to be kept on heating plate
- DC power supply connected to the assembly such that glass is more negative with respect to Si substrate

So with that this is one kind of bonding machine you can see here whole thing is to be done in a vacuum chamber at low pressure. So that the environment hazardous will not be there. In vacuum chamber there are two electrodes where you can apply voltage and at the same time you have to heat the substrate in the range of as I mentioned 3 to 400 degree Kelvin and then if you allow certain time AND it will be automatically bond it, anodic bonding will be there. This is some indigenous equipment made in our laboratory for preliminary studies on the silicon glass anodic bonding and later on we have also procured a very good machine substrate bonder machine and that will help and there are lot of the preventing measures has been taken in that advanced machine.

Substrate bonding machine which we have recently brought and there you can bond the anodic bonding or thermo compression bonding or some other kind of bonding are also possible, fusion bonding is also possible. Now so here that means the system is to be evacuated DC power has to be add supplied and temperature is to be increased. So accordingly the whole system is not so simple. It is complicated in vacuum system, if you heat the substrate with high temperature with the high voltage. So automatically the whole module is not so simple like the normal evaporation system vacuum system you used for aluminum or gold evaporation it will be complicated. Anyway we have done it.

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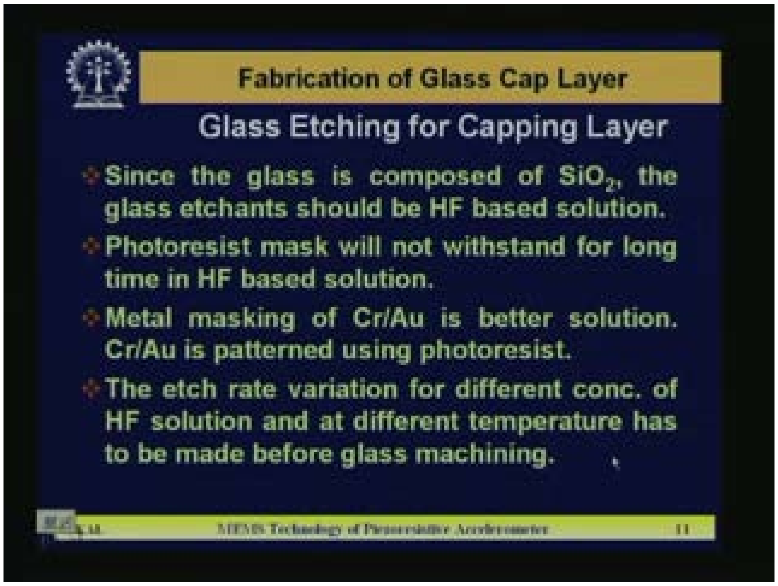

Fabrication of Glass Cap Layer

Glass Etching for Capping Layer

- Since the glass is composed of $SiO_2$, the glass etchants should be HF based solution.
- Photoresist mask will not withstand for long time in HF based solution.
- Metal masking of Cr/Au is better solution. Cr/Au is patterned using photoresist.
- The etch rate variation for different conc. of HF solution and at different temperature has to be made before glass machining.

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Now some other points are also mentioned here. Since the glass is composed of silicon dioxide, the glass etchants should be HF based solution. Now that part which I discussed is the bonding part. But now the glass etching glass micromachining how do you do it? So glass is nothing but silicon dioxide. So obviously its etching solution will be hydrofluoric based solution and then you have to mask the glass and if you etch the whole thing by the hydrofluoric acid, then thing is that you have to have some protective layer. Photo resist layer may not withstand long time in the hydrofluoric acid solution which you can use for etching glass. So we go for another passivation layer for glass etching that is chromium gold. Chromium gold metal mask, gold is a metal. So is better solution as the hydrofluoric base solution will not allow you to use the photo resist as a masking material. So the etch rate variation of different concentration of HF solution at different temperature has to be made before glass machining. So if you use the glass how the chromium gold layer is useful for your etching? To know that part you have to go for a systematic study of what systematic study that etch rate variation with temperature and concentration of the hydrofluoric acid.

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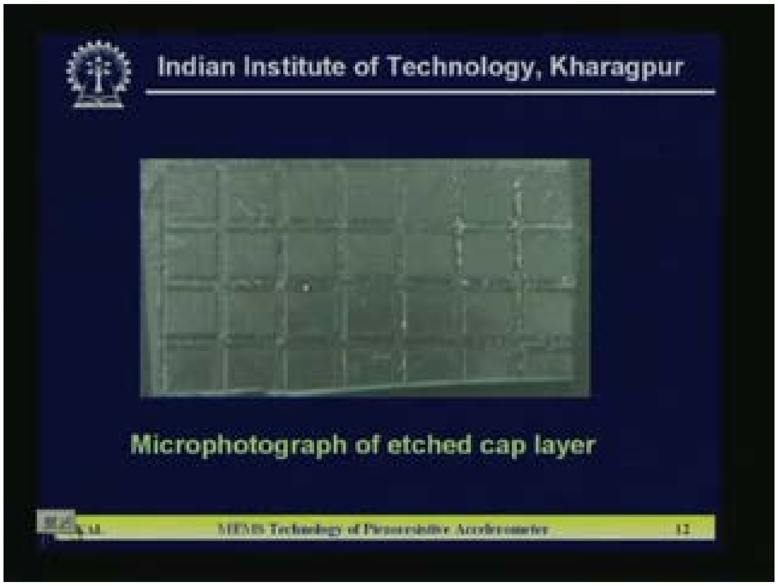

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Microphotograph of etched cap layer

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So that has been made and this is the micrograph of the etch cap layer. You can see this is a glass piece has been just etched in different pieces and in the middle portion also thinned down about say 20 micrometer gap which you have calculated during the dumpling analysis, that has been made.

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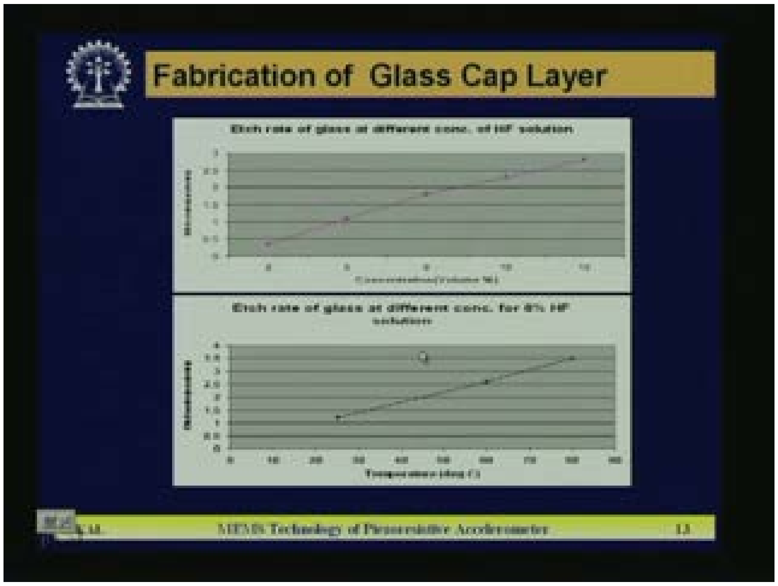

Fabrication of Glass Cap Layer

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So now these are the etch rate of the glass at different concentration; the calibration curve is shown here. The concentration verses the etch rate and bottom is the temperature versus etch rate. So this is almost linear nature of the curve which is good and from there you have to take certain concentration and the temperature to etch your glass and automatically if you know the etch rate, the timings also fixed to how much you want to etch, depending on that you can allow. That time for etching glass in hydrofluoric solution. So for that, this calibration curves are important.

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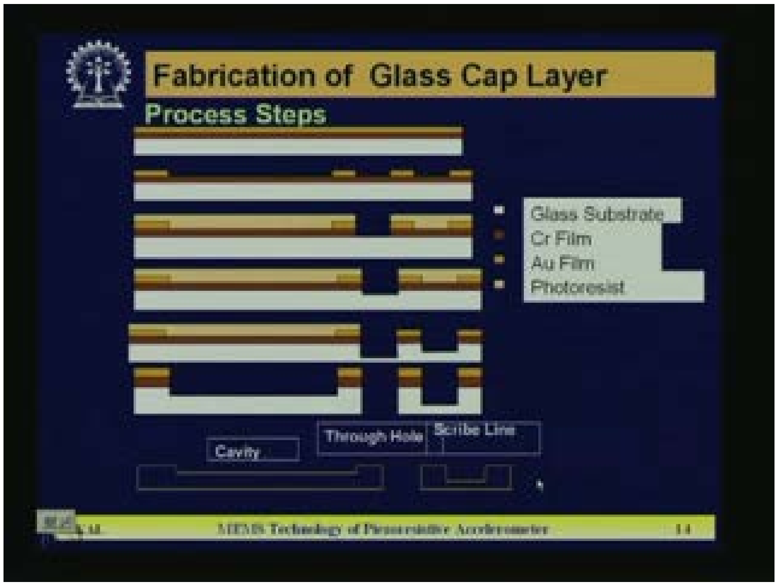

Fabrication of Glass Cap Layer

Process Steps

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Now this is the process steps for fabrication of the glass cap layer and here you can see from the first the cross section diagram is the glass substrate. Then what you have done? The chromium film that is required for gold adhesion, few 100 angstrom unit and top of that is a gold film and on the gold film is this pattern. After patterning the gold film the chromium is a bottom it is steel there; then you go for the photoresist cover. These are photoresist and after photoresist cover, then a particular region you remove photoresist. Because each window opening you required a photo masking. So you etch this particular region and first photo resist is dissolved, then the gold already remove been earlier diagram. So then chromium is removed and then you go for etching and then you will etch a little bit on the glass, not the complete some portion is etched. You can see next phase what has been done? So here window is open after this region the left side of that another window which you are, the gold was removed earlier.

So that portion is open now. So now here also you started etching, during this step here also it will continue etch. So here etch depth will be more and compared to the side depth. So here and then you remove the photoresist as well as the chromium layer from the whole region where the proof mass will bend that region. So now you again go for glass etching. So as a result of which since you have open window at the very beginning this region. So automatically what will happen? So this particular region will completely through hole will be there and here the etch depth will be less compared to the thorough hole region and subsequently which you have open at the later stage. There the etch step will be nearly 20 micron. So why I made like that because somewhere I made thorough hole, somewhere I need this scribe line. So that is why I have opened the windows in different times and at the end when we go for etching, it will etch all the layer somewhere thorough hole, somewhere scribe line and somewhere the desired delineation you will get it. This is the process steps of making the glass cap layer.

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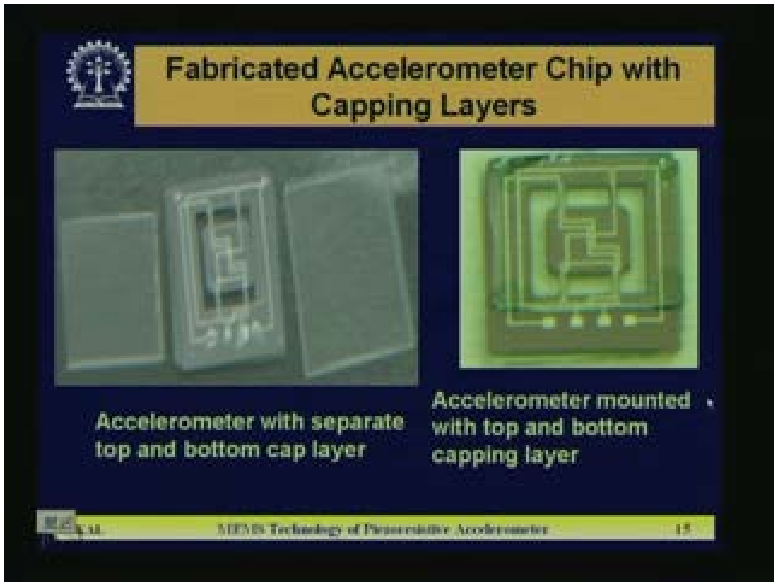

Fabricated Accelerometer Chip with Capping Layers

Accelerometer with separate top and bottom cap layer

Accelerometer mounted with top and bottom capping layer

KAL MEMS Technology of Piezoresistive Accelerometer 15

Then here the picture shows the middle layer is shown here. You can see this is the middle layer. So now in the left side and right at the 2 glass pieces which we etched and separated and in this you can see the size of the glass piece for 1 and glass piece 2 are not same different. Because one is at the bottom you need the complete size, you need the glass. This is the complete size and in the top it is smaller size. Why because you need the bonding pad region to be excluded from the cover. So if you put the bottom layer at the bottom and the top layer at the top, so then it looks like that. So you can see here this is 1, the glass layer. That is the 1 layer 1 and in the bottom is the layer 2 and in between this is a layer 2 and in between you can see the bonding pads regions are open. So there you can take bonding here, here, here and here. So these are 4 bonding pads required, two for input and two for input. Means a power supply and two for output. That is excluded, that is outside the glass cover. So with that this is up to this, you have just substrate bonding substrate to glass bonding is over.

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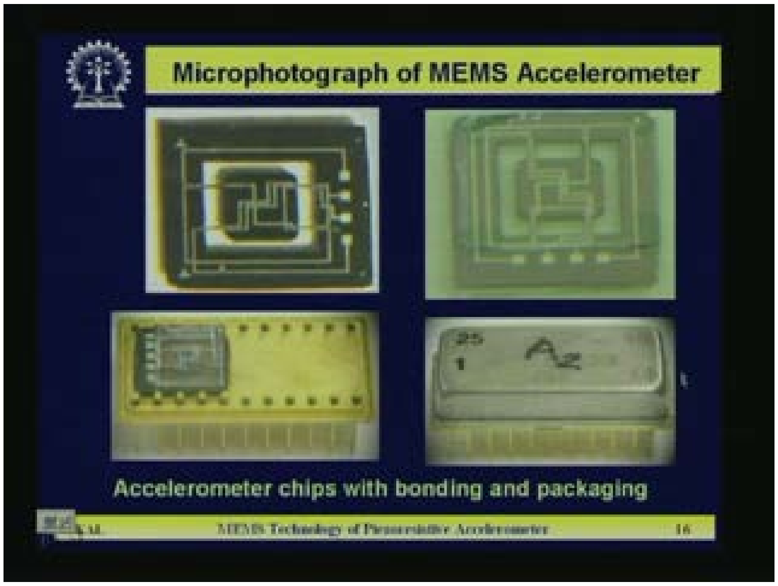
Microphotograph of MEMS Accelerometer

Accelerometer chips with bonding and packaging

MEMS Technology of Piezoresistive Accelerometer 16

Now the next step you have to package it. So you see again I have repeated this is the middle layer. So middle layer is this one, now top and bottom cap layered we have bond it. This is this one, after that what is the next step? The step1, step2 then next step3 are here. So that is, this is step3, that is the wire bonding. So you see the bonding pads1, 2, 3, and 4. If you see minutely in the figure, so bonding pads are connected; one here, so one here, one here and another is here. Here so this one is here. So one is substrate contact the 4 bonding pads. After this, is the encapsulated the case and on the case is a metal, can basically first thing is the whole chip which is shown here glass. Silicon glass is to be fixed at the middle and then where bonding is done, then top cap layer. If you put the top, this is not the sensor cap layer. But it is the encapsulation, the top metal can an encapsulation is covered then the complete the accelerometer looks like this.

This is the accelerometer, with this are leads and this is, this particular package is not ideally meant for this accelerometer. Because here you need only 5 bonding pads. But you can see how many pins are there; 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 is 22 pin. So it is a 22 pin package basically and you need only a half of that, this portion. But commercially available package with only if the 4 or 5 pins and internal size of the diameter or internal size of the size of the accelerometer is not available. That is why who use that particular package where you can use double chip into the same package. Here also you can put another chip, so that two things can be done on the same package and for different application, so this is the package, so after packaging is done, what is the next step?

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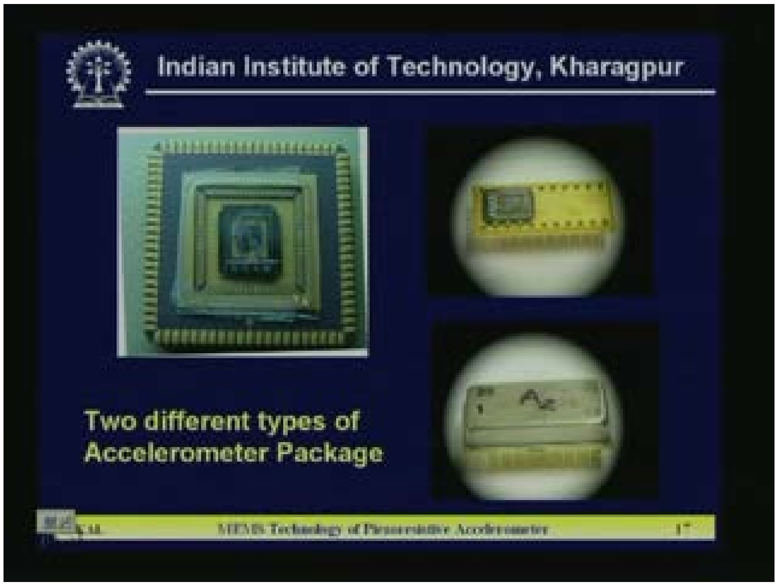

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Two different types of Accelerometer Package

MEMS Technology of Piezoresistive Accelerometer 17

Next step is this is another kind of package is shown. That is known also not meant for that accelerometer. For basically the big VLSI chip, but since the standard, the custom package was not available, we tried with this. Also initially for some testing and that is why we have seen 2 packages and this is with cover with encapsulation. Now the next part is the interface electronics.

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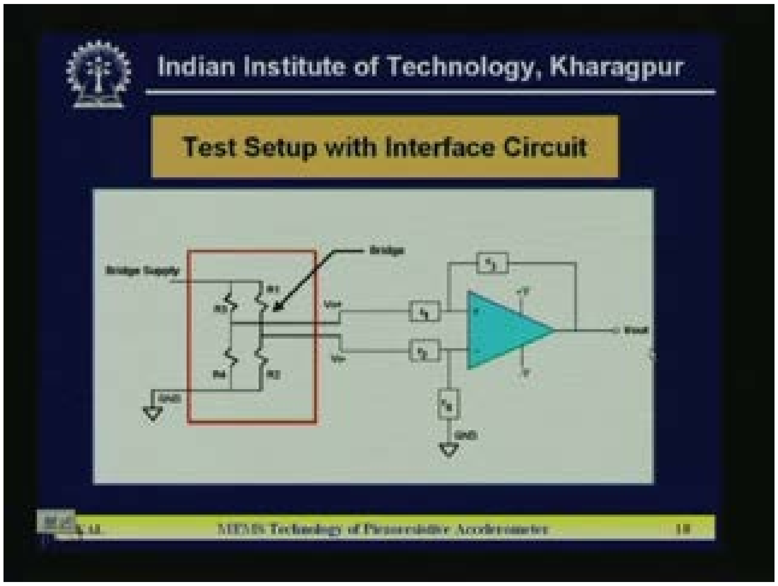

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Test Setup with Interface Circuit

MEMS Technology of Piezoresistive Accelerometer 18

So interface circuit for characterization of the accelerometer we need what we need three things we required? One is the offset null circuit because the resistance values will not exactly same which is designed. So in different arm the resistance values may differ. So because of that you will get some offset value offset means when you do not apply in the acceleration 0g. So of the bridge is perfectly balance and output should be 0. But that will not be there because some mismatch of the resistor values in different arms. So that has to be cancelled before you go for actual testing. So for that you can use a circuit for offset null circuit and that has been shown in some of my lectures. The electronics circuits and the next requirement is the amplifier and we used here chopper stabilized the instrumentation amplifier has been used for that particular purpose.

Because that reduce both 1 by f noise because you know here the sensor signal is very low frequency and almost busy and maximum is nearly 100 hertz or something like that. So low frequency DC signal is to be amplified. So without incorporation of much noise and for that the chopper stabilizing instrumentation amplifier is ideal and some such raise the amplifier module is available in the market. We can connect that the Wheatstone bridge is shown here R1, R2, R3, R4; these are basically the bridge, a resistance and is connected with the amplifier and the offset. Now circuit all has been connected and that is shown in this diagram.

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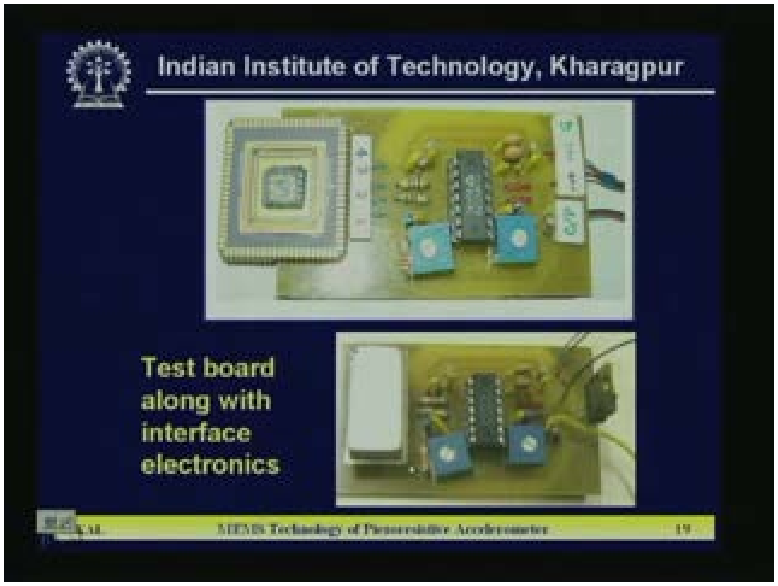

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Test board along with interface electronics

MEMS Technology of Piezoresistive Accelerometer 19

The test board along with the interface electronics. So this is the package this is two, both the packages shown. One package is here and another package is here. So now these are you can see the TC 7652, that is the chopper stabilizer amplifier and 2 trim pots are connected in the board and that is basically for exact nulling of the offset because some external trimming arrangement is also there. So that different accelerometer may have different offside voltage. So that you should have some external control. So that you can get exact null with 0g condition. For that these 2 trim pots are connected and it is amplified version is amplification is made. So that you can get plus minus 6.5 volt output, that was an initial specification.

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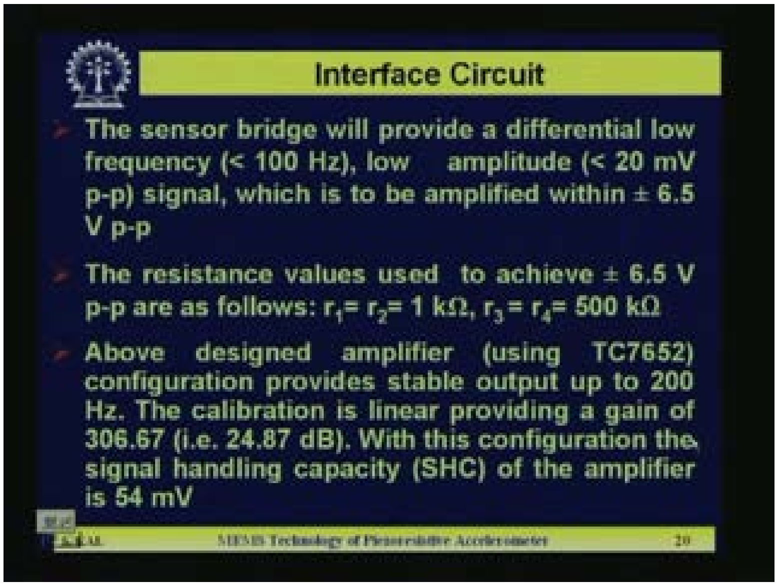

## Interface Circuit

- The sensor bridge will provide a differential low frequency (< 100 Hz), low amplitude (< 20 mV p-p) signal, which is to be amplified within ± 6.5 V p-p
- The resistance values used to achieve ± 6.5 V p-p are as follows: $r_1 = r_2 = 1\ k\Omega$, $r_3 = r_4 = 500\ k\Omega$
- Above designed amplifier (using TC7652) configuration provides stable output up to 200 Hz. The calibration is linear providing a gain of 306.67 (i.e. 24.87 dB). With this configuration the signal handling capacity (SHC) of the amplifier is 54 mV

And if you go the next stage then you can see the sensor bridge will provide differential low frequency less than 100 hertz, low amplitude less than 20 millivolt signal which is to be amplified within plus minus 6.5 volt peak to peak. The resistance values used to achieve plus minus 6.5 volt. R1, R2 equal to 1 kilo and R3, R4 equal to 500 ohms. Above designed amplifier using TC 7652 configuration provides stable output up to 200 hertz. The calibration is linear providing a gain of 306.67 which nearly 25dB. With this configuration the signal handing capacity of the amplifier is 54 millivolt. That is the test board which is made.

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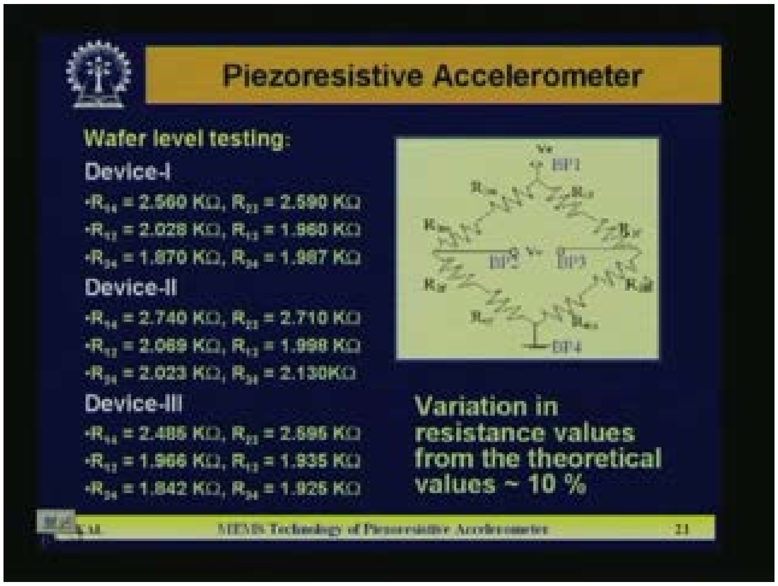

## Piezoresistive Accelerometer

Wafer level testing:

Device-I
- $R_{14} = 2.560\ K\Omega$, $R_{23} = 2.590\ K\Omega$
- $R_{12} = 2.028\ K\Omega$, $R_{13} = 1.960\ K\Omega$
- $R_{24} = 1.870\ K\Omega$, $R_{34} = 1.987\ K\Omega$

Device-II
- $R_{14} = 2.740\ K\Omega$, $R_{23} = 2.710\ K\Omega$
- $R_{12} = 2.069\ K\Omega$, $R_{13} = 1.998\ K\Omega$
- $R_{24} = 2.023\ K\Omega$, $R_{34} = 2.130 K\Omega$

Device-III
- $R_{14} = 2.486\ K\Omega$, $R_{23} = 2.696\ K\Omega$
- $R_{12} = 1.966\ K\Omega$, $R_{13} = 1.935\ K\Omega$
- $R_{24} = 1.842\ K\Omega$, $R_{34} = 1.926\ K\Omega$

Variation in resistance values from the theoretical values ~ 10 %

So now the characterization for characterize means initially we have to measure the individual resistances. So that has been measured on Bayer chip and 3 devices have been made and you can see for different arm. So 1 to 4, one means this point is one, this is fourth band. What second bond point and third bond point? So 1 to 4 if you measure from here to here, the resistance value is 2.56 and from 2 to 3 it is 2.569. So this should be equal, so you can although 2.5 in the second decimal place little variation is there. Similarly1, 2 and 1, 3 it is nearly to 2.028, 1.9624 and 341.87, 1.98. So it should be exactly equal. Why it is not there because of slight variation of the resistance values. Device two is also similar 2.74, 2.71, so if you look individual values say the values are almost equal with slight variation. Because of that you are getting the offset value and variation in resistance values from the theoretical values. This found nearly 10 percent. What about design and these are the measured value and we got nearly 10 percent variation of the resistance. That is always allowed and because of that we you we are getting offset voltage.

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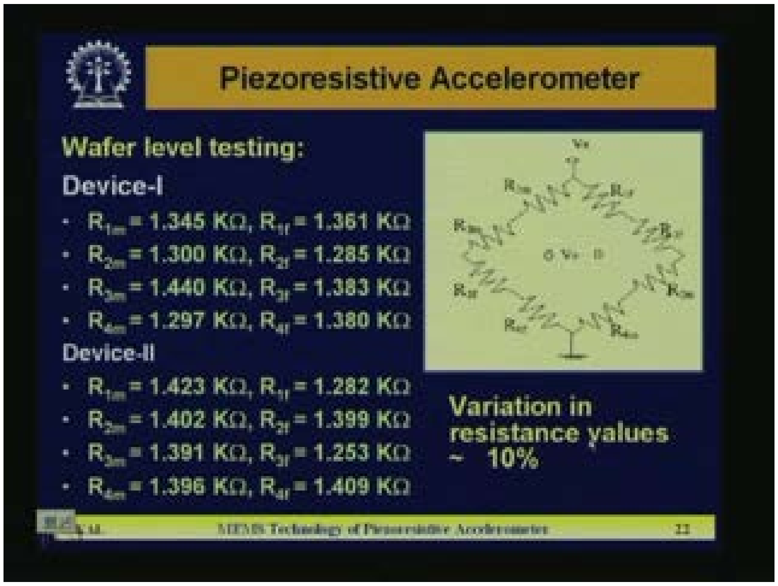

Piezoresistive Accelerometer

**Wafer level testing:**

**Device-I**

- $R_{1m}$ = 1.345 KΩ, $R_{1f}$ = 1.361 KΩ
- $R_{2m}$ = 1.300 KΩ, $R_{2f}$ = 1.285 KΩ
- $R_{3m}$ = 1.440 KΩ, $R_{3f}$ = 1.383 KΩ
- $R_{4m}$ = 1.297 KΩ, $R_{4f}$ = 1.380 KΩ

**Device-II**

- $R_{1m}$ = 1.423 KΩ, $R_{1f}$ = 1.282 KΩ
- $R_{2m}$ = 1.402 KΩ, $R_{2f}$ = 1.399 KΩ
- $R_{3m}$ = 1.391 KΩ, $R_{3f}$ = 1.253 KΩ
- $R_{4m}$ = 1.396 KΩ, $R_{4f}$ = 1.409 KΩ

Variation in resistance values ~ 10%

MEMS Technology of Piezoresistive Accelerometer 22

Now individual resistance has been made. So individual resistance, what about design 1.5K, but we are not getting it. We are getting as 1.34 kilo ohm, 1.36. So 2m, the frame ends 1m, 2m, 3m, 4m, 1f, 2f, 3f, 4f, these are the mass ends m and f stands for frame end and the connections are like that which is shown here. So individual values are also measured and we found that variation is also within 10 percent. But it is not very wide apart. So that shows that there is a possibility of that we make achieve the targeted value of the means design value of the accelerometer. So now these are some other measurements.

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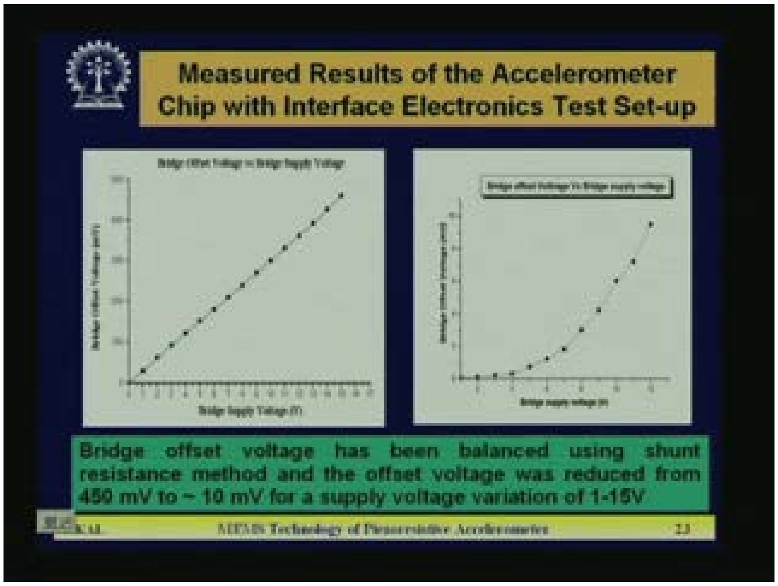

## Measured Results of the Accelerometer Chip with Interface Electronics Test Set-up

Bridge offset voltage has been balanced using shunt resistance method and the offset voltage was reduced from 450 mV to ~ 10 mV for a supply voltage variation of 1-15V

This is the measurement results of the accelerometer chip with interface electronic set up. This is the offset. So initially if you do not use that offset non circuit that is shown with power supply variation 0 to 15 volt. We got the offset bridge voltage is nearly 400 millivolt. So 400 millivolt is very high offset value. So you cannot use that particular bridge for sensing. So we connected that is that offset null circuit in the test board which you I have just now shown you. So there with incorporation of that offset, null circuit we got here. The offset value reduced at 15 volt it reduces to only 10 millivolt. Initially it has 450 millivolt is 10 millivolt. But power supply is not 15 millivolt we are going to use only 5 volt. So for 5 volt range we have seen only up to this region if you see here, so here the offset value is nearly 0.2 millivolt. So since this is a 0.2 millivolt, so that is acceptable for further measurement.

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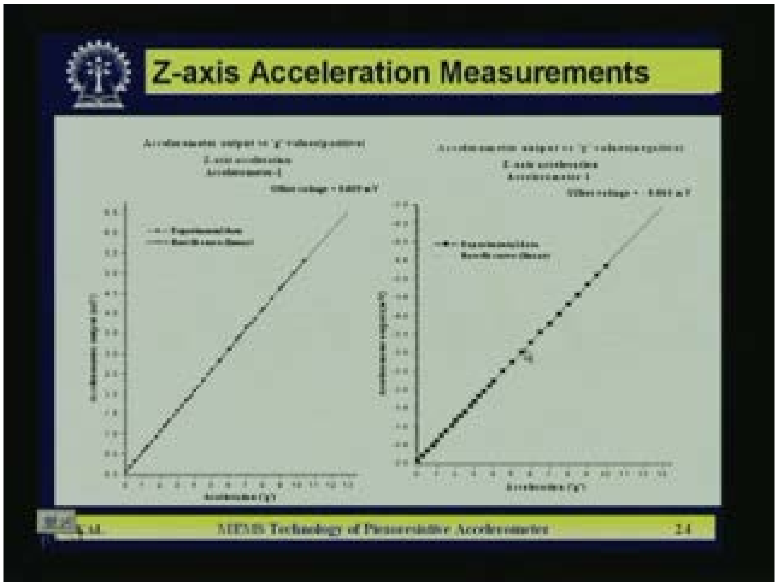

Z-axis Acceleration Measurements

Now next step we did some acceleration measurement. Only Z axis measurement is shown here and 0 to nearly 10 or 12g, you have measured and we found is highly linear. These are measured value after packaging is a dynamic testing and the experimental is a value at best fit curve is shown here and here the offset which found 0.06 millivolt in this particular case and in the second curve is a negative acceleration is a positive acceleration. Means one is acceleration; other is deceleration. So that in both the cases we found from 0 to 13g for which you have measured. So in both the cases we found is exactly linear curve and that is highly desirable and the output voltage we are getting is nearly 500 micro volts per g.

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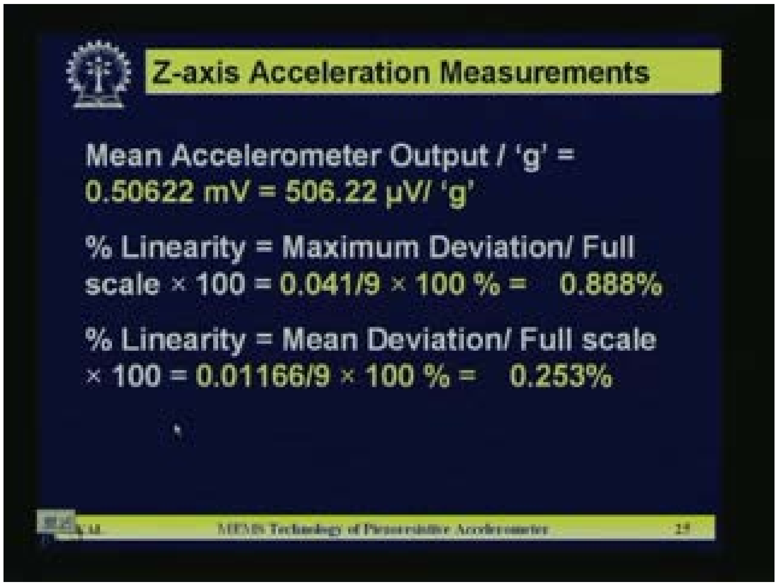

### Z-axis Acceleration Measurements

Mean Accelerometer Output / ‘g’ =
0.50622 mV = 506.22 μV/ ‘g’

% Linearity = Maximum Deviation/ Full scale × 100 = 0.041/9 × 100 % = 0.888%

% Linearity = Mean Deviation/ Full scale × 100 = 0.01166/9 × 100 % = 0.253%

So means acceleration output, we got 506.22 microvolt per g. For linearity has been calculated and if you use the maximum deviation then we are getting 0.88 percent. If you mean deviation then we got the linearity is 0.253 percent. So the linearity allowed in design is less than 1 percent and we got the targeted value, it is well below 1 percent and output is 506 and here we are not getting the output. As per your design value the reason is there, we have designed the flexure thickness of only 20 micron. But later on you measured the flexure thickness is nearly 30 or 32 micron. So because of the variation of the flexure thickness here also because flexure thickness. Thicker means you will not get much output. Output will be lower because it is not that much sensitive. So because of that we got reduced value of the output for g.

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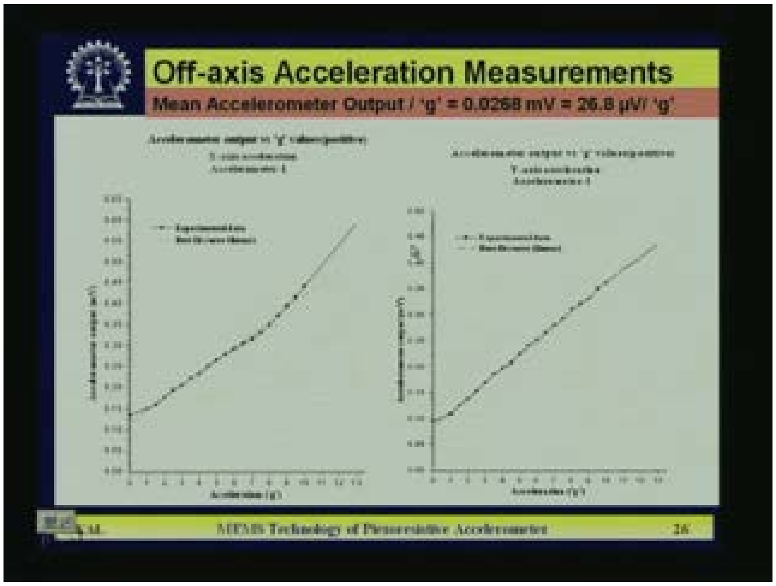

## Off-axis Acceleration Measurements

Mean Accelerometer Output / 'g' = 0.0268 mV = 26.8 μV/ 'g'

MEMS Technology of Piezoresistive Accelerometer 26

Now the next is a off axis acceleration measurement. That also we have made here along x axis acceleration along y axis acceleration the curve is shown here and that value is extremely small compared to Z axis acceleration. Z axis we got nearly 500 microvolt per g. But here you will get the value is nearly 26 microvolt per g. So that means it is highly is 500 in Z direction, 500 microvolt and x and y direction, only 26 microvolt per g. So off axis sensitivity less, but we have to agree the fact that it is not as slow as design value. Because of various reasons of the fabrication tolerance is not exactly showed which is required, which is estimated in our design. So accordingly off axis sensitivity is not that why high value. But it is 500 is 26 at least one more than one order less.

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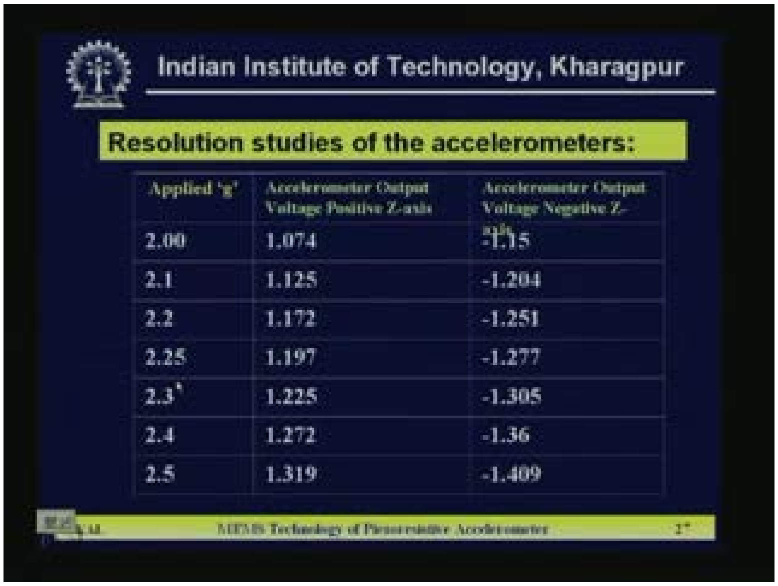

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## Resolution studies of the accelerometers:

| Applied 'g' | Accelerometer Output Voltage Positive Z-axis | Accelerometer Output Voltage Negative Z-axis |
|---|---|---|
| 2.00 | 1.074 | -1.15 |
| 2.1 | 1.125 | -1.204 |
| 2.2 | 1.172 | -1.251 |
| 2.25 | 1.197 | -1.277 |
| 2.3 | 1.225 | -1.305 |
| 2.4 | 1.272 | -1.36 |
| 2.5 | 1.319 | -1.409 |

MEMS Technology of Piezoresistive Accelerometer 27

So now if you see the resolution studies of the accelerometer, then you can see here we can measure the resolution in the z direction up to 0.25. This is a 2.2, 2.25, this is a 2.3; here you can see 0.05, 0.05g we could resolve because you can get this z axis accelerometer difference 1.197, 1.225 here. So difference is there. So that means up to 0.25g you can resolve but again it could be resolved in a further low. But because of the measurement facilities not available to give the milli g acceleration, that could not be measured. That is the limitation of our test facility. But here still we can find thus up to 0.25g then it is 250 milli g, it is resolved. So anyway so that is some of the negative and positive at z axis the resolution has been studied.

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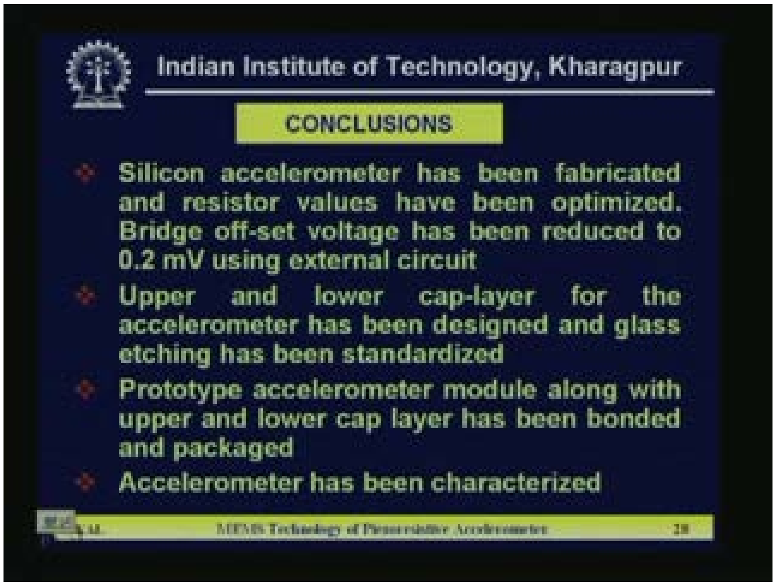

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CONCLUSIONS

- Silicon accelerometer has been fabricated and resistor values have been optimized. Bridge off-set voltage has been reduced to 0.2 mV using external circuit
- Upper and lower cap-layer for the accelerometer has been designed and glass etching has been standardized
- Prototype accelerometer module along with upper and lower cap layer has been bonded and packaged
- Accelerometer has been characterized

So with that actually let us conclude that what we did today. In today's lectures so how the accelerometer piezoresistor accelerometer is fabricated that is discussed in detail and the technology optimization has been done. Offset voltage circuit shows that within 5 volt, the offset can be reduced up to 0.2 millivolt using external circuit that is also possible. How to make the upper and lower cap layer from Pyrex glass, that has been discussed in detail and accelerometer packaging, substrate bonding is shown and the external circuits are also connected with the main sensing element and at the end it has been characterized with the limitation of characterization facilities and all these thing shows that although it is not exactly the same as the design value very close to the design value achieve the target specifications and with this I can conclude this lecture. Means case study on the fabrication of MEMS accelerometer using the piezoresistive pickup technique. Thank you very much.

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Preview of Next Lecture

Preview of Next Lecture.

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Lecture # 25

MEMS Capacitive Accelerometer

MEMS Capacitive Accelerometer.

Today we will discuss on MEMS capacitive accelerometer. In my last few lectures I spent of MEMS piezoresistive accelerometer, a case study. That is particularly for avionics application, we just describe how a accelerometer is designed and then what will the technology fabrication steps and its characterization and today I want to spend on another case study. That is MEMS capacitive accelerometer that is for generalized application for defense and many other automobile sectors also required such accelerometer. So MEMS capacitive accelerometer a case study that is the topic of discussion today.

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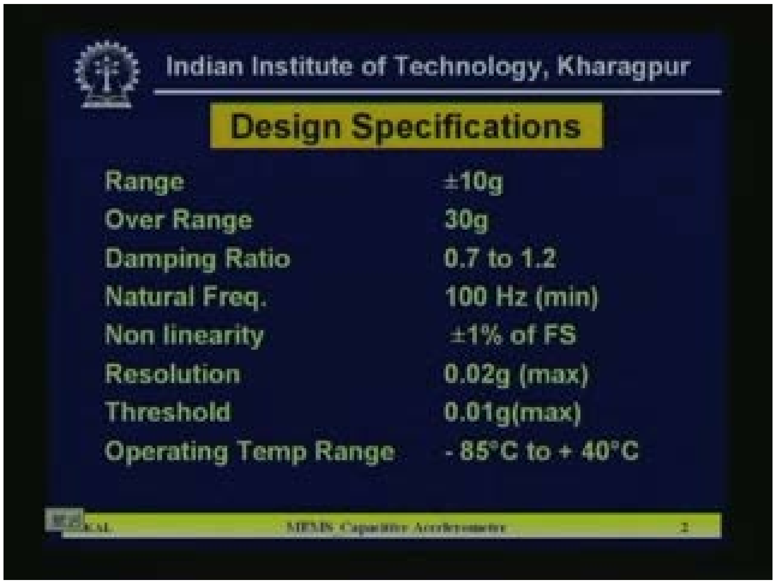

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**Design Specifications**

| | |
|---|---|
| Range | ±10g |
| Over Range | 30g |
| Damping Ratio | 0.7 to 1.2 |
| Natural Freq. | 100 Hz (min) |
| Non linearity | ±1% of FS |
| Resolution | 0.02g (max) |
| Threshold | 0.01g(max) |
| Operating Temp Range | - 85°C to + 40°C |

KAL MEMS Capacitive Accelerometer 2

Now the design specification of that accelerometer is range of the accelerometer is plus minus 10g, over range is 30g. That means up to 30g there is no destruction of the device it should withstand. Damping ratio is 0.7 to 1.2, natural frequency is 100 hertz, non-linearity plus minus 1 percent full scale, resolution 0.02g maximum and threshold is 0.01g maximum, operating temperature range is minus 85 to plus 40 degree C. So now with these specifications, how do you proceed to design a accelerometer which is based on capacitive sensing?

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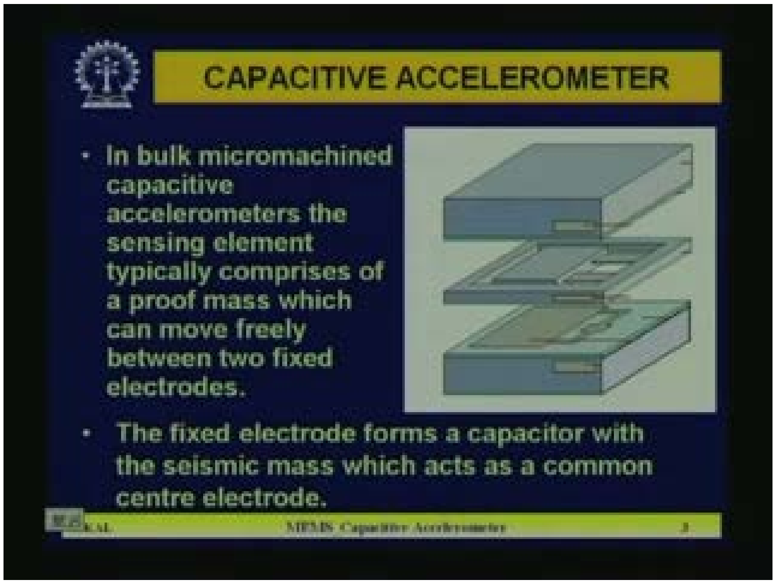

## CAPACITIVE ACCELEROMETER

- In bulk micromachined capacitive accelerometers the sensing element typically comprises of a proof mass which can move freely between two fixed electrodes.
- The fixed electrode forms a capacitor with the seismic mass which acts as a common centre electrode.

Now this structure of the capacitive accelerometer is shown in the figure here you can see. And this figure is 3 modules you can see in the middle piece is basically the sensing element and it comprises of a proof mass which is also known as seismic mass which can move freely between 2 fixed electrodes. What are the 2 fixed electrodes? One is held of the top and another is held at the bottom.