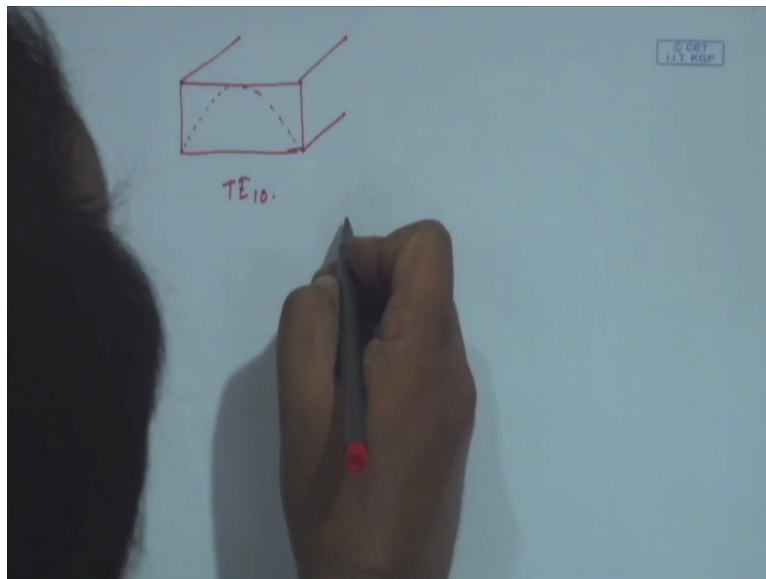


**Millimeter Wave Technology.**  
**Professor Minal Kanti Mandal.**  
**Department of Electronics and Electrical Communication Engineering.**  
**Indian Institute of Technology, Kharagpur.**  
**Lecture-04.**  
**Introduction to Millimetre-Wave Technology (Contd.)**

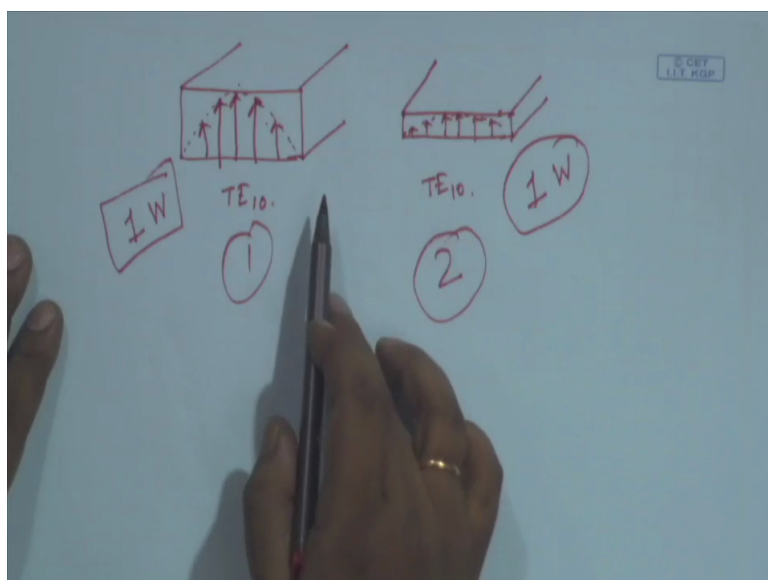
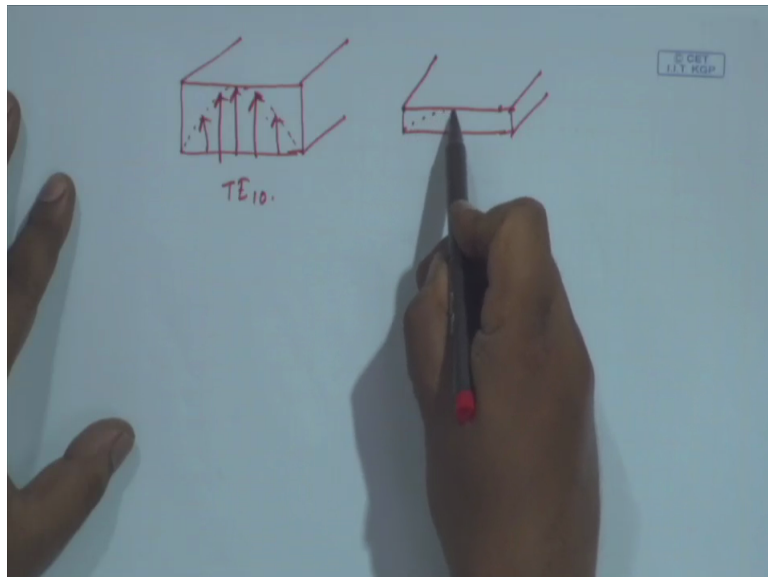
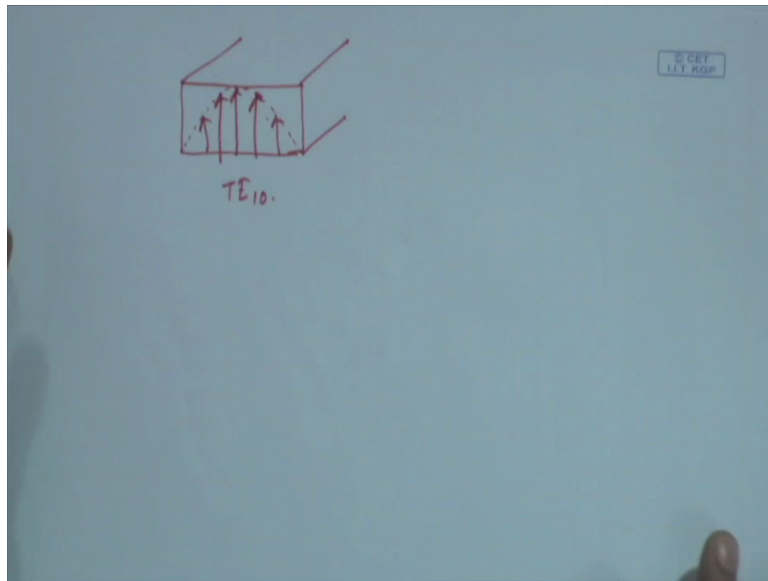
Well so before discussing about other challenges let us see why at millimetre wave frequency power handling capability decreases? And why loss increases at millimetre wave frequency? So there are many sources but because of the reduced size of the wave guide or the wave guiding structure we will see that power handling capability and the loss it increases.

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So let us consider a rectangular wave guide. So this is the cross sectional of a rectangular wave guide let us say it is supporting TE 10 mode so for this TE 10 mode if I plot the electric field strength from left to right side.

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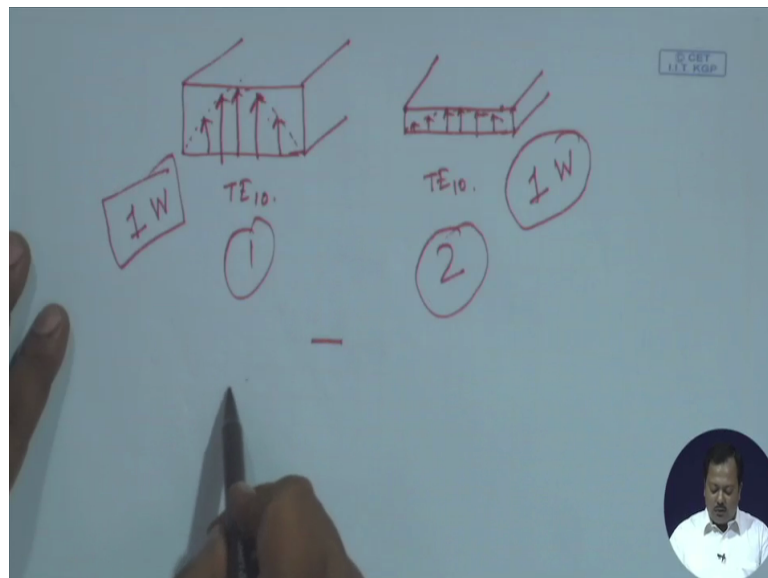


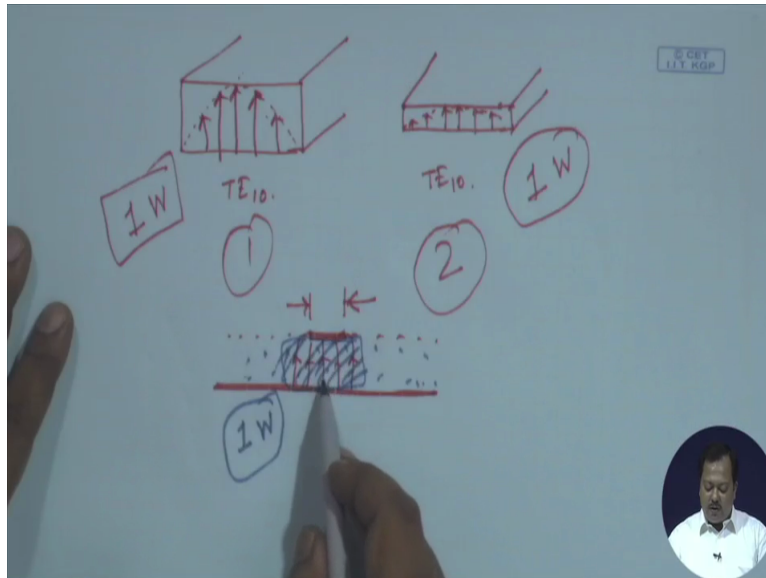
So this is the electric field configuration for TE<sub>10</sub> mode so it is maximum on the mid plane and then if I go left or right side the field decreases. Now I am considering one more rectangular wave guide but its thickness is much smaller compare to this and it is also supporting similar mode TE<sub>10</sub> mode so we have perpendicular electric field components which varies simultaneously along its width.

Now the difference between one and two is that only thickness it changes its width remain same so if I sent now 1 watt of power through rectangular wave guide one and the same power through rectangular wave guide two so now if I calculate the electric field values so obviously in the first case we have much smaller electric field values and whatever current we have maximum current on the mid plane on metal surface.

So obviously that will be much higher for case 2. So since the current component is higher we are expecting more metal loss from case 2 so not only that electric field value as well as the loss both are increasing so power handling capability it will decrease for case 2 as well as loss will increase for case 2. So this is one conceptual explanation why loss increases with reduced height of with the decreasing cross sectional area.

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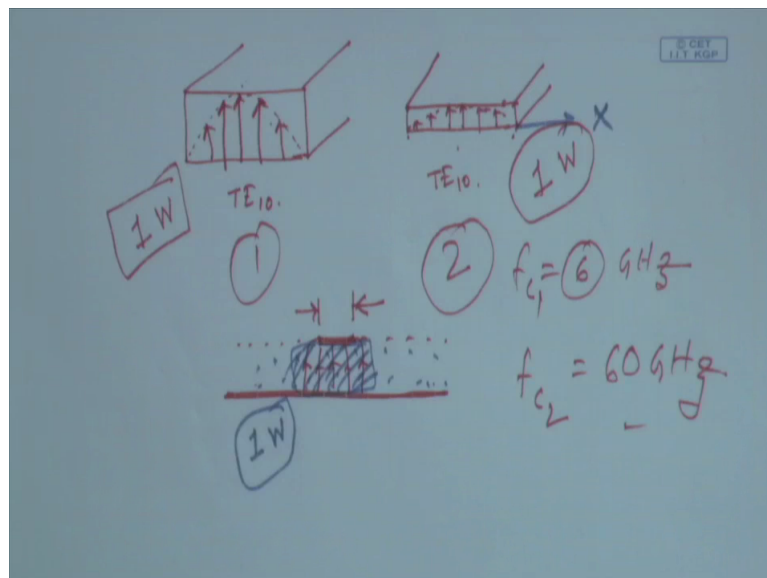
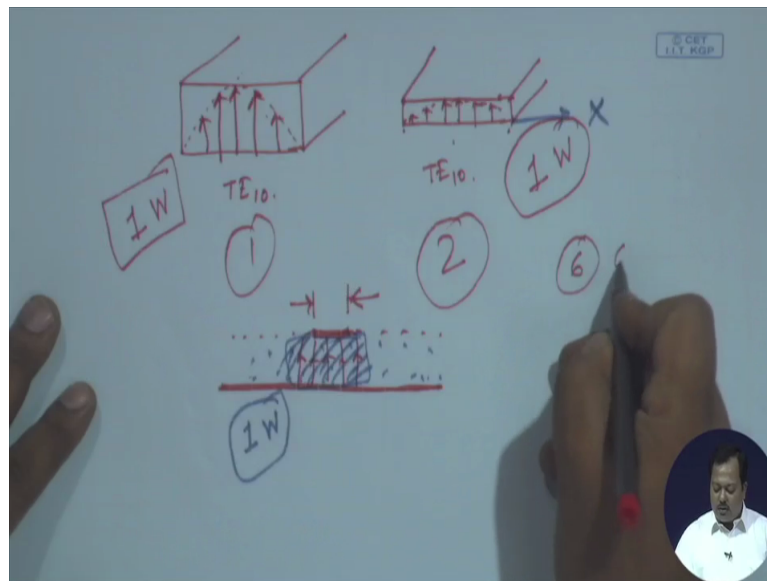




If I consider a micro strip line for example it showing a cross sectional view of a micro strip line so this is the top metallic strip and this is the bottom metal which we called the ground and in between we have dielectric material so in this case the strip width is much smaller compare to  $\lambda_g$  so the energy electromagnetic energy mainly it lies just below this strip and if I draw the electric field it looks like this.

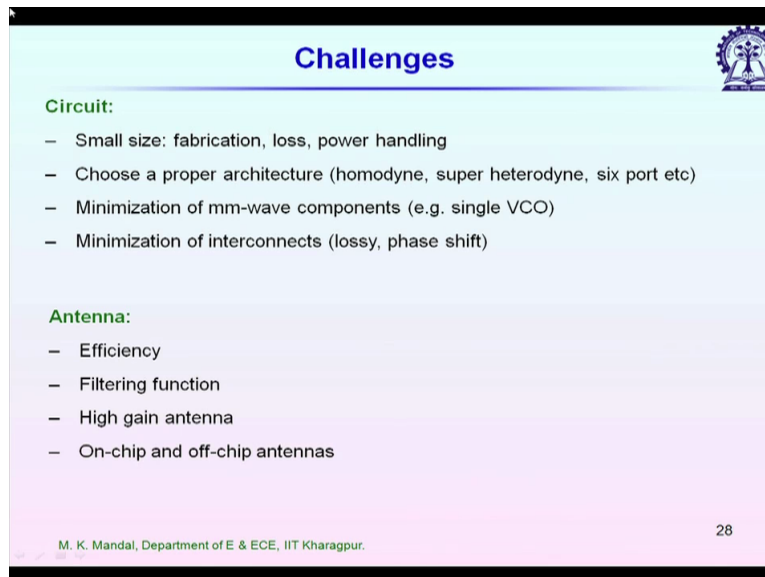
So inside the dielectric I am using a small area for energy propagation so again if I send 1 watt of power through micro strip line what do you expect compare to rectangular wave guide in this case we will be having higher electric field value and higher surface current density. So power handling capability will decrease further and loss will increase further so if I design this rectangular wave guide now let us say at millimetre wave frequency so you know that the diemension along X it depends on wave length for TE 10 mode at start up frequency this width it is approximately  $\lambda$  not by 2.

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So if that is the case then if I design one rectangular wave guide let us say at 6 gigahertz and FC is this is equal to 6 gigahertz case one. And in the second case FC is 60 gigahertz so what we expect for the second case the broad side dimension of the wave guide it ten times smaller than the first case. So it will provide high loss and not only that power handling capability will decrease for the second case so the conclusion is then the if I decrease the cross sectional area of any guiding structure in that case we will have higher loss and lower power handling capability.

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The slide is titled "Challenges" and features a logo in the top right corner. It is divided into two sections: "Circuit:" and "Antenna:". The "Circuit:" section lists four challenges: small size (fabrication, loss, power handling), proper architecture (homodyne, super heterodyne, six port etc), minimization of mm-wave components (e.g. single VCO), and minimization of interconnects (lossy, phase shift). The "Antenna:" section lists four challenges: efficiency, filtering function, high gain antenna, and on-chip and off-chip antennas. The slide footer includes the name "M. K. Mandal, Department of E & ECE, IIT Kharagpur." and the number "28".

**Challenges**

**Circuit:**

- Small size: fabrication, loss, power handling
- Choose a proper architecture (homodyne, super heterodyne, six port etc)
- Minimization of mm-wave components (e.g. single VCO)
- Minimization of interconnects (lossy, phase shift)

**Antenna:**

- Efficiency
- Filtering function
- High gain antenna
- On-chip and off-chip antennas

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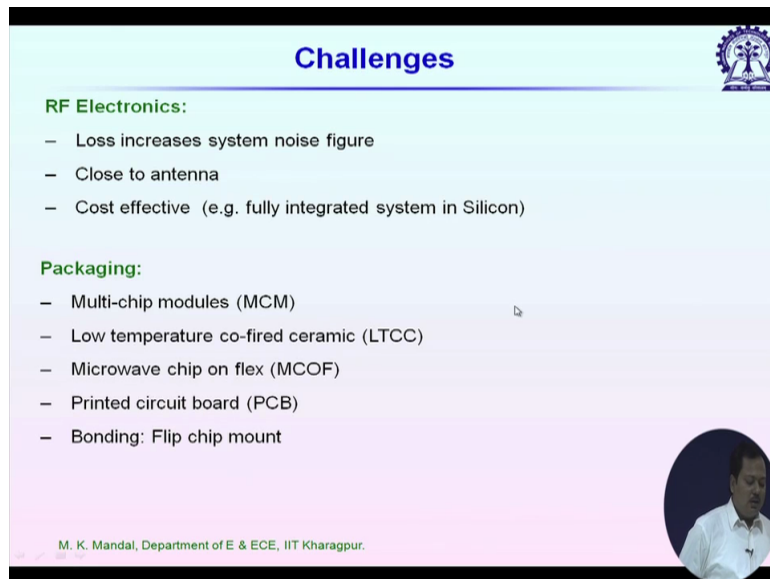
So now let us go back to the challenges. Next is antenna it can be resonating antenna or it can be travelling wave type antenna. So whatever we design at millimetre wave frequency it will give you very low efficiency. Because whatever power you are going to feed to your antenna so a part of that will be radiating and another rest part it will be absorb in the antenna structure itself which is due to the loss.

So as seen that millimetre wave frequencies loss increases antenna efficiency will decrease or radiation efficiency will decrease so its a problem actually at millimetre wave frequency so typical antenna efficiency it can be as small as 10 percent to 20 percent so that means whatever power we are feeding to antenna only 10 percent is being radiating to space.

So not only that if we go for on chip antenna design let us say we are designing the antenna on silicon or silicon dielectric constant is very high almost 12 so if you just place one resonating element on silicon so instead of radiation in space almost all of the power will be absorb in silicon the effect is due to surface wave generation we will see later what is surface wave?

So this type of problem will be facing at millimetre wave frequencies so we have to then use some alternative ways how to reduce this losses? How to improve the gain of the antenna? Next is the filtering function so filter typically use low loss resonators and since we already discussed that if we really on low loss resonator we don't have any other option than increasing the volume. So for small size application then filter design of filter its a challenge.

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**Challenges**


**RF Electronics:**

- Loss increases system noise figure
- Close to antenna
- Cost effective (e.g. fully integrated system in Silicon)

**Packaging:**

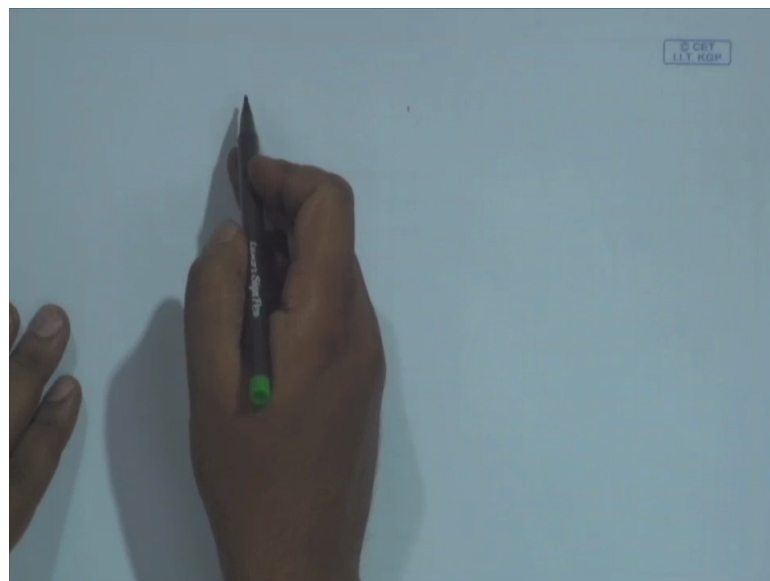
- Multi-chip modules (MCM)
- Low temperature co-fired ceramic (LTCC)
- Microwave chip on flex (MCOF)
- Printed circuit board (PCB)
- Bonding: Flip chip mount

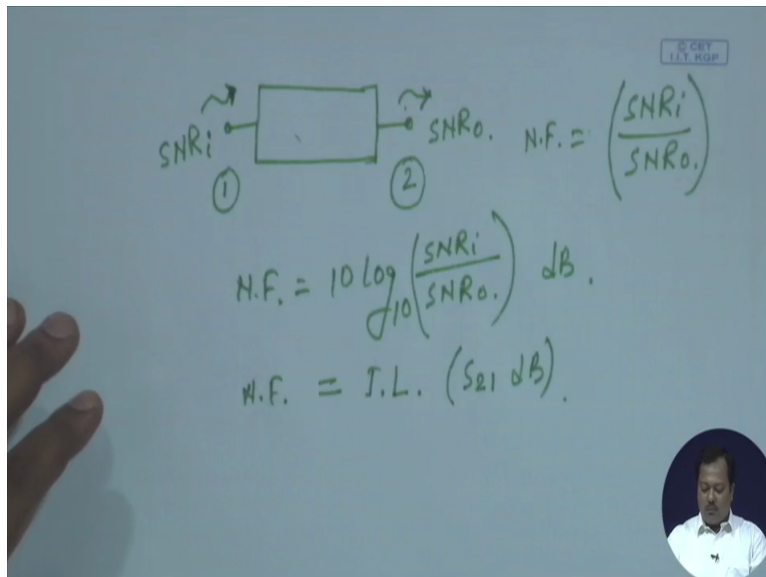
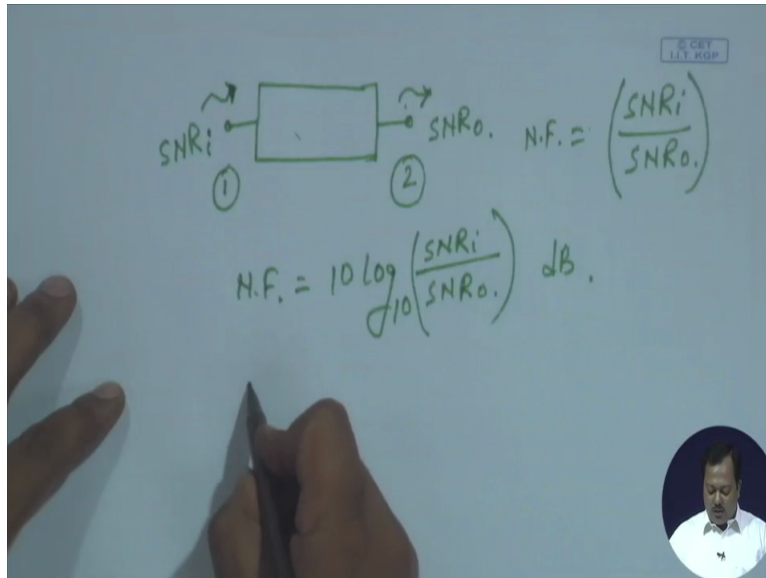
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Next RF electronics part so loss its increases system noise figure so what is noise figure? Okay so let me show you by using some diagram this is another important quantity noise figure.

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Let us say we have a two port network it can be anything it can be a filter, it can be a power amplifier, it can be any two port network. This is port one this is port two. So its receiving some signal at port P1 and then the signal whatever we are collecting at port 2. So let us say the SNR at port 1 its given by S sig signal to noise ratio at port 1 its given by SNR i and the signal to noise ratio at port 2 its given by SNR O so now if I take the ratio.

SNR at the input and SNR at the output usually we represent it in decibel scale we call it the noise figure. So usually the noise figure it is represented in decibel scale 10 log 10 SNR at the input divided by SNR at the output in DB. So for a lossy system for any given passive network let us say filter it will increase the noise figure why? Because whatever signal is coming at the input port due to the loss the signal component will be attenuated further.



And at the same time this component will add some noise so at the output total noise contribution is increasing but total signal strength is decreasing so as a result what we expect that noise figure will increase so at millimetre wave frequency this term noise figure is very popular by these we can understand how noisy the component is?

It may be any active component like power amplifier low noise amplifier, mixer or it can be also passive element like filter, coupler. So for passive element usually the noise figure this is equal to the insertion loss insertion loss of that component for passive element so insertion loss is nothing but a  $S_{21}$  in DB.

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**Challenges**

**RF Electronics:**

- Loss increases system noise figure
- Close to antenna
- Cost effective (e.g. fully integrated system in Silicon)

**Packaging:**

- Multi-chip modules (MCM)
- Low temperature co-fired ceramic (LTCC)
- Microwave chip on flex (MCOF)
- Printed circuit board (PCB)
- Bonding: Flip chip mount

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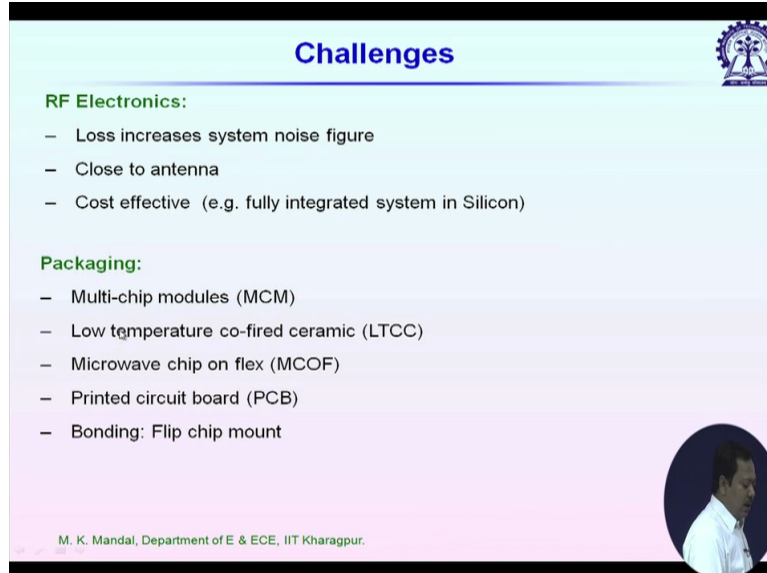
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So let us go back, so then we see that at millimetre wave frequency loss increases so it increases the noise figure of the component. So one way to decrease the no overall noise figure of any transmitter or receiver is that a first element of the chain of the component of the let us say for receiver if I start from antenna. Just after antenna we have low noise amplifier then mixer component so the first element should provide minimum noise figure and it should be placed at close to antenna as possible.

So that we can decrease the overall noise figure of the system and finally the system must be cost effective because if we use group 3 group 5 semi conductor materials like gallium arsenide to fabricate millimetre wave system it is not cost effective. So that is why till now it is popular only with the defence sector who can afford this expensive system. So if we really want any consumer application we have to find out low cost solution and that is possible if we fabricate the same system using silicon germanium technology of CMOS by CMOS

technology. So already some of the university group and some research lab they did it at 60 gigahertz using silicon technology.

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The slide is titled "Challenges" and is presented on a light blue background with a purple gradient at the bottom. It features a logo of a tree in a circle in the top right corner. The content is organized into two sections: "RF Electronics:" and "Packaging:". The "RF Electronics:" section lists three bullet points: "Loss increases system noise figure", "Close to antenna", and "Cost effective (e.g. fully integrated system in Silicon)". The "Packaging:" section lists four bullet points: "Multi-chip modules (MCM)", "Low temperature co-fired ceramic (LTCC)", "Microwave chip on flex (MCOF)", "Printed circuit board (PCB)", and "Bonding: Flip chip mount". At the bottom left, the text reads "M. K. Mandal, Department of E & ECE, IIT Kharagpur." In the bottom right corner, there is a circular inset photograph of a man in a white shirt.

**Challenges**

**RF Electronics:**

- Loss increases system noise figure
- Close to antenna
- Cost effective (e.g. fully integrated system in Silicon)

**Packaging:**

- Multi-chip modules (MCM)
- Low temperature co-fired ceramic (LTCC)
- Microwave chip on flex (MCOF)
- Printed circuit board (PCB)
- Bonding: Flip chip mount

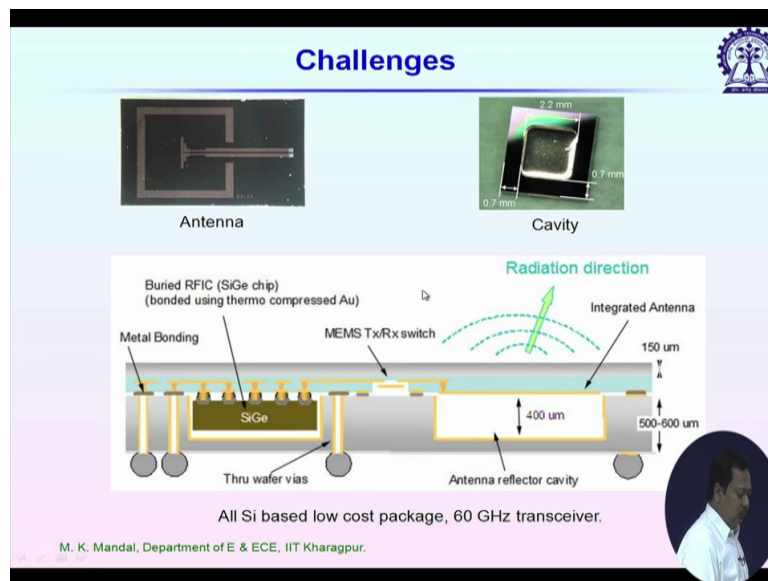
M. K. Mandal, Department of E & ECE, IIT Kharagpur.

So next is packaging another important issue. So whatever components we are designing we have to put it under some packaging to protect it from severe weather condition and we have different packaging systems one is called multi chip module. So where basically different chips or different functions are integrated together in one single chip and from and then it is put under one single package.

So from outside you cannot understand that inside there are many chips. So this MCM or multi chip modules it can be fabricated using low temperature co-fired ceramic technology or more popularly known as LTCC using microwave chip on flex so basically its a one type of flexible laminates also we can use conventional printed circuit board technology or laminates to integrate this multiple chips and next then how to connect the chip with the other component.

So for that we have to use some sort of bonding so wire bonding or it can be flip chip mount we will see it later. At millimetre wave frequency usually wire bonding is lossy, flip chip mount is less lossy but it has some additional problem of power leakage and coupling and generation of surface wave modes.

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So this is showing a typical scenario one on the chip antenna you can see the copper part fabricated on silicon but the problem is that if we directly fabricate one antenna on silicon most probably it is not going to radiate anything. So almost all of this power it will be absorbed by the silicon.

So then how we can make it radiate so one alternative solution is that use one AR cavity just below this antenna structure so this right hand side picture actually showing that AR cavity and this antenna then it is placed on the AR cavity so now it will radiate into space so this is one solution how we can improve the gain of the antenna so now the second picture this is showing a silicon based low cost gigahertz transceiver.

So this antenna now it is being integrated in the single chip where we have other components like low noise amplifier and switching and everything all are millimetre wave components so when we integrate antenna inside the same chip we have to take care of many factor for example this antenna is resonating structure it has some  $(\text{E})^2$  electric field in silicon and air so it can interact with other metallic part of this chip itself.

So then antenna it should be placed as far as possible from the chip not only that if there is any metal part on this chip itself then we have to use some sort of insulator in between antenna and the chip part or simply we have to increase the separation between antenna and this chip part.


Now if I look at this chip then the passive components typically the inductors it occupies very large area and usually they are fabricated on the top metal layer of the chip so the coupling

between the inductors and the antenna it is expected to be maximum so sometimes that's why to avoid that coupling between the inductor and the antenna we use some sort of guard ring around the antenna structure which will minimize the coupling between antenna and the inductors.

So you can also see this is since silicon substrate so they are using that AR cavity so this is the radiator and just below it we have this 400 micrometre thick AR cavity so it's just below the AR cavity we have antenna reflector cavity this is just metallisation on the cavity wall so which behaves as a reflector and further increases the gain.

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**Substrate parameters**



RT/duroid 5870/5880 Laminates

PROPERTY	TYPICAL VALUE <sup>(1)</sup>				DIRECTION	UNITS <sup>(2)</sup>	CONDITION	TEST METHOD
	RT/duroid 5870		RT/duroid 5880					
Dielectric Constant, $\epsilon_r$ Process	2.33		2.20		Z	N/A	C24/23/50 C24/23/50	1 MHz IPC-TM-650 2.5.5.3 10 GHz IPC-TM-2.5.5.5
	2.33 + 0.02 spec.		2.20 + 0.02 spec.					
Dielectric Constant, $\epsilon_r$ Design	2.33		2.20		Z	N/A	8 GHz - 40 GHz	Differential Phase Length Method
Dissipation Factor, $\tan \delta$	0.0005		0.0004		Z	N/A	C24/23/50 C24/23/50	1 MHz IPC-TM-650, 2.5.5.3 10 GHz IPC-TM-2.5.5.5
	0.0012		0.0009					
Thermal Coefficient of $\epsilon_r$	-115		-125		Z	ppm/°C	-50 - 150°C	IPC-TM-650, 2.5.5.5
Volume Resistivity	2 X 10 <sup>14</sup>		2 X 10 <sup>14</sup>		Z	Mohm cm	C96/35/90	ASTM D257
Surface Resistivity	2 X 10 <sup>12</sup>		3 X 10 <sup>12</sup>		Z	Mohm	C96/35/90	ASTM D257
Tensile Modulus	Test at 23°C	Test at 100°C	Test at 23°C	Test at 100°C	N/A	MPa (ksi)	A	ASTM D638
	1300 (189)	490 (71)	1070 (156)	450 (65)	X			
ultimate stress	1280 (185)	430 (63)	860 (125)	380 (55)	Y	%		
	50 (7.3)	34 (4.8)	29 (4.2)	20 (2.9)	X			
ultimate strain	42 (6.1)	34 (4.8)	27 (3.9)	18 (2.6)	Y	MPa (ksi)		
	9.8	8.7	6.0	7.2	X			
Compressive Modulus	9.8	8.6	4.9	5.8	Y			
	1210 (176)	680 (99)	710 (103)	500 (73)	X			
	1360 (198)	860 (125)	710 (103)	500 (73)	Y			
	803 (120)	520 (76)	940 (136)	670 (97)	Z			
	30 (4.4)	23 (3.4)	27 (3.9)	22 (3.2)	X			

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Now let us say we are going for a practical design. We want to design some millimetre wave components at using some printed circuit board technology so for that we have to choose a printed circuit board first. What is printed circuit board? It is nothing but a dielectric slab and it comes with a top and bottom copper (())(19:48) metal.

So if you take the cross section the dielectric layer it is sandwiched between two metal layer and what is the thickness of dielectric we have some standard thickness available and just if you companies actually make this substrate we call it substrate and some standard dielectric constant also available so one of the popular company name is Rogers corporation from USA.

So if you go through Rogers website you can see that it's coming with some standard thickness as well as with some standard dielectric constant so for example if I consider a typical substrate its name is RT duroid 5880 its dielectric constant is 2.2 and if you go

through Rogers website you will find out some typical thickness like 5mil 1mil equal to 1000 of one inch.

So 10 mil, 20 mil, 32 mil some standard thickness are only available you don't have any value in between so you have to choose first your substrate. So how to choose your substrate first? So we have to keep many factors many parameters in mind when we are going to choose your substrate so for example if I increase dielectric constant of the substrate what will happen? The components size will decrease. Why?


Already we discussed that  $\lambda_g$  this is the call to approximately  $\lambda$  not by root epsilon R so if I design a resonator  $\lambda_g$  by 2 length at least say in a substrate with dielectric constant 10.2 and we have one more substrate of dielectric constant 2.2 so obviously it will be of small size in 10.2 dielectric constant substrate. So then obviously we have some advantage we can miniaturise component.

But at millimetre wave frequency already the components size is small and not only that if we go for miniaturisation we face one more problem. What is that? Loss increases as well as power handling capability decreases. Different substrate provides different loss value that loss we want we we quantify by using a parameter we call it loss tangent of the substrate so we will see later.

So loss tangent that is another important factor for any given substrate higher at the loss tangencies higher the dielectric losses so when you are choosing your substrate for your application you have to keep all this points in mind and now let us visit through Rogers page and find out how the specifications are given.

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**Substrate parameters**



RT/duroid 5870/5880 Laminates

PROPERTY	TYPICAL VALUE <sup>10</sup>		DIRECTION	UNITS <sup>10</sup>	CONDITION	TEST METHOD	
	RT/duroid 5870	RT/duroid 5880					
<sup>10</sup> Dielectric Constant, $\epsilon_r$ <small>Residual</small>	2.33 2.33 ± 0.02 spec.	2.20 2.20 ± 0.02 spec.	Z Z	N/A	C24/23/50 C24/23/50	1 MHz IPC-TM-650 2.5.5.3 10 GHz IPC-TM-2.5.5.5	
<sup>10</sup> Dielectric Constant, $\epsilon_r$ <small>Design</small>	2.33	2.20	Z	N/A	8 GHz - 40 GHz	Differential Phase Length Method	
Dissipation Factor, $\tan \delta$	0.0005 0.0012	0.0004 0.0009	Z Z	N/A	C24/23/50 C24/23/50	1 MHz IPC-TM-650, 2.5.5.3 10 GHz IPC-TM-2.5.5.5	
Thermal Coefficient of $\epsilon_r$	-115	-125	Z	ppm/°C	-50 - 150°C	IPC-TM-650, 2.5.5.5	
Volume Resistivity	2 X 10 <sup>10</sup>	2 X 10 <sup>10</sup>	Z	Mohm cm	C/96/35/90	ASTM D257	
Surface Resistivity	2 X 10 <sup>10</sup>	3 X 10 <sup>10</sup>	Z	Mohm	C/96/35/90	ASTM D257	
Tensile Modulus	Test at 23°C	Test at 100°C	Test at 23°C	Test at 100°C	N/A	A	ASTM D638
	1300 (189)	490 (71)	1070 (156)	450 (65)	X		
	1280 (185)	430 (63)	860 (125)	380 (55)	Y		
	50 (7.3)	34 (4.8)	29 (4.2)	20 (2.9)	X		
ultimate stress	42 (6.1)	34 (4.8)	27 (3.9)	18 (2.6)	Y	%	
	9.8	8.7	6.0	7.2	X		
ultimate strain	9.8	8.6	4.9	5.8	Y	MPa (kpsi)	
	1210 (176)	680 (99)	710 (103)	500 (73)	X		
Compressive Modulus	1360 (198)	860 (125)	710 (103)	500 (73)	Y	MPa (kpsi)	
	803 (120)	520 (76)	940 (136)	670 (97)	Z		
	30 (4.4)	23 (3.4)	27 (3.9)	22 (3.2)	X		

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So for example I am considering a typical RT duroid 5870 substrate and RT duroid 5880 substrate so this page I am showing from Rogers corporations website this is the data sheet so you can see dielectric constant epsilon R some suggested values are given they are calling it the design value. For 5870 its 2.33 for 5880 it is 2.2.

And not only that if I go to right the suggested frequency range is 8 gigahertz to 40 gigahertz so they are specifying this dielectric constant value for design from 8 to 40 gigahertz if I increase the frequency further so that means dielectric constant may vary it may not be fixed at 2.33 or 2.2. So similarly the dissipation factor or loss tangent another name is tan delta so you see for 5870 they are suggesting two values point 0005 this is at 1 megahertz and below point 0012 this is at 10 gigahertz for 5880 these values are point 0004 and point 0009.

So you see as the frequency increases what they are showing the measured loss tangent values they are increasing but we will see theoretically loss tangent should take place but practically if I look at the measured value loss tangent is increasing with frequencies. There are many other factors like what is the thermal co efficient of epsilon R so epsilon R its changing with frequency not only that epsilon R its also a function of temperature consider any space based application.


In space temperature can be as low as minus 60, minus 70 degree centigrade or if any component is under constant sunlight illumination so the temperature can be as high as 100 degree or even more than that we have a wide range of temperature this component should support is variation.

So dielectric constant whatever we are using to design that components then it should not vary with temperature in fact there are only few space certified components for the space certified components the dielectric constant or whatever change in dielectric constant its really small, negligibly small.

So depending on application you have to choose your substrate very carefully for example if you go for any space based application you have to only choose space certified substrate. So with this some there are additional parameters like what is the young modulus of your substrate? What is the vapour absorption coefficient of your substrate because if the dielectric it absorbs vapour so water is very lossy and if it absorbs vapour dielectric substrate it will become very lossy.

(Refer Slide Time: 27:33)

### Substrate parameters




RT/duroid 5870/5880 Laminates

PROPERTY	TYPICAL VALUE <sup>1)</sup>				DIRECTION	UNITS <sup>2)</sup>	CONDITION	TEST METHOD
	RT/duroid 5870	RT/duroid 5880	RT/duroid 5870	RT/duroid 5880				
<sup>1)</sup> Dielectric Constant, $\epsilon_r$ Process	2.33 2.33 + 0.02 spec.	2.20 2.20 + 0.02 spec.	Z	Z	N/A	C24/23/50 C24/23/50	1 MHz IPC-TM-650 2.5.5.3 10 GHz IPC-TM-2.5.5.5	
<sup>1)</sup> Dielectric Constant, $\epsilon_r$ Design	2.33	2.20	Z	Z	N/A	8 GHz - 40 GHz	Differential Phase Length Method	
Dissipation Factor, $\tan \delta$	0.0005 0.0012	0.0004 0.0009	Z	Z	N/A	C24/23/50 C24/23/50	1 MHz IPC-TM-650, 2.5.5.3 10 GHz IPC-TM-2.5.5.5	
Thermal Coefficient of $\epsilon_r$	-115	-125	Z	Z	ppm/°C	-50 - 150°C	IPC-TM-650, 2.5.5.5	
Volume Resistivity	$2 \times 10^{10}$	$2 \times 10^{10}$	Z	Z	Mohm cm	C96/35/90	ASTM D257	
Surface Resistivity	$2 \times 10^9$	$3 \times 10^9$	Z	Z	Mohm	C96/35/90	ASTM D257	
Tensile Modulus	Test at 23°C	Test at 100°C	Test at 23°C	Test at 100°C	N/A	A	ASTM D438	
	1300 (189)	490 (71)	1070 (154)	450 (63)	X			
ultimate stress	1280 (185)	430 (63)	860 (125)	380 (55)	Y	A	ASTM D438	
	50 (7.3)	34 (4.8)	29 (4.2)	20 (2.9)	X			
ultimate strain	42 (6.1)	34 (4.8)	27 (3.9)	18 (2.6)	Y	A	ASTM D438	
	9.8	8.7	6.0	7.2	X			
Compressive Modulus	9.8	8.6	4.9	5.8	Y	A	ASTM D438	
	1210 (176)	680 (99)	710 (103)	500 (73)	X			
Compressive Modulus	1360 (198)	860 (125)	710 (103)	500 (73)	Y	A	ASTM D438	
	803 (120)	520 (76)	940 (136)	670 (97)	Z			
Compressive Modulus	30 (4.4)	23 (3.4)	27 (3.9)	22 (3.2)	X	A	ASTM D438	
	30 (4.4)	23 (3.4)	27 (3.9)	22 (3.2)	X			

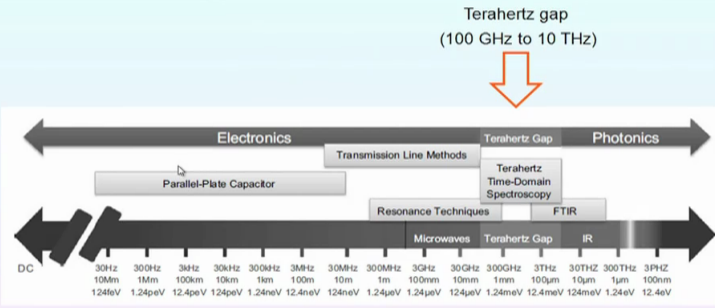
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M. K. Mandal, Department of E & ECE, IIT Kharagpur.

### Dielectric properties at mm-wave and terahertz




Terahertz gap  
(100 GHz to 10 THz)



Various popular material characterization techniques at different frequencies

M. K. Mandal, Department of E & ECE, IIT Kharagpur.



So there are many other factors so we have to keep in mind. So in the next part we will see what are the different material properties at millimetre wave frequencies and not only that even at terahertz frequencies. So sometime we use the same material for microwave frequency designs circuit design.

And as well as for the millimetre wave frequency design but then since already we know that dielectric constant its a function of frequency then how are these material behaves at millimetre wave or sub millimetre wave frequency. Okay so we will take a short break then we start again.