Analog Integrated Circuit Design
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Lecture No - 14
Two Stage Miller Compensated Opamp

Hello and welcome to lecture 14 of Analog Integrated Circuit Design, in the previous lecture we tried to make a matter of an and we were met with through the analysis to see whether it is better are not.

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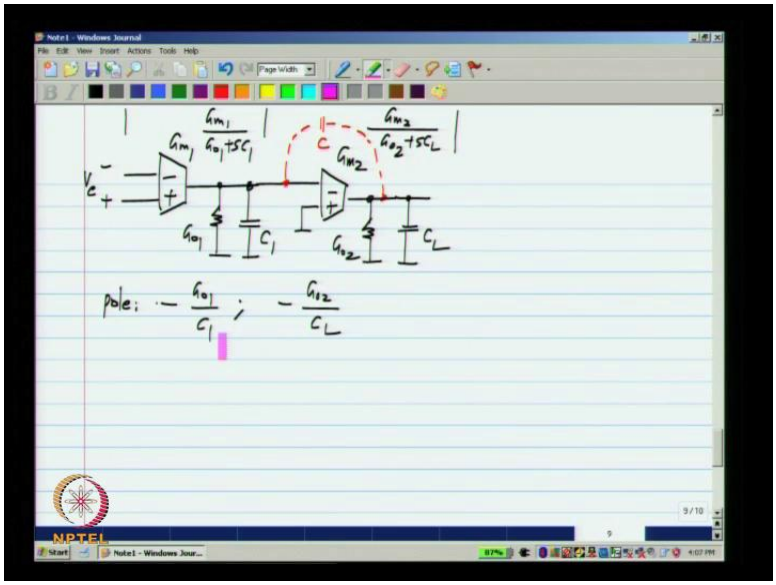

And the topology of the Op Amp that we came up with was like this, the first trans conductor converts the input voltage to a current. And that is passed through a current control voltage source might using a second Op Amp, which is simply this G m 2 and C L and the current voltage conversion happens because, of the C that is connected from the input to the output of this Op Amp.

This is basically a current control voltage source of a trans impedance 1 over s c, we derived the transfer function of this Op Amp. And we saw that the transfer function as 1 0 and 2 poles, and we were trying to make a intruding sense of the poll values that we obtained. And to do that, what we also did was we removed this C and evaluated the poll values, which turns out is very easy to do G o 1 by c l and G o 2 by C L.

Now, when we do have the C, we will get these pole values this complicated thing here and that complicated thing there. And this first one we made intuitive some sort out of by seeing that, it is 0 1 divided by some other capacitance initially we had G o 1 by C 1. Now, we have G o 1 by C 1 plus miller multiplied by C and we also saw why miller multiplication happens, similarly now for the second poll it is G o 2 by C L. First of all even then numerator as changed it is G o 2 plus some other terms, which represent conductress, and in the denominator we have C L plus all of this term. So, what does this make sense indeed does as will see shortly.

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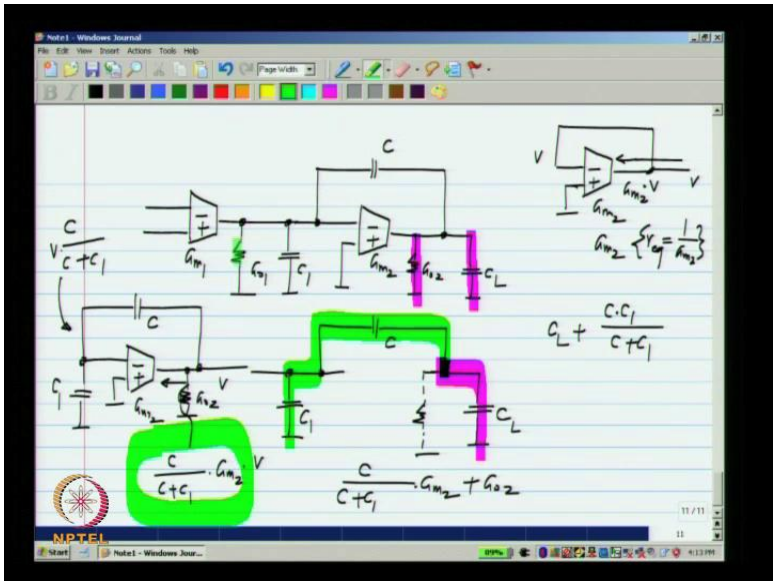

So, again let me repeat the Op Amp that we have G m 1, G o 1, C 1, G m 2, G o 2 and C L and we have C from there to their. So, now, reason ally the conductance hear was 0 to now it appears it be something different, originally the capacitance here was C L, but it again appears to be something different. So, again what we can do is to examine the network around is, and we also know that poles are characteristics of the circuit they have nothing to do where the input is applied. So, we can examine the circuit with a 0 input are determined the polls.

So, when we have 0 input this a conductor G m 1 is as good as not being there, so circled we have is something like that, I will draw only the capacitances C, C 1 and C L. And I do this, and I also try and see what is the capacitance associated with this node that is

from this node to ground. And I do this because, this is where 0 2 or right with this is 0 2 is, originally we had only G o 2 and C L from this node to ground.

Now, we have some conductance and some more complicated network of capacitances, but it is not all that complicated all we have is this C L in parallel with the serious combination of C and C 1. So, what does that give you the total capacitance will simply be C L plus C C 1 by C plus by C 1, and if we go back to the expression you see that the denominator is exactly that it is simply load capacitance plus the serious combination of C and C 1 that is all.

Similarly, now the conductance the term in the numerator seem to contain some G m 2, whereas G m 2 is the trans conductance how did this happen, I think all of you aware that you can take a trans conductance G m 2 or a voltage control current source. And make it appear like a conductance using the feedback, what does the trans conductance do if I have some voltage here, it draws a current G m 2 times V.

If I connect an input and output together what does it mean, if I have a voltage hear it draws the same the current from that voltage. And what is that that is nothing, but a resistor or a conductance, if you have voltage and you draw there is an element which draws the current that is proportional to the voltage. That is nothing, but a conductance, and the conductive of this is G m 2 or the resistance is 1 over G m 2.

So, something like this must be happening that is the trans conductor is an feedback, and that is why we are ending up with I conductance which has a term containing the trans conductance G m 2. And clearly there is indeed feedback here, you see that there is feedback with C and C 1 around G m 2, now I will draw only that part of the network if I apply voltage V, the voltage here will be C primes C by C plus C 1 it is simply a capacitor division of the voltage V, and a current drawn hear will be that voltages times G m 2.

So, that is nothing, but C by C plus C 1 times G m 2 times V, so clearly this entire network as for other contribution of the trans conductance is concerned, looks like a conductance of that value. So, the trans conductance because, it is in feedback contribute a conductance of C by C plus C 1 times G m 2, in this case it is equal to G m 2 because, all of this way was feedback to the input, here only a fraction of V is feedback to the input.

So, it is smaller than G m 2, but nonetheless related to G m 2, so that is the conductance contributed by G m 2 in addition to this here G o 2 itself over there. So, we have expect that will have C by C plus C 1 times G m 2 plus G o 2, and indeed if you look at the expression we have G o 2 plus the effect of G m 2 being in feedback. Now, we also have this extra term because, what we have here is not only C 1 we have G o 1 in parallel.

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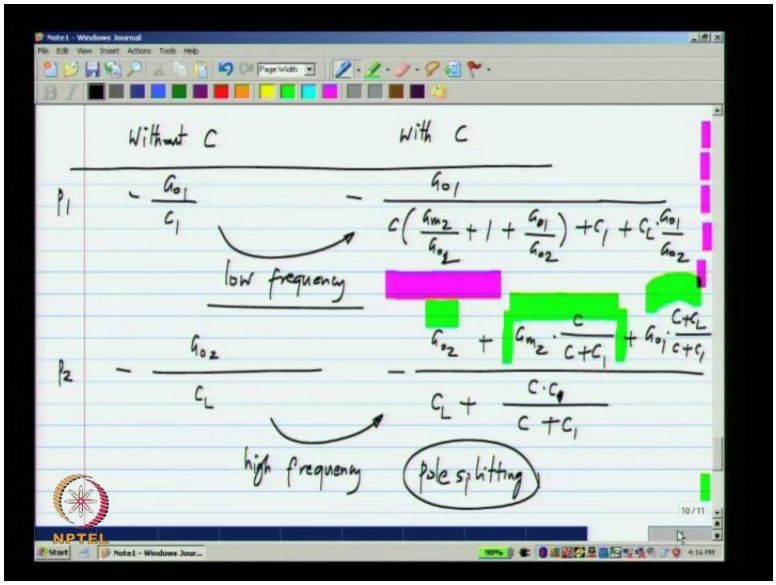

So, that gives you some extra terms because, if you did not have G o 1 at all you would have only this capacitive network we also have G o 1 here and that gives you some conductive portion which is related to G o 1. But, typically you expect that G m 2 is much more than G o 1 and G o 2, so in fact, the dominant conductance is the expected to be this medium term here, this one alone and other two will be smaller.

So, although again whereas, the expression looks complicated it is very easy to make introduce sense out of it, it is again some conductance. Were some capacitance the conductance happens to come from the output conductance of the second stage, as well as the trans conductance being in feedback. Similarly the capacitance comes from the load connected to the second stage, which is C l plus the series combination of C and C 1 because, that how their connected in the circuit.

Also another thing we absorbed was that this P 1 which was minus G o 1 by C 1 without C move to a lower frequency. Because, the apparent capacitors increased now what happens to P 2 it is G o 2 by C L and here will see that both numerator and denominator

have changed. The numerator as increased the denominator also as increased, but it is important to keep in mind that G m 2 is expected to be much, much more than G o 2. If I that is how you get gain, the gain of the second stage is G m 2 by G o 2 and you expect the DC gain to be at least 10 if not in many times of 100's.

Whereas, the capacitance was become C L plus some value, which you generally expected to be as to same order of C L same order as C L or even smaller. So, the denominator increase, but only modestly the numerator increases enormously, so it turns out that this P 2 moves to high frequency compared to the case where we did not have a C, we considered the case without C only because, poles were easy to calculate.

And also it turns out that it is a common scenario, you have one amplifier after another, and if you cascade a number of amplifier. So, you get a number of poles from each amplifiers output, now in our case we have to 2 amplifiers one after another, and our Op Amp looks like such a structure with 2 amplifiers, and a capacitor connected from the input and output of the second stage. And when you do that it turns out that, one pole moves to a lower frequency and another pole most higher frequency, so such a thing is known as poles splitting.

So, it turns out the that is in fact, the useful thing you to have when we are trying to make Op Amp's. Because, after all what we want, we wanted the Op Amp to behave like an integrator that is a single pole system, and we also saw from stability criteria that if you have extra poles at all, they should be a much higher frequencies. Now, here in this case what happens is one of the poles most to higher and higher frequencies, and that is a good thing for an Op Amp as we will see also in future analysis. So, in summary the new Op Amp that we came up with as 2 poles and a 0, and the poles are given by these expressions. And the 0 all we already determined it is at plus G m 2 divided by C.

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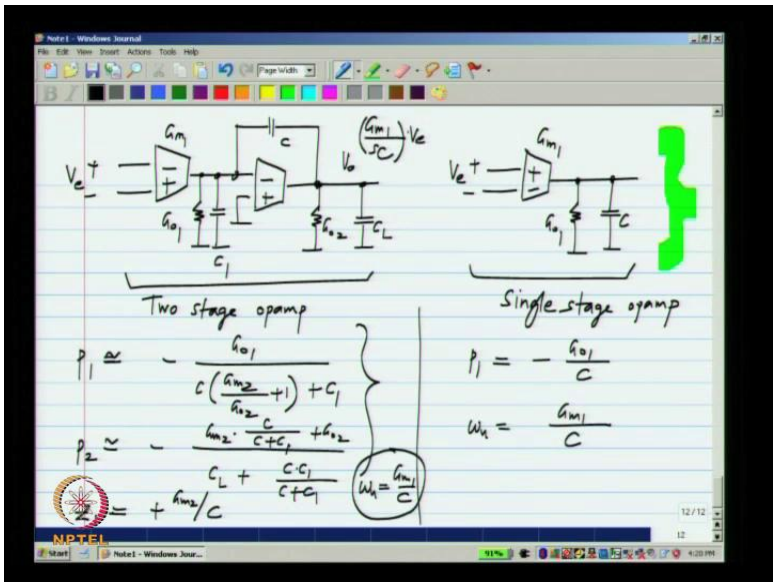

So, this because, it has 2 trans conductance stages, one after another it is known as two stage Op Amp and or earlier Op Amp which as a single trans conductance stage, loaded by capacitors this is known as a single stage Op Amp. And in each of these cases you could use voltage buffers after these Op Amp, but like a mentioned earlier voltage buffers are order to make in the CMOS technology, it specially with low voltages, low supply voltages.

So, we typically tend to use this Op Amp's without expected buffers, these things will become clearer one when we come to circuit realization of this Op Amp's. And this as 2 poles I will write only the approximate values here, it also have a 0 which is at plus G m 2 by C. Whereas the single size Op Amp's if you recall it as a single pole at minus G o 1 divided by C.

Now, what is the unity gain frequency of the single size Op Amp that is nothing, but G m 1 divided by C. And what is the unity gain frequency of the two stage Op Amp it is also G m 1 by C because, after all they recall how we came of this topology, we have this trans conductance G m 1 whose output current is passed through this capacitor, by putting a capacitance feedback around a second Op Amp. So, that we form a second current control voltage source. So, the approximate transfer function from the input to the output is still G m 1 by S C times V. So; that means, that the unity gain frequency here is G m 1 by C as well and this can also be verified very easily.

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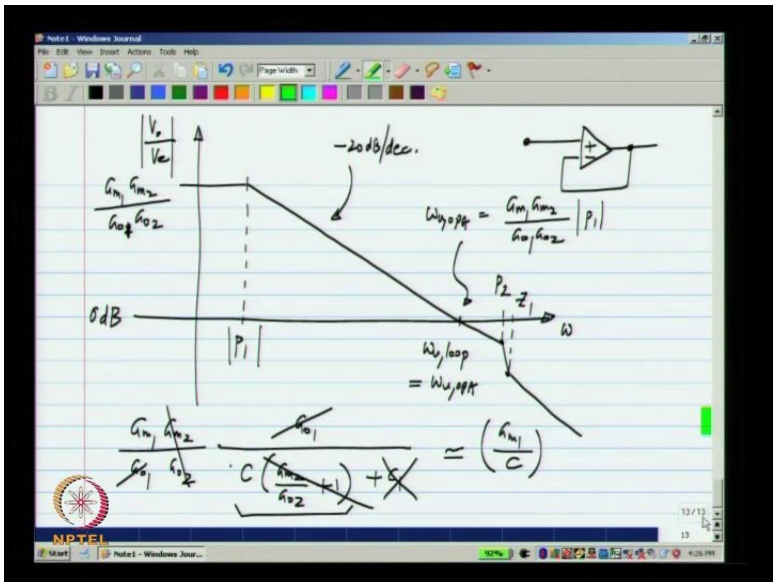

If you draw the magnitude response of the two stage Op Amp, it will have a DC gain of G m 1, G m 2 by G o 1, G o 2 which is the product of the DC gain of two stages. And there is a pole, and at that point there will be a breakpoint and the gain drops at 20 degree per decades. And then at some frequency there will be a second pole P 2, and then some other frequency there will be a 0 G 1 I was assume that P 2 is smaller than G 1 which may or may not be decades.

Now, here you see that the behavior is first out order all the way down to P 2 and this is the 0 d B line I am assuming that the behavior is first-order all the way down to 0 d B line. This we anyway know as to be true for good stability, from our earlier study of bode plots and nyguist criteria, we are seen that the system as to maintain, the loop gain as to maintain first-order dependence of frequently all the way down to unity loop gain frequency.

Now, if we place this Op Amp or two stage Op Amp in unity feedback, the unity loop gain frequency of this feedback loop is nothing, but the unity gain frequency of the Op Amp itself. So, we will assume that we are made a unity gain feedback configuration like this, so in this case the unity loop gain frequency will be the unity gain frequency of the Op Amp. And first-order behavior as to be maintained all aware down there and because, this is first-order behavior, this frequency is easily seen to be the product of this DC gain and this pole times to magnitude of P 1.

And if we evaluate that P 1 is nothing, but G o 1 by, so that cancels with that and this approximate the cancels with that, and this C times G m 2 by G o 2 plus 1 is a much larger than C 1. So, the C 1 can be neglected and then this G m 2 by G o 2 term cancel G m 2 by G o 2 plus 1 because, G m 2 by G o 2 is the number is much more than 1, so the unity gain frequency approximately is G m 1 by C. Now, remember this is the unity gain frequency that is we were trying to implement, so it is not surprising at all that we get the same number.

But, just wanted to show that when you calculated without knowing a anything about the circuit, you simply calculated as a product of the DC gain and first pole. Assuming that first order behavior is maintained all the way down to 0 d B gain, you will get the same answer. And it is nothing, but the unity gain frequency the single size Op Amp we start offs with, after all we made this as an improvement to that one without changing the unity gain frequency is the fine.

Now, so what is the advantage of this after all the advantage of the two stage Op Amp is that, the single size Op Amp as the DC gain, which is G m 1 by a G o 1 were as the two stage Op Amp as a DC gain which is G m 1 by G o 1 times G m 2 by G o 2. So, the DC gain of the this can be significantly larger than the DC gain of that one, both are the same unity gain frequency, and this as a single pole whereas, this has multiple poles and 0's. So, while stabilities and conditional where a single stage Op Amp, we have to worry about this stability of the two stage Op Amp.

Because, multiple poles and 0's and as I will mention earlier stability for us not only me not oscillating, it not just that it is also as to be well-behaved, it should not are ringing and, so on the step response. We see the conditions for that as soon, but the advantages is very clear, we get the DC gain of the single stays here whereas, the we get DC gain of two stages and we have designed it. So, that the unity gain frequencies or the same, so we have to compare the other things.

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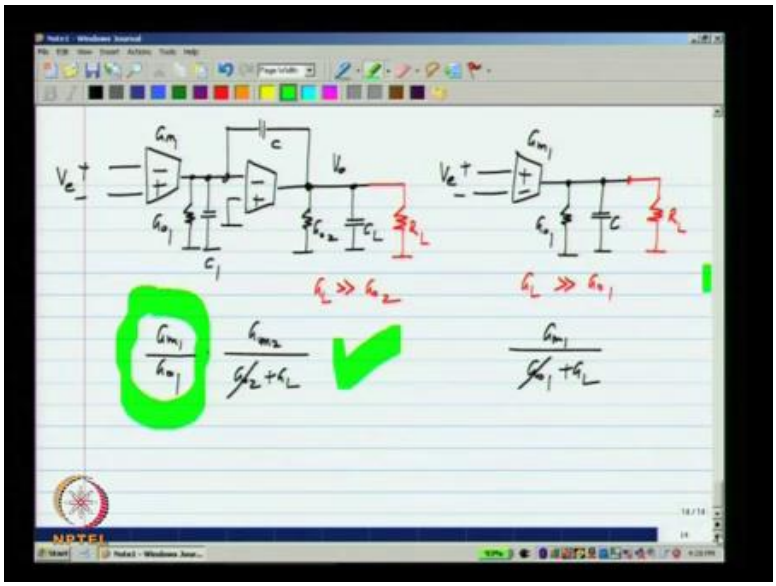

Now, besides these there is also another advantage of using gate two stage Op Amp compared to a single stage Op Amp. Let me copy these things over, and that as to do with what happens in the load is resistive that is let us we have external load, which we also connect to this and connect to that point. And in general when you do that expected that the load conductance G L is much more than G o 1 that is R L S much more are than R o 1.

Similarly here G L can be much more than G o 2, so the DC gain in this case will be a G m 1 while G o 1 times G m 2 by G o 2 plus G L. Similarly here, were DC gain will be G m 1 by G o 1 plus G L and G L will dominate G o 1 G L will dominate to G o 2 there. Now, clearly you can see the problem here in case of a single stage Op Amp, if you do as a resistive load you have to make this G m 1 much, much more than the load conductance. So, that you will get a significantly large DC gain, the DC gain required maybe a order of the 1000's in even higher.

And while try to implement a large value of G m, you end up desecrating lot of power and that is a serious problem for circuit design. Here what can be done is G m 2 does not how do we much, much more than G L it as to be more than G L, but not by a factor of 100 or 1000. But, it could be more by a only a factor of 10 let us say that is because, you can still keep G m 1 by G o 1 very large and get a DC gain that as laws respectable value.

In other words, you place the burden of getting a large DC gain on the first stage, the first stages isolated from the load. So, it will not be affected by how low this value R L S, and the second stage as to provide only a modest gain, so when you have resistive loads this is really only the reasonable alternatives. Because, if you try to use this it is possible, but you will have to end up using such a large G m that it will be very wasteful of power. Now, what about stability with the two stage Op Amp I said that, you have multiple poles are 0's, so you have to worry about stability.

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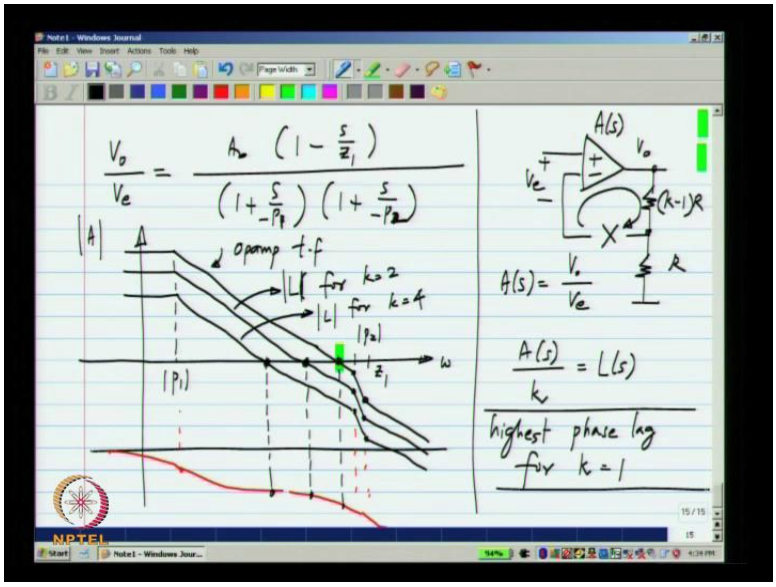

So, we have the transit function of Op Amp is to be A naught which is the DC gain, I will write in this form 1 minus s by z 1. Let me do it like this, so that minus P 1 and minus P 2 are positive enormous, now what about stability, stability margins and, so on, are determined by to gain and the loop in itself well depends on the feedback loop that you are placed of Op Amp. So, let us say realize an amplifiers of gain K the loop gain of this, let us say the transfer function of the Op Amp itself is some A of s A of s is V o by V e.

The loop gain is what I get by breaking the loop, and going around it and seeing what comes back there. So, that will be nothing, but A of s divided by K, this we have seen earlier, so this is the loop gain, now, so the loop gain depends on value of K which means there the depends unamplified that we are trying to implement. Now, let us say we take the Op Amp, and the gain of the Op Amp A of s of the Op Amp as this magnitude.

So, this is modules A and the modules V naught by V e and it as a pole and P 1 it as a pole as P 2 and 0 at and G 1, this is the gain of the transfer function of the Op Amp.

Now, what will be the loop gain depending on the value of K this curve shifted down by 20 log K on the bode plot. So, if K equals 1 this itself if the loop gain, if K equals to it will be like that, and similarly K equals 4 it will be like that and, so on, so this will be magnitude of L for K equals to the magnitude of L for K equals 4 and, so on. And also if I plot the phase response, what happens there is a 45 degree phase shift at the first pole.

And than in the phase reaches minus 90, at the second pole there is another 45 degree shift, and that the 0 there is another 45 degree shift because, it head option 0. So, we will not worry about the details of the phase right now, but what I the point I want to make use that, we have seen that the stability merging depends on what happens at the unity loop gain frequency. For the three cases I have considered K equals 1, K equals 2 and K equals 4, these are the unity loop gain frequency.

And we can see that the phase keeps going on monotonically for a function like this, so we are interested in the phase margin that is how for the phase lag is away from a minus 180 degrees phase lag. So, clearly it gets works for lower values of K, this is the worst it as the maximum phase lag, this is better it as less phase lag, this is even better it as the least phase lag. So, we have the highest phase lag for K equals 1, now this is relevant because, normally when your design in a Op Amp without any further information, you simply have to assume some value of K.

Obviously, the value of K that you have to assume is the worst case, which is in this case 1 that is you assume that whoever is going to use your Op Amp can use it with various values of K. And you design it for the worst case, and the worst-case happens to be 1, so if case 1 the loop gain is nothing, but the Op Amp gain itself, so it is easy in way you design the whole thing without worrying about which feedback loop there is use that evaluate the gain of the Op Amp, and assume that that itself is the loop gain and adjusted first stability.

Now, this is not a general procedure when you do know what value of K you have to design it for, you design it for any that particular value, you do not design it for the worst case value is only when it is do not know that you design a for the worst case value, will assume the purpose of this lecture that will design it for K equals 1.

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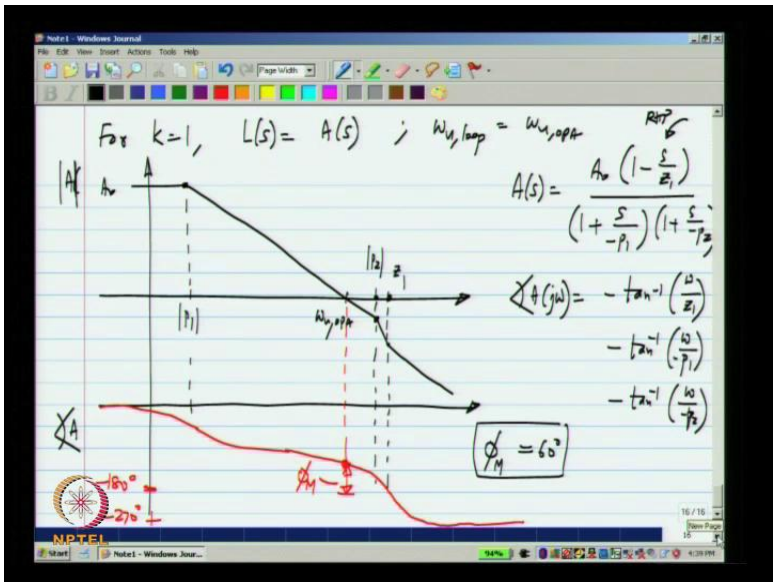

So, if we have K equals 1 the loop gain equals the gain of the Op Amp or the unity loop gain frequency equals the unity gain frequency of the Op Amp. Now, let us again examine the function that we have, magnitude and phase A of s is A naught times 1 minus s by hat 1 plus s by minus p 1 1 plus s by minus p 2. So, as I plotted earlier you start with A naught, and then you have a 20 degree per decades slope in a magnitude plot.

We have to make sure that, these other poles appears beyond the unity loop gain frequency this we have seen during discussions stability analysis, and also these 0's have to appear beyond the unity loop gain frequency. So, this is the condition that we must satisfied and you should be beyond by a certain value, and how do we determined that value for that we this is a magnitude of A we plot the angle of A which is also angle of the loop gain in this case.

So, in our case we have a right half plane 0, now the right half plane 0 introduce the phase lag. If you write the expression for the phase of this, the angle A of j omega will be minus tan inverse omega by G 1 minus tan inverse omega by P 1 minus tan inverse omega by minus P 2 here P 1 and P 2 over the poles which one negative numbers, so this is how I will return it. So, each of this contributes phase lag, and the total phase lag happens to be minus 270 degrees.

Now, what is that we want at the unity loop gain frequency which for K equals 1 is the unity gain frequency if Op Amp itself, it should make sure that this margin which is the margin between minus 180 degrees, and the actual phase at the unity loop gain frequency insufficiently high that is called the phase margin. And again we absence of any information, will assume that the phase margins and as to the let us say 60 degree sources. So, this again is not a secret number you could have phase margin anyway from 30 degrees to 80 degrees or whatever you based on the contact. But, generally we assume that 60 degrees is a good number and use that.

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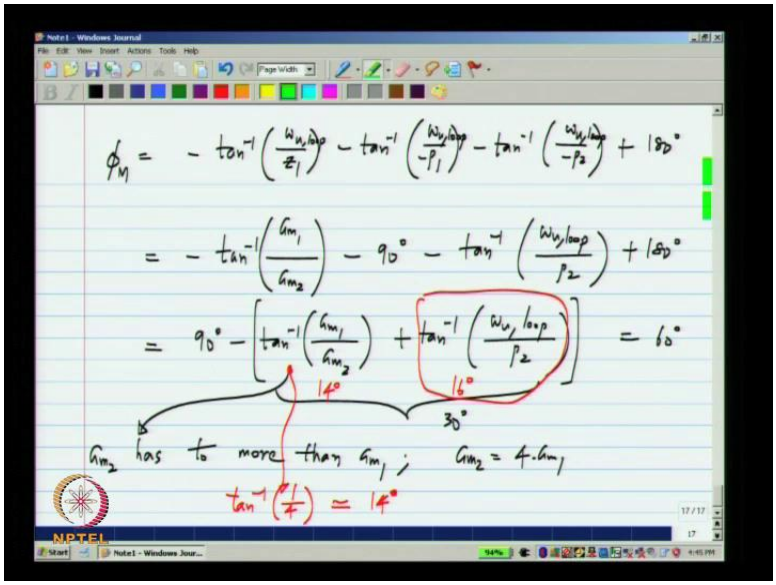

Now, what does this mean the total phase margin is the total phase lag which is minus tan inverse omega by G 1 minus tan inverse omega by P 1 minus tan inverse omega by minus P 2 plus 180 degrees is the distance from 180 degrees. So, first of all what omega we talking about here this is the omega u loop unity loop gain frequency that is where the phase margin is measured. And the unity loop gain frequency is minus tan inverse G m 1 by C and the 0 G 1 is at G m 2 by C.

So, this is to the first and it simply reduces to G m 1 by G m 2, the second one the ratio of omega u loop divided by P 1 and the tan inverse of that, omega u loop is here and P one is there. And they are very widely separated, what is the factor of separation between these two it is very easy to see this is 20 d v per decade drop. So, this is nothing, but the

separation between these two is the same as this number A naught, the ratio of these two numbers omega u OPA by P 1 is A naught.

We will something we know already omega u OPA the approximately calculated is A naught P 1 when the role of is predominantly a first order now because, of that this is an inverse of a large number. So, this is simply minus 90 degrees that can also be seen from a plot, the phase drops down minus 90 and stays that way for stays that way this is a phase like due to P 1. Now because, P 1 is far from omega u OPA as you could have reach 90 degree somewhere, here and then stays on 90 degree all the whether the contribution due to P 1.

And finally, we have minus tan inverse omega u loop by P 2, this is something that has to be calculated I just leave it as it is omega u loop by P 2 plus 180 degrees. And this is nothing, but 90 degrees minus tan inverse G m 1 by G m 2 minus tan inverse omega u loop by P 2. Let me write it as minus in some of these 2, this is a phase back due to right half plane 0, this is the phase like due to the second pole, and we would like this to be let us say 60 degrees.

So, what is this mean the sum of this 2 should be a 30 degrees, it is up to us apportion the 30 degrees between these 2, we can have a large phase like due to the 0 are the pole for, but the some of them as to be 30 degrees. Now, if you make one of them very large, and other one as to be very small and that usually very difficult, and also you see that the phase like due to 0 depends only in the ratio G m 1 by G m 2. Clearly to make this small you have to make G m 2 much more than G m 1 this is very clear right that guideline appears directly from this G m 2 as to be more than G m 1 where a significant factor.

Because, if G m 2 were equal to G m 1 this would be 45 degrees, and there is no way to make this 30 degrees. In fact, we have to keep this number well below 30 degrees right, so let us say for instance we will take G m 2 equals 4 times G m 1 than this particular number will be tan inverse 1 by 4 which is approximately 14 degrees. So, these sounds like a reasonable choice, than we have 14 degrees from this and we have 16 degrees from their will have 16 degrees for this one and we have to adjust the value of P 2.

So, that this number happens to be 16 degrees, this innocence is the design of the Op Amp on for this level. We have not yet got to the transistor level that is the reason we discuss the Op Amp, at the level of the control sources before going on to transistor

level. So, that these issues with transfer function and loop gain and, so on, come out very clearly without being distracted by the transistor level details.

So, what we do when we have want to design a two stays Op Amp we have to choose this second stage trans conductance. So, G m much more than the first say G m, let us say we make it 4 times, again not a secret number you could choose 3, you could choose 6 whatever is convenient. If you do choose 4, the 0 will give you 14 degree phase like and you will are 16 degree phase lag left for the second pole. And you can adjust the second pole, so that you can get be only 16 degrees phase lag Op Amp.

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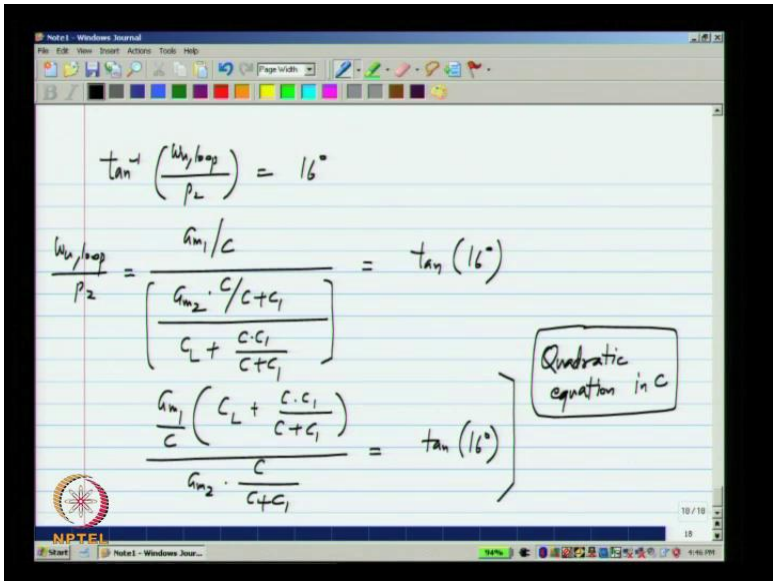

Now, what does this give you first of all omega u loop itself is G m 1 by C and P 2 is G m 2 C by C plus C 1 divided by C L plus C C 1 by C plus C 1. And this is the ratio omega u loop by P 2, and that is tan 16 degrees, I have here neglected the contribution due to G o 2. Because, that is expected to be much smaller than, the contribution due to G m 2 right, now I will expand that this out I will get equals tan 16 degrees. Now, what comes out of this is a quadratic equation in C given C l and C 1 and values of G m 1 and G m 2 you can solve for this.

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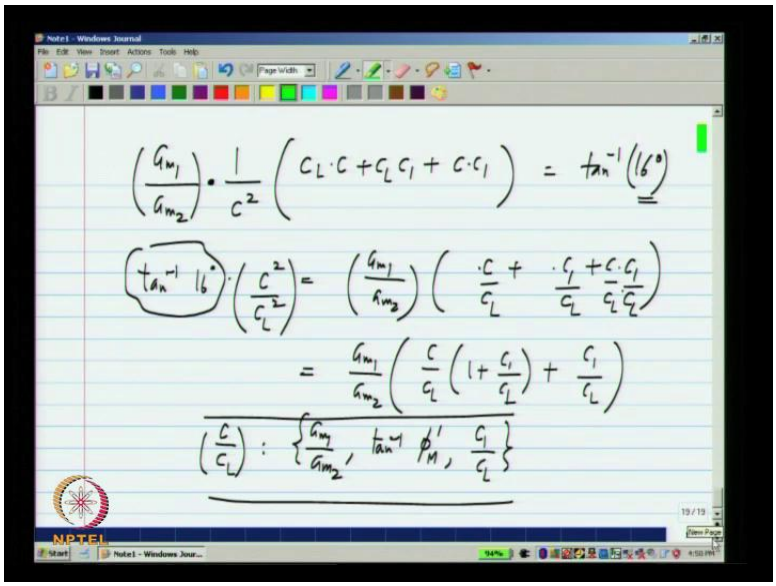

So, let us try to pull it on a more eliminating form will have G m 1 by G m 2 times 1 over C square appear there, and this 16 degrees came. Because, which was a G m 2 by G m 1 of 4 otherwise will get some other number, now I will divide both sides by C L's square it makes sense to express everything as the fraction of the low. So, here I will get C by C L here I will get C 1 by C L and here I get C by C L times C 1 by C L.

So, that is what the whole thing is, so this is the quadratic equation is C by C l square and it intuitively makes sense to normalize everything to C l. Because, if you have a large C L then; that means, that the unity gain frequency of the second Op Amp that we used to make current control voltage source, tends to be small. And we already said that, the unity gain frequency of overall Op Amp as to be smaller than that unity loop gain frequency of the second loop, otherwise the second loop is not behave like an ideal feedback loop.

So; that means, that we will am to have a large C or small omega u, so if you have a large load capacitance, all the other capacitance also tends to be larger. So, you can calculate C by C L from this expression based on the ratio G m 1 by G m 2, the phase margin that we have I will put phi M prime. Because, this is the phase lag excluding the phase lag due to the 0, and it is also depends on this ratio C 1 by C L. So, the bottom line is it can be calculated based on these things, and then we can verify with simulation whether it is exactly right or wrong. Let us go back here, we have the expression for the

wholes and 0, now when certain conditions the expression for this pole can be further simplified this P 2.

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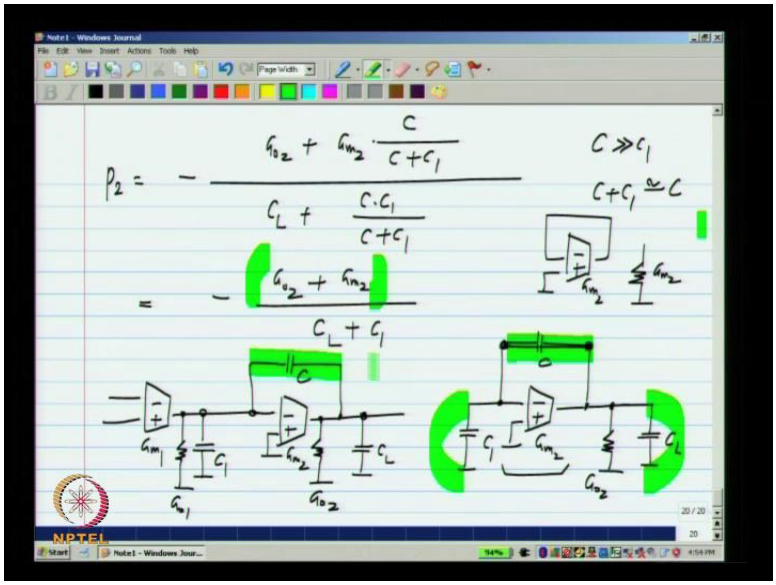

What is the expression for P 2, it is minus G 0 2 plus G m 2 C by C plus C 1 divided by C L plus C C 1 by C plus C L. Now, let us imagine a case where C is much more than C 1, let us say the design value is done out to the like that, so what is it mean I will approximate C plus C 1 by C itself. So, P 2 becomes minus G o 2 plus G m 2 divided by C L plus why C L sorry minus G o 2 G m 2 divided by C L.

Now, does this make intuitive sense, again let us go back to the structure that we have, now what we are assuming is that this C the capacitor C here is much more than the capacitor C 1 over there. So, what does this mean earlier we assume that in this feedback, we had a division ratio C by C plus C 1, now if C is much more and more than C 1 there is no division at all, any voltage there appears here also appears there.

So, C is approximately like a short circuit right, in that case we will have this topology when this is a short circuit I just shock this. Now, if this G m 2 is shouted down itself the conductance is nothing, but G m 2 itself, so if you have G m 2 like that it is looks like a conductance whose value is G m 2 under the resistance of 1 over G m 2. So, the total conductance is G m 2 plus G o 2 that is what we see here, and there is a mistake in the denominator here it should be C L plus C 1.

Clearly you see that if C is very large, what happens is you will simply end up with C 1 here. And we have these two capacitors C 1 and C L in parallel. So, we have G 0 2 and G m 2 in parallel with in C L and C l the second pole expression becomes even simpler than before, it is simply G m 2 plus G o 2 divided by C 1 plus C L.

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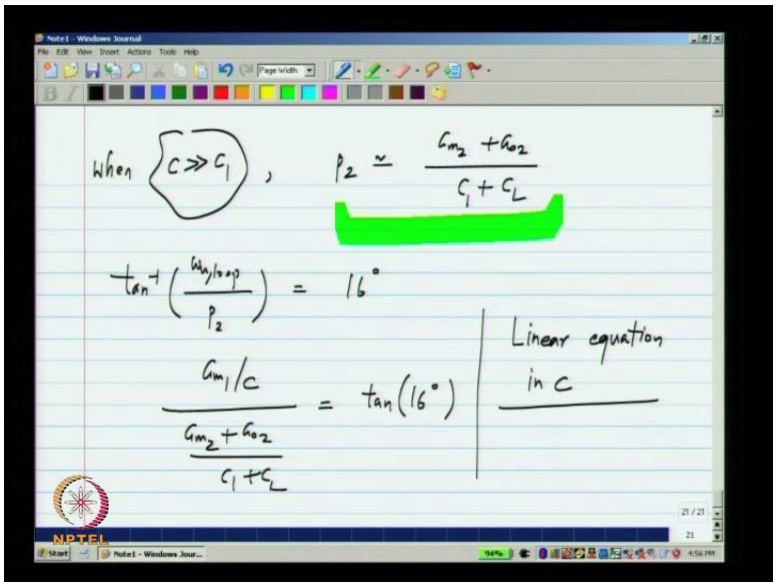

Now, this is true only when C is much more than C 1, which may or may not be true always, but what you can do is use this expression for P 2 as the first cut approximation. Now, that is useful because, we are earlier said tan inverse omega u loop divided by P 2 should be 16 degrees or some particular value that we used to have. Now, omega u loop is G m 1 by C and P 2 is G m 2 plus G o 2 divided by C 1 plus C L, so now, you see that we have linear equation in C is much easier to solve.

So, what you can do is you can use this further approximation for the value of P 2 and get a first cut value of C based on the linear equations solution, which is very easy to compute. Sometimes when you are calculating things in your head, this may be the method to follow and finally, you can see really whether C is much more than C 1 is or not, C turns out to be much more than C 1 you do not have to do anything further, if C is not much more than C 1 what you will have to do is to go back and recalculate based on the quadratic equation.

Thank you I will see you in the next class.