Analog Integrated Circuit Design
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Lecture - 28
Common Source Amplifier Frequency Response; Differential Amplifier

Hello and welcome to lecture 28 of Analog Integrated Circuit Design. We were looking at performance of basic amplifiers in presents of parasitic, basically the high frequency performance of the basic amplifier stages. We looked at what happens in a common drain amplifier and a common gate amplifier, now we will look at the Common Source Amplifier in this lecture.

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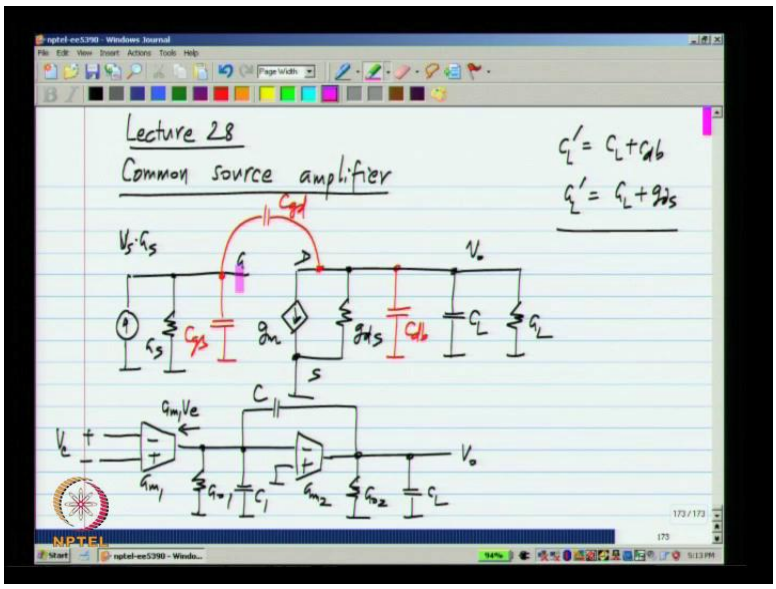

Now, this is the small signal model of the common source amplifier, including the transistor parasitic that we drew yesterday, now the C d b parasitic appears the cross C L. And C g d and C g s are here, we also saw that it has a close correspondence to the miller opamp that we analyzed earlier. If I glitter when we do the implementation, we will see that the miller opamp is formed around a common source amplifier as well. We have the same network of three capacitor C 1, C n, C L which are analogous to C g s, C g d and C L prime.

We have some conductance here G o 2 which is analogous to G L prime G o 1, which is analogous to G s and this trans conductor G m 2 is analogous to this G m. And it is in the

same polarity, because if I increase the this node current will be drawn into G m 2, so if I increase the gate node, the current will be drawn into this G m. Now, the only other difference is what happens with the input, before we had V e which provided the current of G m 1 V e in this direction, through the trans conductance G m. Now, we have an input of V s, but the transformed input source is a current source V s G s were pushes into the node, so this V s G s is analogous to minus G m 1 V e.

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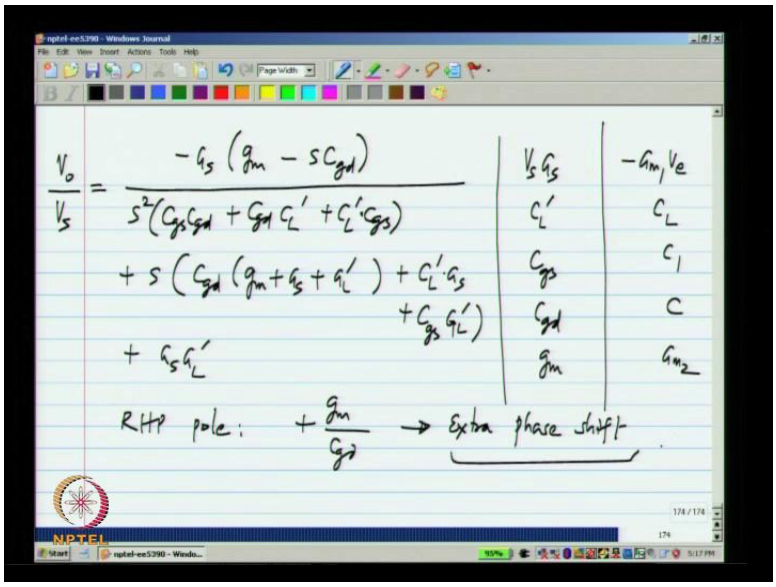

So, let me write out the corresponding terms, V s G s in the new circuit is like minus G m 1 V in the old circuit and V C L prime is like C L and C g s is C 1, C g d is C and G m is G m 2. Now, because we have already done the analysis I am not going to repeat it and we saw that V naught by V e was something that had a single 0 and two poles, so this is the expression. We had and all we have to do is to substitute the corresponding terms, I will not worry about the others that we can do very easily, the only one thing is first I will write out the expression for V naught which will be G m 1 times V e, and G m 1 times V e has to be substituted by minus V s G s.

Now, I want the transfer function, now I will divide both sides by V s, so I will have minus G s over there, now by the way just as a practice for circuit analysis I suggest that, you put down the circuit and then do the analysis and make sure that you get exactly the same answers as before. This is more of a drill exercise, because we have already done

the analysis, but nonetheless do the nodal analysis again, and make sure that you get this expression.

So, G m 2 is g m and this S C g d and this expression will be C g s C g d plus C g d C L prime plus C L prime C g s, so by the way I put C g d here, this was originally C, it is C g d and this will be g m plus G s plus G L prime C L prime G s and this is C g s G L prime and finally, we will have G s G l prime. So, that is the expression for V naught by V s in a common source amplifier including the parasitic capacitor.

So, now first of all its very obvious that, if you look at only the D C terms, we will have minus G s times G m divided by G s times G L prime or minus G m by G L prime, this is a very familiar minus g m R L formula for the gain of a common source amplifier that is true. And a rest of it the poles and zero will be analyzed and exactly the same way as we did the miller amplifier. We see that there is a right half plain pole at plus g m by C g d and this has the usual effects of extra phase shift and so on, and there will be two poles which are as before.

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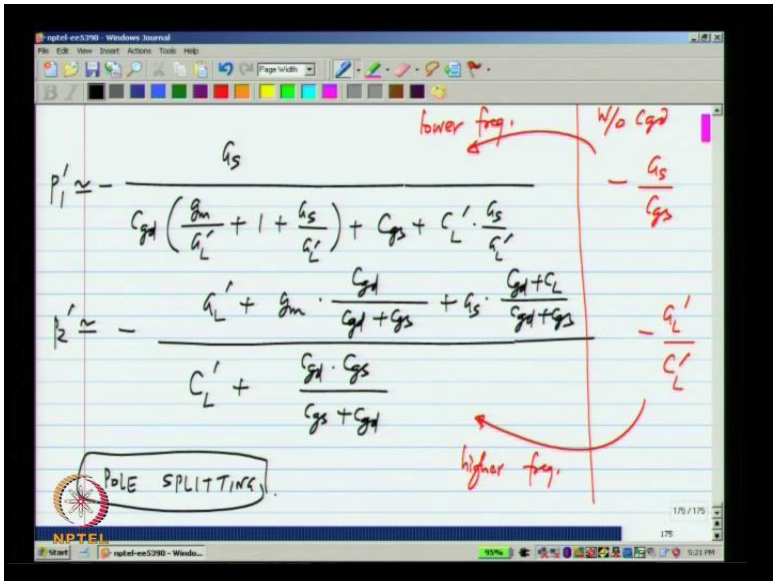

So, the pole associated with the input node of the common source amplifier will be related to G s, this will be the pole, by the way first of all this is an approximation, it is obtain by approximating, the quadratic equation into two linear equations assuming that the poles are far from each other. If not this approximation is not valid and a further approximation tells you that it is roughly like having the conductance G s ((Refer Time:

07:27)) at the input in parallel with C g s and miller multiplied C g d. If you imagine a most transistor without G g d the pole would be simply at minus G s by C g s and the other pole would be at minus G L prime by C L prime.

Now, because we have C g d, we will have this modification just for easy comparison, let me put down what happens without C g d this would have been minus G s by C g s that is all. And similarly, the pole associated with the output conductance would be some conductance, which is the sum of the G L prime that exists plus the conductance due to this G m being in feedback, which is g m times this capacitor divider ratio. There will be some other minor term associated with G s, which I am going to ignore, you would get something like G s times C g d plus C L by C g d plus C g s, this usually can be safely ignored as long as G s s sufficiently small.

In the denominator we will have C L prime plus series combination of c g d and c g s, so exactly the same as before and with the same intuitive explanation, and to understand this C 1 better, we will put down the value without the C g d and the would be simply minus g l prime by c l prime. So, with the conductance g s, we had a capacitance C g s now we have C g s plus multiply c g d, so this moves to lower frequencies. And here with the conductance G L prime we have a capacitance C L prime, now with the conductance G L prime plus g m time sum fraction, we have a capacitance C L prime plus some small capacitor C g d and C g s to C g s.

So, this typically goes to higher frequencies, so the larger the value of C g d the greater this effect and we saw that this effect was called pole splitting, if we did not have C g d the input and the output of the common source amplifier are isolated from each other. We have a pole at the input, we have a pole at the output the input pole is not influenced by what is happening to the load, the output node pole is not influence by what is happening with the source resistance and so on, But, now we have coupling, so C g d introduces coupling between the input and output nodes, clearly pole associated with the input node is influenced by the gain.

We have g m by G L prime here ((Refer Time: 10:48)) and the pole associated with the output node is also influence by C g d, because C g d introduces feedback around g m and that significantly influences the pole. So, the input and output are no longer well isolated when you have C g d, and this is what I remarked when I was discussing the

common gate amplifier, that common gate amplifier is 1 in which the input and output are very well isolated.

And that is sometimes the reason for using a common gate amplifier, it has a current gain of only 1, but it is a way of providing a current while providing isolation between the input and output, we will see more of that later. So, this is the summary of the common source amplifier, there will be pole splitting due to C g d, now we can analyzed more complicated situation where the load is not merely capacitive, what inductive and so on. it turns out that in such cases, the coupling introduced by C g d can also introduced instability, we will not worry about that for now.

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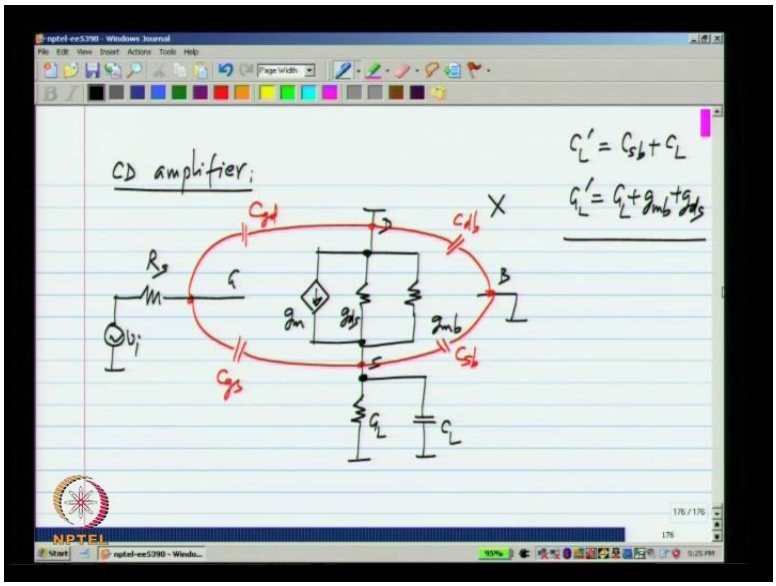

Now, let us revisits the common drain amplifier, we analyzed the common drain amplifier for D C as well as including parasitic, but when we included the parasitic we did not include the source resistance. I assume that the common drain amplifier was driven like this, this is the bulk drain source gate, this is g m, g m b, g d s, C g d, C g s, C d b, C s b as usual we will observe the capacitances and reduce the number.

So, we have C L prime to be C s b plus C L and C d b prime has no effect, because it is to fixed voltages. When reality we will also have resistance R S and finally, this conductance g m b is between this point and ground, and the controlling voltage is also between this point and ground. So, this can be simple replaced by a conductance g m b

which finally, means that we can have an effective load conductance, which is G L plus g m b plus g d s.

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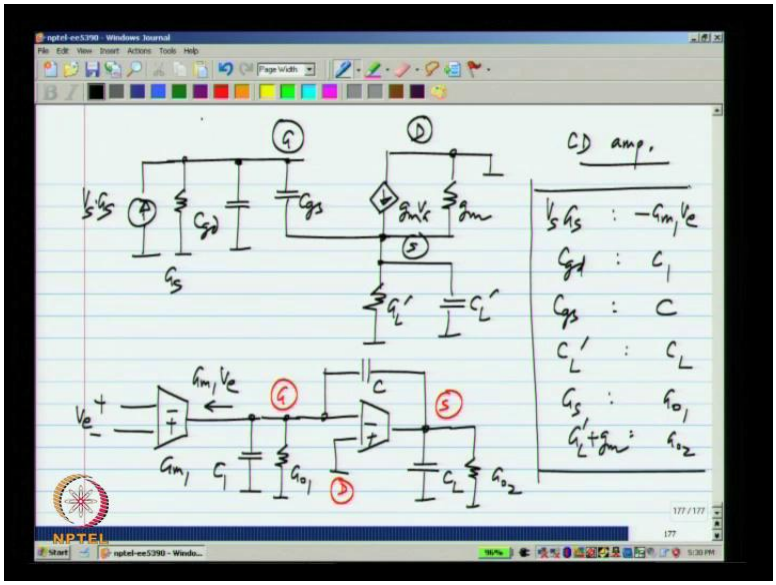

Now, let me reduce this picture I will have something like this, when I said reduce the picture I mean reduce the shutter and the number of components that we have, C g s g m and C g d will be here, and this point is grounded and I will have G L prime and C L prime with the appropriate value. So, this is the small signal picture of a common drain amplifier, now this can be analyzed, but my point was again how useful the analysis we did earlier with the miller opamp force. So, let me redraw that I have G m 1 with V e applied this way, so this draws a current G m 1 V e C 1 and the conductance G o 1 is over here.

Here is the C, C L and G o 2, now if you look at this particular picture it also has a loop of three capacitances C g d, C g s and G L prime and this is gate drain and source. Now, if I had to make a correspondence between the nodes and the upper and the lower circuits I would say, this is the gate and this is the source and the ground is the drain. And also let me transform the source, as I read for the common source amplifier, I will have a source V s G s. So, again you see that the analysis we did for the miller opamp can be used as it is for the common drain amplifier.

Now, what are the other differences first of all this g m goes from drain to source and also it is not dependent on the voltage between this G and ground, but between G and

source. So, I can replace that with two trans conductance, so this is g m V g s right, so let me make it g m V g in this direction and g m V s and that direction, and you also notice that for this control source, the controlling voltage is across the control source itself. So, it can be replaced with a conductance g m, then the correspondence becomes exact, this control source is controlled by the voltage between this point and ground just like this ((Refer Time: 17:45)) one.

Only when the voltage increases it pushes current into this node whereas, here when this voltage increases it pulls current from that node. So, the corresponding quantities are first of all V s G s in the common drain amplifier is like minus G m 1 V e, C g d is like C 1, C g s is like C, C L prime is like C L I had omitted the source resistance here, this is G s source conductance, G s is like G o 1 and G L prime plus g m is like G o 2. So, again by using the analysis we did earlier for the miller amplifier and substituting with the appropriate terms, we can get the detail answers for the common drain amplifier including its source resistance.

I am not going to do it here, please do that and make sure that first of all you have consistent results with what we analyze before that is only the D C analysis and when R S is 0. And then you can also see that you will have two poles and zero, you can compute the poles and zero sub approximately and see how the whole thing behaves. It is also important to intuitively explain to yourself, quite again behaves the way it does, like for instance what happens in the low frequency limit, what happens in the high frequency limit and so on.

So, we have reviewed the basic amply stages, the common source, common gate and common drain amplifiers, we know how they behave, now which of them gives you at least one pole probably two poles and sometimes zero as well. And this will come into play when we realize more complicated amplifiers, turns out that when we go to more and more complicated amplifier, we cannot go on with this business of writing node equation and analyzing them it is possible. But, the expression would be, so complicated that you would not get any inside into them.

So, you have to be able to recognize individual stages, see how they behave under different conditions make suitable approximations and get the answer for the entire circuits. Otherwise, we will not be able to design any circuit more complicated than a

signal transistor circuit we will soon go into multi stage amplifier and so on. And there is no way we can write out third, fourth, fifth order transform function, first of all it is hard to evaluate and more importantly even if you did so it will be useless because it would not give you any intuition.

So, you draw intuition from the analysis of basic circuits and applying it appropriately to the more complicated circuits, and when you want exact answer you go to simulator calculate it and reconcile it with the intuitive results that you have got. Now, the next topic of a importance after finishing the basic amplify stages, is air tunnel basic stage which many of you would be familiar with, it is the differential pair.

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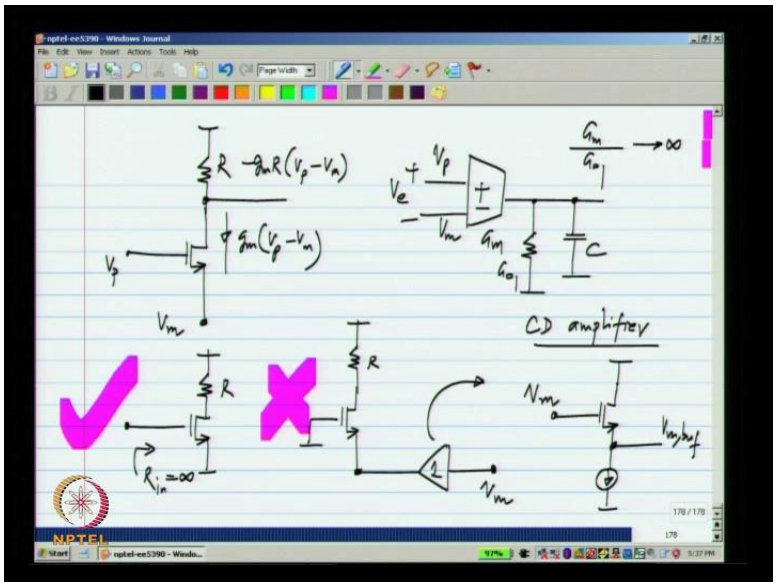

Now, why is this relevant at all let us go back to the most basic opamp we have, what does it have it has a trans connector G m and a capacitor C and the input is difference input V e, that is there are two inputs with respective ground. And the circuit responds to the difference between the two voltages, if I called this V p and V m it can responds to V p minus V m. So, we need to have a circuit topology that will amplify the difference between these two stages, what is it that we can use first of all we need to have a high DC gain.

In fact, infinity we know that the D C gain of this is G m by G o 1 and it should approach infinity ideally, so how would we design amplifier that has a very large gain, so let us start with the basic amplifier that we know that is the common source common drain and

common gate amplifiers. First of all common drain amplifier is ruled out, because it has a voltage gain of 1 and common gate amplifier it is also ruled out, because see here the inputs V p and V m should look at high impedance inputs that is no current should be drawn from here, in order not to interfere with those voltages.

At least that is the assumptions with which we design the negative feedback circuits prototype, so we will still assume that, that is what we want so the only thing that gives you a high gain and high input resistance at one pole is a common source amplifier. Now, what does the common source amplifier amplify it amplifies the difference between V p and V m and let me ignore g d s for now, so the current here will be g m times V p minus V m, if you pass through a resistance you can obtain an output voltage which is g m R times V p minus V m negative of that.

Now, one of the things that we immediately see is that, the what a seen by V p and what a seen by V m are very different, if I draw the circuit with only V p I get this, and the resistance looking in there is infinity. But, draw a circuit with only V m, I really have a common gate amplifier here and the resistance looking up there is 1 over g m which is very low, I already said that we would like to sense the difference between the input and feedback without disturbing them, that is what it desirable in a negative feedback system. So, this is this is not and we have to fix it, now what should we do to fix that, first of all what would you do, if you have a low impedance to drive.

But, you would like to see a high impedance the obvious answer is the voltage buffer, that is the purpose of the voltage buffer, if you have a heavy load, but you do not want to present a heavy load to the input source you insert a voltage buffer in between. So, I should not do this, but what I should really do is insert a voltage buffer and have V m over there.

Now, what is a voltage buffer topology that I am familiar with from basic transistor amplifier the only thing that I know is a common drain amplifier, or the source follower and it looks something like that. So, this is the common drain amplifier, if I have V m here I will get a buffered version of V m above there, so I can try to use this in that circuit and try to make my amplifier, which amplifies the difference between V p and V m.

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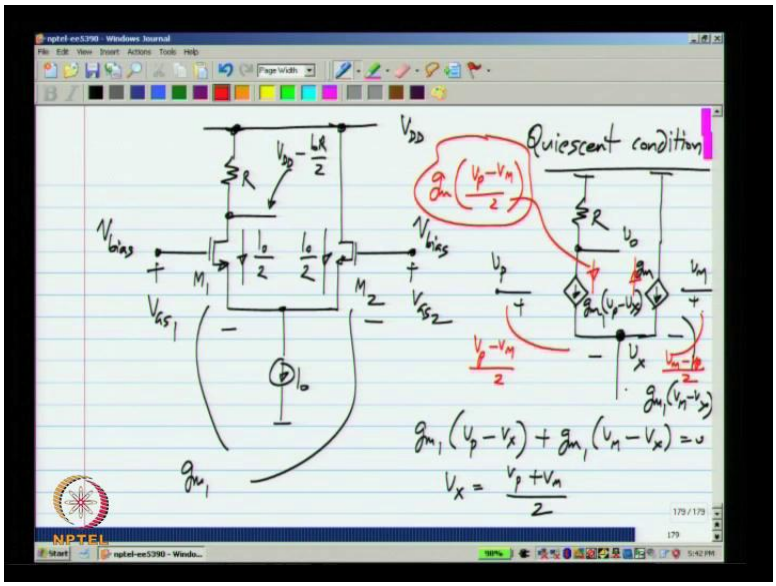

Let me put it down here this is my amplifier and I have V p, and I would have wanted V m here, but because it looks at a very low input resistance I would do not want, but a buffer version of V m. And how do I get a buffered version of V m using a source follower, and I will just ternate by draw the mirror image of it, so that it is convenient to draw. So, this is the source follower bias with some current source and the drain is connected to V D D, so this is what I will have. Now, I expect that here I get something proportional to V p minus V m, let us see if I really get that.

So, let me put the current source in the middle and V p and V m are really small signal voltages I will assume that, they have some bias voltage plus V p and bias voltage plus V m. And let me call this M 1 and M 2 and in all my initial analysis, I will assume that there is no G d s that is the transistor is simply represented by g m, I will also ignore body effect for, now I will later see what it does to this circuit. Now, what happens first of all what is the quiescent condition or the operating point, at the quiescent condition V p and V m are both 0.

So, I have V bias and V bias over there and clearly the V g s of m one and V g s of m two are equal to each other in this condition. So, if they are equal to each other this two currents have to be equal to each other remember we assume no G d s, which means that v d s has no influence on the drain currents. So, this two will be equal and since, the sum of them has to be I naught, each of them equals I naught by 2 and if I connect this to

some supply voltage V D D, this will be voltage V D D minus I naught R by 2. And let us also assume that all transistor are operating in saturation region, that is some basic assumptions that we make everywhere.

Because, the trans connection of the transistor is highest in the saturation region, and also the conductance G d s is the lowest in the saturation region, that is the prefer region of operation for amplifiers, so the quiescent operating point is set. Now, at that operating point this two resistors will have some trans conductance, because the operating point are identical the trans conductance is also will be identical and I call that G m 1. So, when I draw this small signal picture, this is what I will have the input here is V p the small signal input, the input here is V m and I have R over there and nothing over here, this is where my output is.

This is g m times let me call this V x this is g m time V p minus V x, this is G m 1 times V m minus V x, so what this node I have G m 1 time V p minus V x plus G m 1 times V m minus V x equal to 0. So, V x obviously, equals V p plus V m divided by 2, so this means that across this two terminals, I have V p minus V m by 2 across this 2, I have V m minus V p by 2, so the incremental current here which is the same as the incremental current than the opposite direction other transistor will be equal to g m times V p minus V m by 2.

So, as expected we have got a small signal current that is proportional to V p minus V m, and that flow into the load resistance R and we will have an output voltage that is g m R by 2 times V p minus V m. Now, in our original common source amplifier, the case where we applied V p to the gate and V m to the source, we would have expected that an incremental current of g m times V p minus V m. But, the important thing here is that, we are driving the source with an imperfect buffer, the buffer output resistance is not 0, it is equal to 1 by g m of that transistor M 2 is being used as a buffer, according to our view point.

And it is output resistances 1 over g m of that transistor, so first of all the common source amplifier it is source is not exactly at ground, it is connected to ground through a small resistance 1 by g m that is why the gain from V p to the output changes. And also as far as the buffer is concerned it is not terminated by a very impedance, it is terminated by 1 over g m as we will see. So, V m does not appear at the source of M 2 with the gain

of 1, in fact, it appear with the gain of half as if we have seen here, it is V p minus V m by 2. So, because of this reason the gain of this amplifier is g m R by 2 times V p minus V m, but that is perfectly fine what we wanted was something proportional to V p minus V m and that is what we have here.

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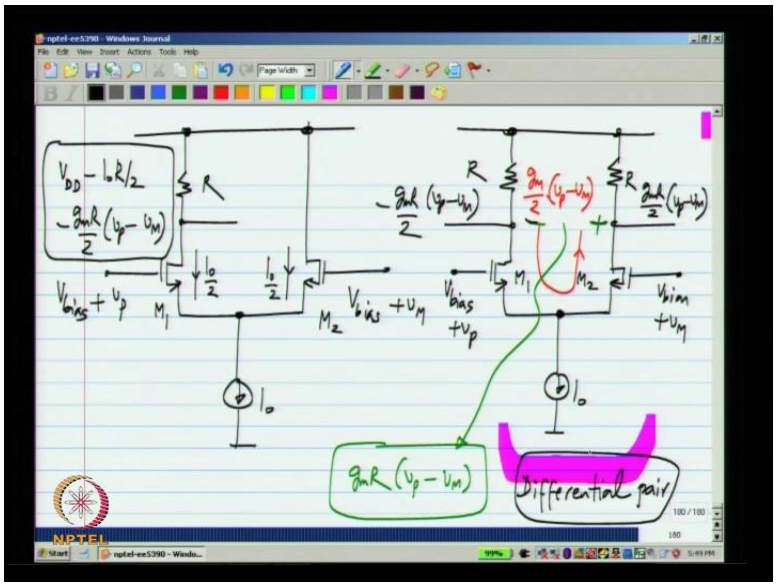

I have a current I naught R and I apply V bias plus V p V bias plus V m in quiescent condition I have I naught by 2 I naught by 2, this is M 1 that is M 2, and the small signal output voltage will be minus g m R by 2 V p minus V m. And the quiescent output voltage will be V D D minus I naught R by 2, so that is the total voltage at the output and we have a small signal output voltage that is an amplified version of V p minus V m. Now, this is equal into having a trans conductance with some output resistance this is g m 1 G o 1 and it should be connected to a capacitor, ideally we would like to have no G o 1, but we had to have some resistance here to bias the circuit, as well as convert the output current to a voltage.

So, we will learned of having D C gain of G m 1 by G o 1 here, which basically is g m R by 2 in our case. Now, if you observe this circuit, it is obviously, symmetrical with respect to M 1 and M 2, meaning the entire circuit is not symmetrical we have a resistance R connected to the drain of M 1 and not M 2, but the quiescent condition is symmetrical. And we could as well have a connected R to M 2, now what will happen the currents will be exactly the same as before, let us say this is V bias plus V p and that

is V bias plus V m. And this output would be remember this current here, the incremental current was g m by 2 times V p minus V m.

So, the output voltage here incrementally would be g m R by 2 V p minus V m it is symmetrical after all it is simply like interchanging V p and V m in the circuit. So, I could do that as well, in that case I get again a plus g m R by 2 instead of minus g m R by 2 and obviously, in the circuit I can also do this, I can connect another resistor here and at this point I will get minus g m R by 2 V p minus V m. And if I take the difference between this two notes, I will have g m R V p minus V m, so our efforts to open some output related to the difference between V p and V m has given us this particular circuit.

The way we started of with was a common source amplifier, because that was the only thing that we knew which could give an appreciable gain, and we knew that it amplifies the difference between gate and source. So, we connected one of the voltages to the gate other one to the source, but the impedance looking into the source was very low, so instead of connecting it directly, we connected through a source follower. And when we put down the whole circuit we came up with this circuit, which has two transistors M 1 and M 2 and the current in the two transistors is related to the difference V p minus V m.

Now, this current can be integrated in a capacitor and in this case for biasing reason, we need a resistor as well, but this is the circuit that can be used for our opamp, at least as a first cut circuit for our opamp. And this circuit as you most likely are already familiar with is the differential pair, it is the differential pair and this is an interesting circuit by itself and we will analyze it in some detail.

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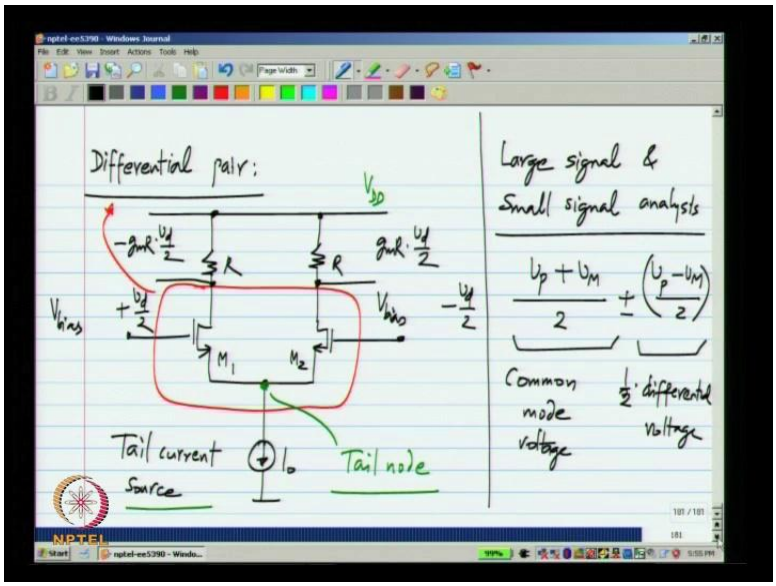

Before we go on to design opamp with it, we will considered the completely symmetrical circuit that, we put down last where we have resistance R in the drain of a both transistor M 1 and M 2. And it is biased with the current source, and this current source is usually call the tail current source, this is the differential pair, this is the symmetrically loaded differential pair that we have here. And this node of the differential is known as the tail node and it has being driven by voltages V bias plus V p and V bias plus V m some voltage on the two sides.

Now, how would we analyze this circuit, we need to do both large signal and small signal analysis we have already done this small signal analysis, but we need to put down some more details. Now, first of all as usual we will assume that the g d s of this transistor is 0, and it has an ideal current source biasing the tail node. Now, the first thing I will do is write this V p and V m as the average value plus minus of the difference value, and this average value is known as the common mode voltage. And this is known as the differential voltage V p minus V m is the differential voltage and this is half of the differential voltage.

Now, the reason I do that is let me again rewrite this is V bias plus V average plus half the difference voltage, and here I will write it as V bias plus V average minus half the difference voltage. Now, it is very obvious that V average has no influence on this circuit, because let us say their difference voltage was 0 and you have some V average.

So, you have V bias plus V average on the left side and V bias plus V average on the right side as well. Now, what is the affect of V average it is nothing, because the V g s of M 1 and M 2 are still identical to each other, and the sum of currents in M 1 and M 2 equals I naught.

So, whatever the value of V average, if the current source is ideal the current in each of this transistors will be equal to I naught by 2. Now, later we will see that when the current source is not ideal, V average will have some influence, but for now I will ignore that, because it has no influence at all on this circuit. So, I will consider inputs that are applied anti symmetrically like this, V D by 2 on the left side and minus V D by 2 on the right side. And with this we can do our analysis, the small signal analysis we have already done that is we end up with a voltage of g m R by 2 times V p minus V m, which means that this is g m R times V d by 2 and minus g m R times V d by 2.

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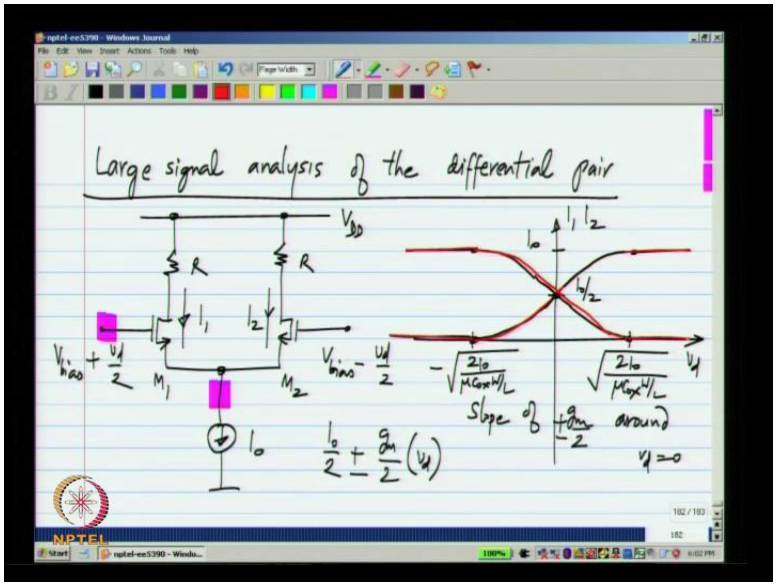

Now, we will do the large signal analysis of the differential pair what I will do is, I will try, and plot the currents I 1 and I 2 following in the two transistor M 1 and M 2. Now, what happens what do we except if a V D by 2 is positive, then V g s of M 1 is more than the V g s of M 2, and so I 1 will be more than I 2. And similarly when V D is negative V g s of M 1 is less than the V g s of M 2 and I 1 will be less than I 2, when V D equal 0 we know that, I 1 and I 2 both equal I naught by 2. And what I would like to do is to plot

the currents I 1 I 2 as a function of V D and I know that this point and V D equal 0 both are equal to I naught by 2.

Now, what happens for very small values of V D, now for very small value of V D, we are deviating to a very small extent from the operating point, so the small signal analysis will hold. Now, what are the incremental currents the current in M 1 was I naught by 2 that is the quiescent current plus g m by 2 times V p minus V m, which is V d and the current in M 2 is simply this with a minus sign. So, what will happen is for small values of V D, there will be straight lines with a slope of g m by 2 or minus g m by 2, depending on whether we are talking about I 1 or I 2, when V D is very small.

Now, what do we expect or happen when V D is very large, as V D becomes larger and larger this V g s of M 1 becomes larger and larger, about some point it will become so large that, the current corresponding to that will be equal to I naught. We know that in the quiescent condition M 1 cross a current I naught by 2, and as you increase V g s it will increase from I naught by 2, and at some point the current in the transistor M 1 will be equal to I naught.

So, obviously, at that point the current and the transistor M 2 will be equal to 0, so the transistor M 2 cuts offs and for any increase in V D beyond this point, the transistor M 2 cannot have a current that is less than 0. So, it will continue to have a current of 0 and transistor M 1 will continue to have a current of I naught. Now, what is the voltage at which this will happen, this will happen when the V g s of this is just equal to the value require to carry I naught.

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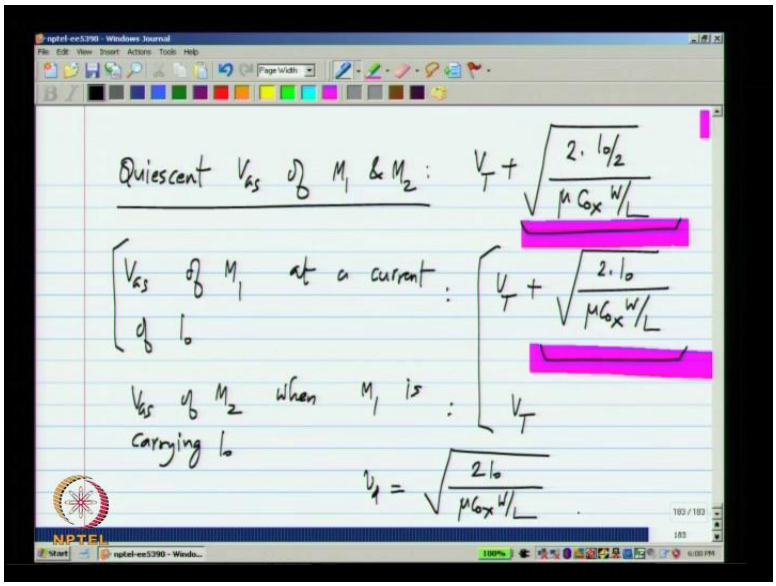

The quiescent V g s M 1 and M 2 equals V T plus square root 2 times the current which is I naught by 2 divided by mu C ox W by L. Now, V g s of M 1 at a current of I naught is V T plus square root 2 times I naught by mu V ox W by L, so this is the over drive voltage, when in the quiescent condition. And this is the over drive voltage in the condition when all of I naught is flowing through M 1, now what is the V g s of M 2 in this condition, M 1 is just carrying I naught, when I say M 1is carrying I naught. What I mean is the value of V D has been increased such that, the current in M 1 just reaches I naught, and the current in M 2 just reaches 0.

So, when the current in M 2 just reaches 0, it is gate source voltage will be equal to V T, so the difference voltage between these two will be simply equal to square root of 2 I naught by mu C ox W by L. So, the current or the voltage equal to square root 2 I naught by mu C ox W by L, the current in M 1 will reach I naught and current in M 2 will reach 0. And the circuit is symmetrical, so the voltage equal to minus square root 2 I naught by mu C ox W by L, the current in M 1 will reach 0, and the current in M 2 will reach I naught.

And in the middle they will do something non-linear like this ((Refer Time: 48:51)), they are linear close to the point where V D equal 0, and beyond that they are non-linear. Now, the main lesson to take home from this is, when the differential pair is operated with a small difference voltage, then the currents are linearly related to the difference this

is important and this is what we will use in our opamp design. In fact, we came up with the differential pair as a means of having some current, that responds to difference between two voltages; and also presents are very high impedance to both the voltage sources.

Now, when the difference voltage V D becomes very large, what happens is the circuit starts becoming non-linear just like any other circuit, and for a large in of V D the currents in the transistors will become constant. All of the tail current will flow into either M 1 or M 2 and the other transistor will carry 0, now this will become important to study some of the non ideality so the opamp. And maybe some other circuit as well, we will see all those detail later, but in the next few lecture, we will look at how to make the opamp using the differential pair.

Thank you.