Analog Integrated Circuit Design
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Lecture - 37
Two Stage Opamp; Three Stage and Triple Cascade Opamps

Hello and welcome to lecture 37 of analog integrated circuit design. We were discussing the 2 stage opamp. We have calculated the spot signal parameters, offset and noise. We also saw that offset was contributed by a mismatch between transistors in the first stage as well as the biasing condition of the second stage. If we make the current density in the second stage transistors equal to the current density in the load transistor for the first stage, the systematic offset can be avoided. Now, we will calculate the slew rate and signal ranges. That is input common mode range and output signals range of the 2 stage opamp.

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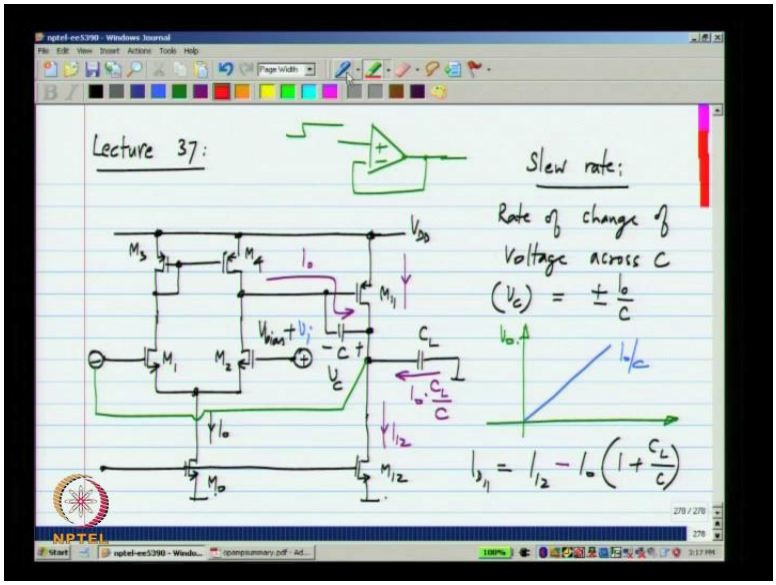

This is the second stage opamp, positive input, negative input and the output and this is integrated capacitor C. Now, we have to assume that there is some load here and the load will be connected between the output and ground. If it is the capacitor load; if it is a resister load we will see later what to do with it. We will assume that there is only a capacitor load for now. That is why the tile current of the input stage is I naught.

The slew rate as usual is limited by the amount of current flowing into some capacitor which limits the rate of change of voltages inside the opamp. As before, if we test the Opamp, the unity gain configuration that is; I make this circuit and apply a step and look at maximum rate of change of the output voltage.

The input is V bias plus some step Vi. Now, we know that for larger and larger values of Vi the incremental current in M 2 is larger and larger for very small values of Vi. The total current here will be I naught by 2 plus Gm 1 times Vi. As Vi increases the current in M 2 is larger and larger, but the increment cannot go beyond I naught by 2. That is the total current in M 2 can only be I naught. At that point 0 current will be flowing through M 1 and all of that I naught will flow from the integrated capacitor C. That will be equal to I naught for large values of positive Vi.

Now, similarly for large values of negative Vi, that is large in negative. All of the current will flow though M 1 and nothing will flow through M 2 and there is a current I naught that can go in that direction. So, what is the rate of change of the output voltage? First of all, rate of change of voltage across C, this voltage Vc that is equal to plus or minus I naught by C assuming that the current I naught will flow through the capacitor.

Now, what will be the output voltage? Remember, if you recall the representation of the 2 stage opamp at the level of transconductors, this is what we have. Gm 2, Gm 1, C and C l. Now, the second stage will be the current controlled voltage source and it becomes a current controlled voltage source because the voltage at the negative input of Gm 2 is very small. If Gm 2 becomes very large, if the second stage has an ideal opamp, this voltage will be at 0. So, this voltage is approximately 0.

So, Vc is simply the output voltage itself. Vc equals V naught. So, this is not simply the slew rate across the capacitor, but it is also the slew rate of the output. So, it looks likes the slew rate is similar to what we were get in a single stage opamp, but we have to consider other things here. Let us say that V naught which is Vc is changing at some rate.

V naught is changing at a rate of I naught by C. What does it mean? It means that the voltage across Cl which is V naught is also changing at this rate. So, the current to C l is the slope of this voltage, times the capacitance. So, the current through Cl would be Cl times I naught by C. Similarly, if the output voltage was reducing, if the output voltage

was growing, something like that, with the slope of the minus I naught by C, there would be current in the other direction. Now, also of value Cl times I naught by C.

Now, let us examine these 2 cases separately. First, let me take the first case where current I naught is drawn in this way. So, that means that the output is ramping up at positive I naught by C and that means, that current of I naught times Cl by C is flowing through the load capacitor. What does it mean? It means through M 11, we need to have current equal to the current in M 12 which is some bias current I 12, plus the current through C, plus the current through Cl ok?

So, this is I 12 plus I naught times 1 plus Cl by C. I d 11 will be I 12 plus I naught of 1 plus Cl by C. Is it possible to have this value? Yeah, because in quiescent condition the voltage here would be such that the current through M 1 equals I 12. Now as Vi increases, this voltage reduces slightly and that the increases current in this. Now, total current is limited here by how far the voltage can go, but we will assume that it is not limited. So, the current in M 11 can increase in positive direction ok?

So, in this direction, current in M 11 can increase while it is I 12 it can easily become this value by lowering of the gate voltage. Now, this may be a little confusing. Earlier while calculating output voltage, I assumed that the voltage at the gate of the M 11 is hardly changing. So, this is just approximate calculation for current in M 11 to increase.

The voltage here has to decrease, but just to be able to calculate output voltage we assume that this is fixed for calculating that output voltage. Now, while lowering the gate voltage of the M 11 the current in m eleven will increase. So, it is indeed possible to have this current in M 11. Let us see what happens in the other direction. That is why, that is I naught and that is I naught Cl by C.

And this is some I 12. So, the current through M 11 will be I 12 minus I naught times 1 plus Cl by C. Now, is it possible for this to attain any value? Clearly not. In the quiescent condition I 12 is flowing through M 11 and when we reduce Vi, I naught flows this way. I naught flows that way and the output voltage will reduce, then the current in M 1 will reduce. Now the smallest that the current in M 11 can be is 0. The current in M 11 will reduce and the smallest value of the current in M 11 is 0.

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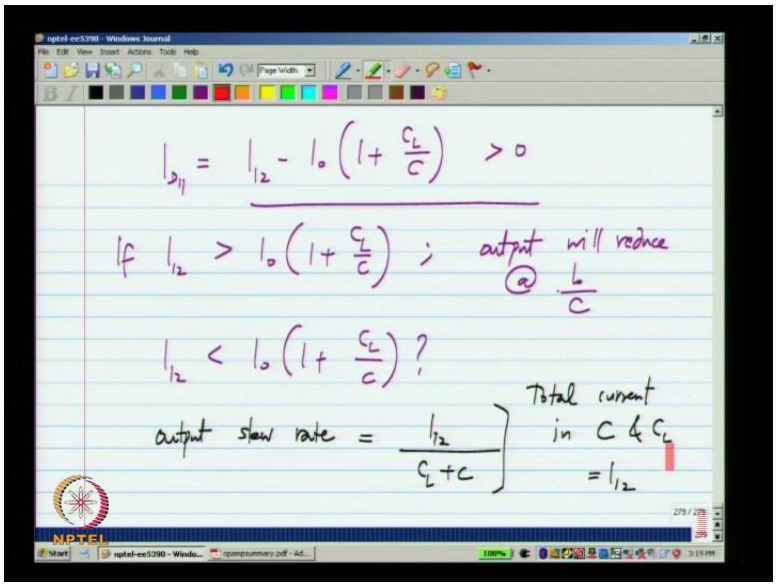

So, what does it mean? I d 11 which is I 12 minus I naught of 1 plus Cl by C must be greater than 0. Now, if this is the case, if I 12 is greater than I naught times 1 plus Cl by C, the output will reduce at the rate of I naught by C, but what happens if I 12 is less than I naught times 1 plus Cl by C. What happens in that case is that as we apply a negative step to VI and make the size of the step larger and larger, more and more current will flow into the integrated capacitor ok?

Now, before all of a current I naught can flow through this, transistor M 11 will cut off because I 12 minus the current in this, minus the current in Cl will become 0. The current in Cl will always be the current in C times Cl by C, because the output is changing at the same rate. The voltage is across the 2 capacitors are changing at the same rate. So, M 11 will cut off before the input differential pair can switch completely.

So, in that case the output slew rate will be I 12 divided by Cl plus C. This is because the total current in C and Cl must be equal to I 12 when M 11 cuts off. When this cuts off, some current is flowing there and some current is flowing there and the sum of 2 equals I 12. If that happens, then the change of output will be I 12 divided by Cl plus C.

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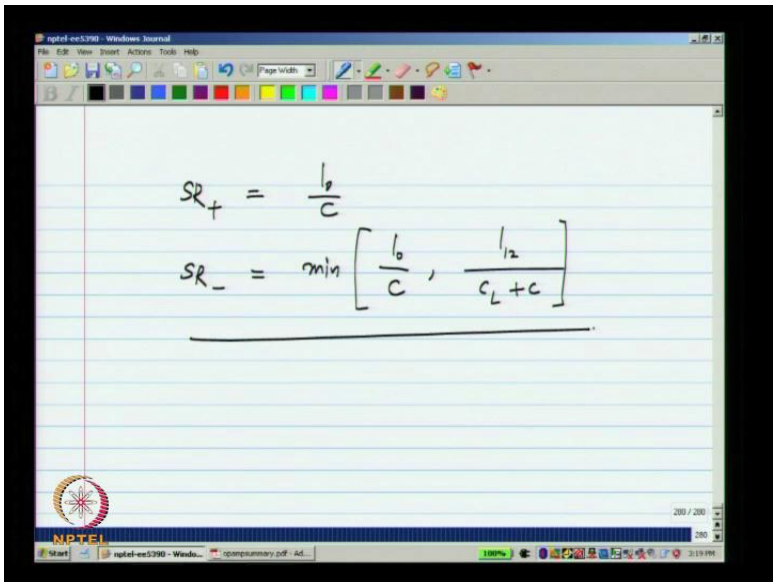

So, in 2 stage Opamp, the positive slew rate is I naught by C and the negative slew rate is whichever is smaller of I naught by C and I 12 divided by Cl plus. So, there are 2 mechanisms of slewing. Either the input differential pair can cut off, in which case maximum current out of first stage will be equal to I naught. Alternatively, the second stage can cut off, in which case the maximum current through C plus Cl would be I 12. Which of this is limited defends the value of I 12 and I naught. So, it is possible for the negative slew rate to be either I naught by C or I 12 by Cl plus C. So, this is come out for some sort of simple calculation.

This is actually an approximate calculation because we assume that at the input of the second stage we have 0 volts, but this is good upon practical purpose, this also means that if the current in the second stage is very small, then that will be the end of the rather small slew rate in 1 direction.

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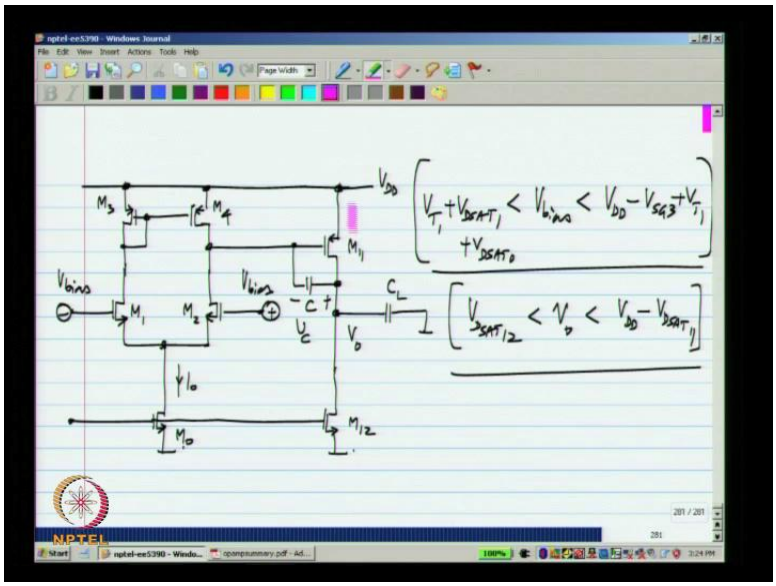

And it is also possible for slew rate to be different in positive and negative direction. So, the next thing is the single swings. Last time, we have determined, here is the single swing limits. Let me remove this feedback loop. Now, what are the limits on the input bias voltage V bias? We have evaluated this many times. If the input voltage V bias increases, the input transistors M 1 and M 2 can go into triode region and if the input V bias reduces the tail current transistors M naught can go into the triode region ok?

So, the limits are exactly the same as before. The maximum value would be the drain voltage of M 1 plus 1. Threshold voltage and the minimum value would be the old drive voltage that is required across M naught to keep it in saturation region plus the voltage of M 1. That will be Vt 1 plus Vdca plus Vdsat naught. We can see that it is very close to Vdd at somewhat far away from the ground and what is the limit of the output as the V naught increases? There comes a point where across M 11, very small falling into the saturation region. So, V naught has to be less than Vd d minus Vdsat 11. Similarly, as V naught increases the voltage across M 12 becomes smaller and smaller and at some point it will go into triode region.

That will be Vdsat 12. So, you can see that this kind of output structure, where we have a single transistor connecting to the supply voltage and a single transistor in to ground will give you the maximum possible swing limit. It can go within Vd sat of the upper rail and within the V d sat of a lower rail which is ground. In general this the maximum swing

that is possible. In integrated circuit, this is the maximum possible swing a transistor circuit. Now, there are some specials where the voltage can go above supply rail or below the lower supply rail. We will not consider that. In general, we have to leave at least one Vd sat loop on the top and the bottom.

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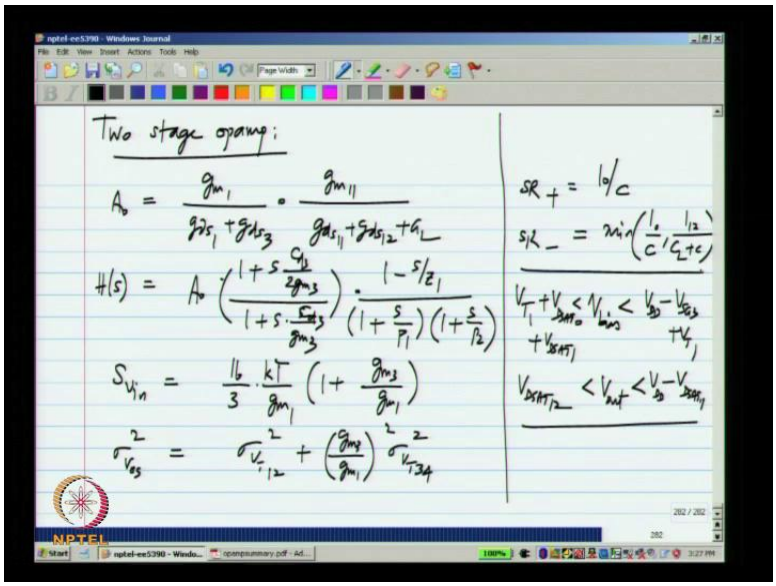

So, to summarize, the 2 stage opamp has a DC gain which is the product of the first stage and the second stage gain and the important thing is that even if you have a resistive load G l with a very high conductance, it affects only the second part of this ground. The first one can remain very large. So, that is how we will be able to operate the opamp resistive loads in the frequency response, can be return as Gm the transconductance of the first stage and the 0 and pole which appear due to current varying and right up plane 0. This should be a DC gain A naught of 0 the dominant pole and the non dominant pole.

Now, that we have spent lots of time evaluating, I am not going to write down the expression. The dominant pole appears at the output of the first stage and the non dominant at the output of the second stage and the noise and offset are contributed mainly by the first stage. So, input refer noise voltage density is that and the input referred offset voltage is that and we also calculated the slew rate and the swing limits.

So, what does the second stage opamp operate at? The other opamps that we studied so far told us first of all that it has a higher DC gain that off the small slop Gm by G 3 square. If it is a capacitive load and even with a resistive load, the first stage has to be

designed to have a substantial amount of gain. The noise and offset contributed only by the first stage. So, it is similar to what we would get as the differential pair and the slew rate. It depends on either the first stage, second stage limiting it can be similar to what we can get in a single differential pair case and finally, the signal ranges the range of input bias voltage and the output voltage are the largest waves in so far.

The input bias range is same as what we would get in simple single differential pairs case and the range of the output voltage is the largest that is possible. That is, within the Vd sat of upper rail and the Vd sat of the lower rail. Before we go further, little bit clarification on how I connected the load to the 2 stage opamp. As I mentioned earlier they are operating with a single supply. So, the input signal and the load can be connected to some bias current voltages, the V d d on the top and the ground on bottom.

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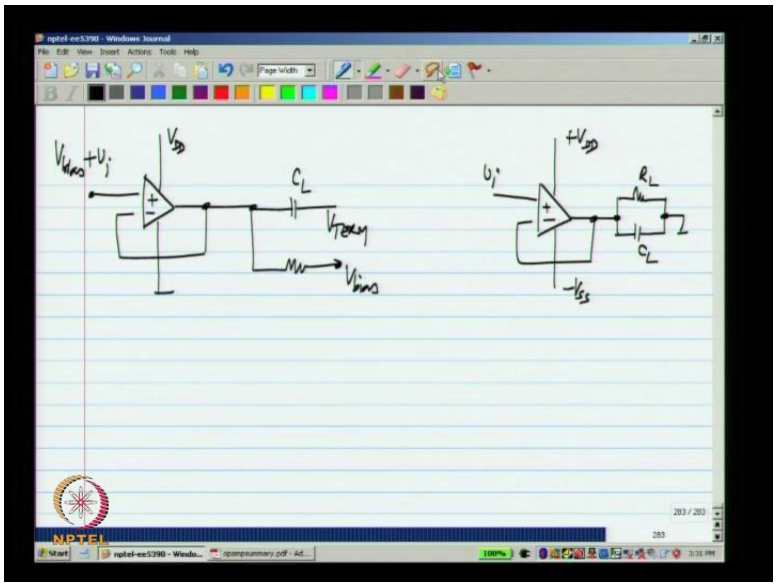

So, the input will be some V bias plus V. I have taken a voltage follower as an example, but it can be any circuit and the load that we have must also be connected to V bias ok? So, what happens is if VI is 0, the input is V bias, the output is at V bias due to feedback. So, no current will flow through Rl. In fact, this is the very similar situation to having the conventional picture of opamp with the dual supply and the load going to ground as was explained earlier. Simply by shifting all the voltages in this, we get that circuit. Now if we have only the capacitive load, it is not necessary to connect to the V bias.

We can be connected to any voltage because even if we have some DC across the capacitor, it is not going to draw any current. So, if we have only capacitive load it can be connected to any voltage. So, this V term can be anything, but we do have a resistive load. If the voltage on the right side is anything other than the V bias, even in the quiescent condition some current will be flowing out of the opamp ok?

What does it mean is, this side I have a resistor here Rl and this is at some V bias. It is different from the quiescent output voltage. Current will be flowing through that, that has to be supplied by the transistor M 11. So, that is not a good way to operate it. Just to connect a resistive load, such that the quiescent output current is 0. When we do have a resistive load, we connected up to V bias. Now, what else is there? With these opamps we have discussed single stage opamp and the 2 stage Opamp. We can make 3 stage opamp by just following this procedure. I will not discuss that in a great detail, but just put on the topology here.

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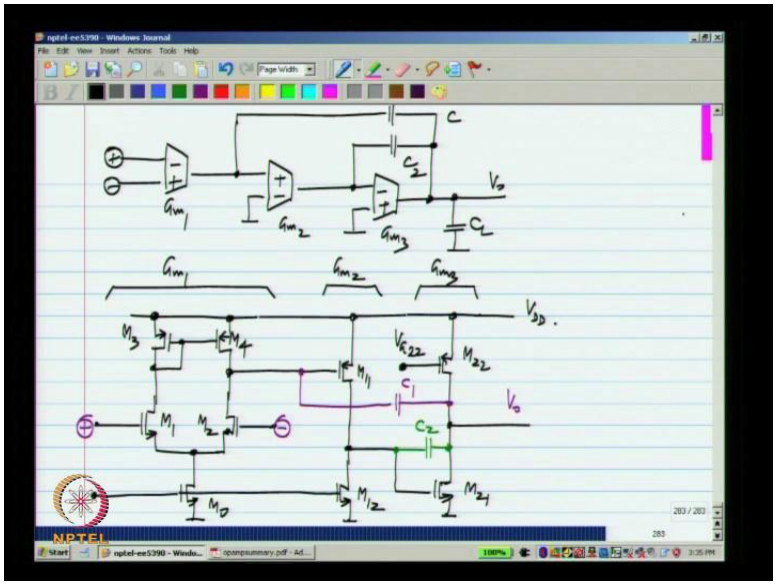

We know that at the signal level, what we need is three stages. This is the input of the opamp and that is the output. We can think of it as the input Gm 1, driving a current controlled voltage source with a transadmittance Sc and a transimpedance 1 by Sc and the current controlled voltage source is made this opamp ok?

In the 2 stage opamp itself, can through of Gm 2 as driving the current control voltage source with the transadmittance of Sc 2 and transimpedance of 1 by Sc 2. Now, how

would we go to implementing this is a simple connection of 2 stage opamp we have that can continue the same topology. This forms the second stage Gm 2. This is Gm 1 and it is required to take the difference between 2 inputs and a providing an output current and Gm 2 is single ended. In that, 1 of the inputs is at ground and Gm 3. Now, we have a freedom to chose either an nmos stage or pmos stage just for variety. Let me make this an nmos amplifier, where this pmos is biased at some fixed voltage. Now, as usual that is derived from current error ok?

So, this is Gm 3. We have to connect the integrated capacitors. That will be C 2 and this will be C here. I am not showing requirements like possibly connecting resisters in series with C and so on. This is the output. This is the negative input, that is the positive input of the Opamp. Now, exactly as we did before, you can analyze this. In fact the transfer function has already been analyzed and you can do the exact analysis including these zeros and poles. The principle is same.

The non dominant zeros and poles are sufficient at the unity loop gain frequencies. So, that the system is stable will behave. Now, at the transistors level, more stages you go to, the more degrees of freedom you have. Now, one obvious one is, now either 2 choose a nmos trans conductors or a pmos trans conductor in the third stage. I have drawn it for the nmos transconductor, but other way round is equally possible. Now, it is also possible to analyse the other parameters like the noise, offset, slew rate, swing limit and so on. It is very obvious that the swing limits are similar to that of the 2 stage opamp.

The input bias voltage limits the same and the output voltage can be within one week DC sat of the supply. The slew rate can also be calculated. It is also limited by current in first stage going to capacitor and there is a possibility of the current in the first and the third stage limiting the total slew rate as far as the noise and offset is concerned. As with multistage amplifiers, they are dominated by the contribution from the offsets and the expressions will remain exactly the same, as for the 2 stage opamps, for the simple differential pair single stage opamp. Now, one thing I did not mention earlier. Let us say we have 2 stage opamp. One of the requirements, we can do to make this more stable is to add a resistance in series ok?

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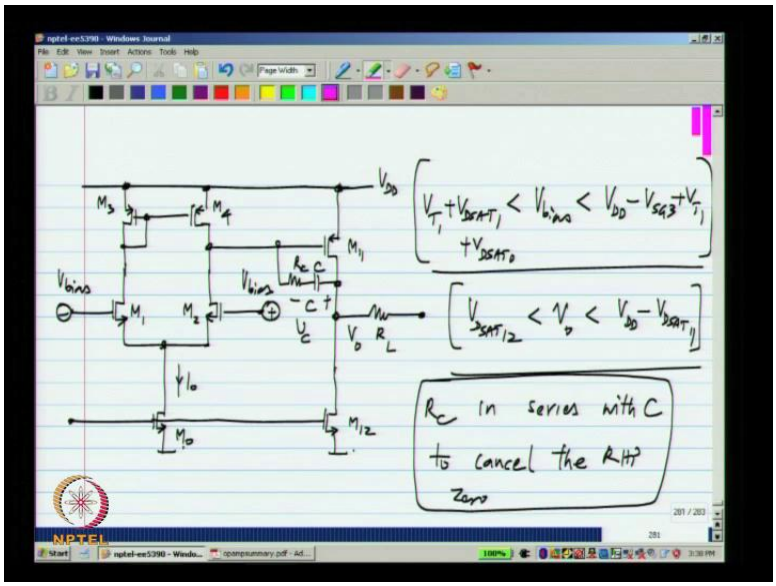

So, that the right of plane 0 cancelled it is implemented exactly as we did in the single level. That is, at the level of transconductance the value of R1 must be equal to 1 over g M 11, in this case 1 over Gm 11 of the transistor M 11. So, now to ensure that, may be difficult if you use a real resistor. So, there is a resistor we put there has to matched to reciprocal of the Gm of the transconductance of the M 11 and sometimes what you can do is to implement the resistor also has mos transistor in triode region. So, that they are matching across process and temperature corners is good similarly.

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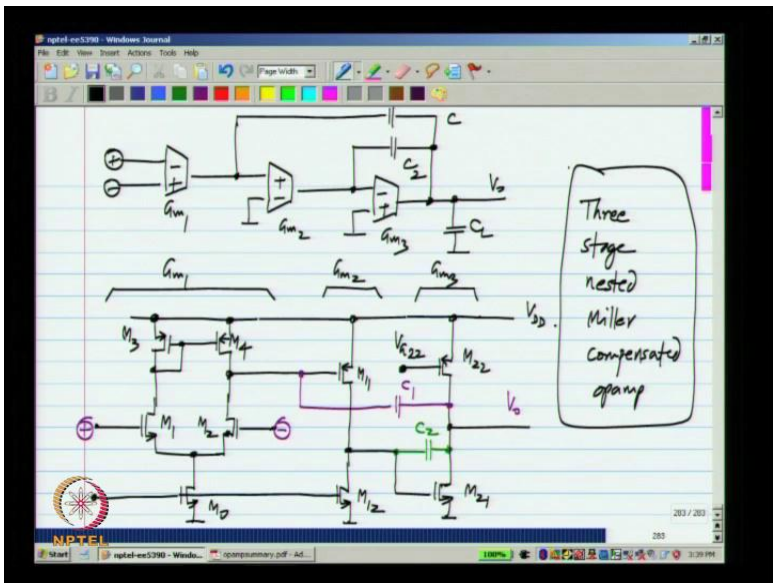

If you want to tailer to zeros in series with C 1 or C 2 or both, we can connect resistor in a 3 stage opamp. This is 3 stage nested Miller compensated Opamp. Let me copy over this circuit just illustrated the couple of details.

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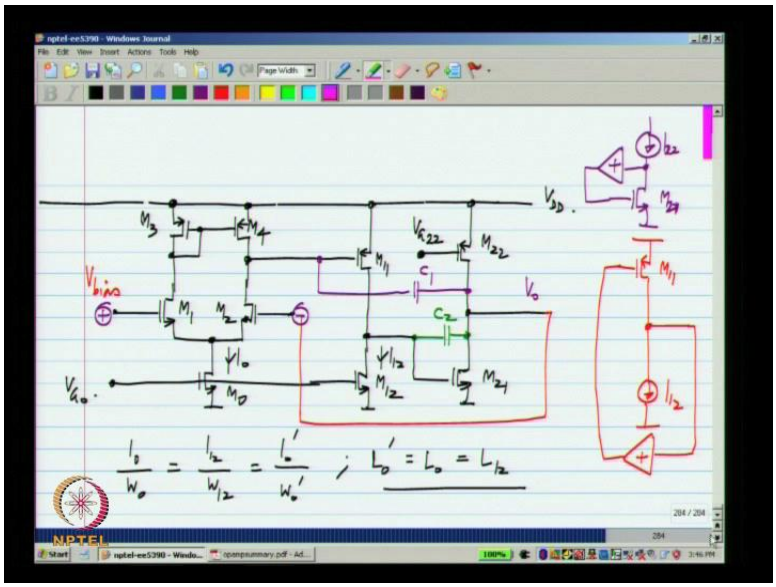

So, first of all as I mentioned earlier several times the gates of M 0 and M 22 and M 12 and so on are not connected to fixed voltages they are always derived from current mirrors. Let me call this as M 0 prime and this is I 0 prime. As usual, whenever you make a current mirror, you made a lens of all transistors same and the widths are in the ratio of currents. That you let us have this is I 0 and this is I 12. That means, that I naught by W naught should be I 12 by W 12 which should be I 0 prime by W 0 prime and l 0 prime and l 0 and l 12 should all be equal. Let us say now we did not make lengths of M 0 and M 12 equal to each other.

Now, the best thing to do is to not use common biasing line for M 0 and M 12 bias then separately for another connected transistor. Similarly Vg 22 has to come from some diode connected transistor which also is same in length and the width ratio is such that the current ratio is required. So, that is how we bias the opamp, but it is very common some.

If we slow transistors in the circuit, so it is very frequently not shown, current mirror devices are not shown. We show only that much. Now, the other thing is we have a current source going into the drain of the transistor and there is no other path for direct

current DC. Similarly M 22 is a current source that is speeding into the drain of M 21. How is this bias proper? Because, normally if I have something like this that is a I x and this is a mos transistor there what is going to be happen?

How much will be the current through this transistor? Unless there is feed back around this transistor we cannot say that the current in this will be I x. The transistor is a unilateral device. It is only by adjusting the Vg s that we can change the drain current. We cannot apply a current through a drain directly and expect the Vg s to be established automatically. We have to provide the feedback from the output from the drain side to the input side to V g s so that the correct Vg s is established for whatever bias current we want to have in the opamp. We have drawn it. The current source is going directly to the drain and nowhere else. Obviously, as we know opamp can be used only inside a feedback loop ok?

Let me again for illustration consider a unity gain pole over. What happens in that case? You have a connection from there to there and the plus input. That is why it is biased at V bias. Now, if you think of let us say M 11, M 12 states, let me redraw that here. So, this M 12 is a current source. So, I show it as a current source. This is I 12. There is feedback through this M 21 and through the input differential pair. Now, if you see from here to there, there is an inversion. This is a common source amplifier and from there to the drain of M 2, there is an inversion. So, what we have is some amplifier with a positive incremental gain feeding back to the gate of M 11.

We know that this is exactly what we need if the voltage here increases. That means, that the current in M 11 is too much and gate voltage should be increased so that it reduces and vice versa for smaller current. Similarly, if we think of M22 and M 21, M 22 is a current source I 22 and this is a M 21. So, that again is the gain from here to there is negative and the gain from there to there is negative. It is a common source amplifier. So, we have a positive incremental gain amplifier connecting that way and we know that if we do that M 21 is a negative feedback and a current I 22 flows through that.

So, if there is DC negative feedback around the entire opamp, each of these stages will be negative feedback and everything will be biased correctly. If you operate the opamp in open loop, there is no guarantee that bias current will flow through the transistor because we have to establish the Vg s for the transistor for correct current to flow. Now,

while discussing opamp, already we have heard that we have to use them in negative feedback this is the reason ok?

If they are not in negative feedback and you apply a 0 differential input voltage, there is no guarantee that the opamp will be biased properly. In fact, because of mismatches and so on there is almost guaranteed that the transistor will all being some triode region. 1 of the transistors will be triode region. That is about DC negative feedback around the opamp.

Now, let us say the 2 stage opamp used a gain of Gm by Gd s square. Let us say we want even higher gain. What should we do? For a 3 stage opamp and we can go for 4 stage opamp and so on. That is possible. That is one of the ways of doing it. Also there are other ways. What we want to do is to go through the DC gain. What did we have?

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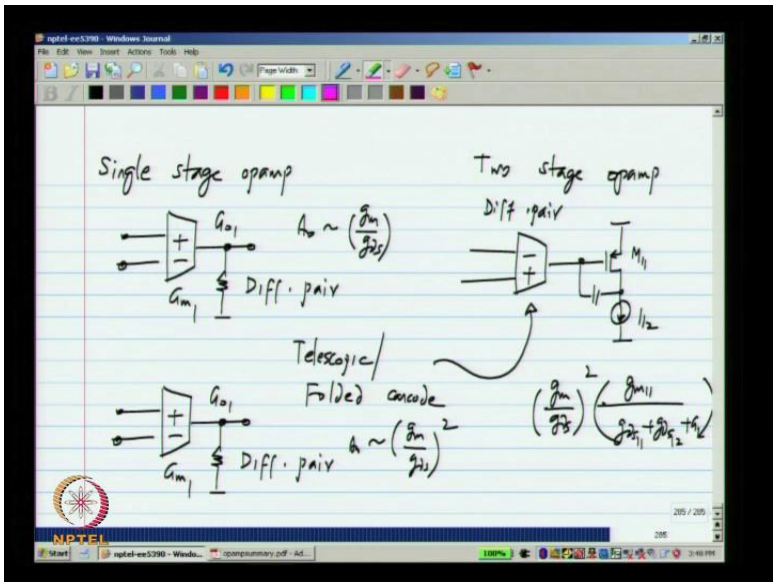

We have a single stage Opamp of some Gm 1 and this is just a differential pair. It has some G naught 1 and the DC gain approximately Gm by Gd s of a single transistor. We can also simplify this by going into telescopic or folded cascade. What that will do is to have a similar topology.

But the gain will be approximately Gm by Gd s square. Now, we had a 2 stage opamp. We use a simple differential pair here followed by the second stage that is M 11 with a current I 12. What we can instead do if you use a telescopic or folded cascade at this

stage. If we do that, what happens is the gain of first stage increases. It will be of approximately G m by Gd s square and the second stage will have a gain of Gm 11 by Gd s 11 plus Gd s 12 plus Gl.

So, by increasing the first stage gain, we can increase the gain of overall opamp. So, we can still stay with 2 stage. Which means that the composition scheme, the scheme to make the opamp behave like a integrate is as same as 2 stage opamp, but the difference is… So, we can stay just with 2 stages and have a higher gain by making first stage as a telescopic cascade opamp or a folded cascade opamp ok?

This is the very commonly used technique as what does it happened is that as we go finer and finer technologies that is shorter and shorter channel lengths. The problem is that the Gm by Gd s transistors will keep becoming smaller and the smaller. This is simply because the length is becoming smaller. Now, if we make the length higher and a higher values of Gm by Gd s, but that reduces the speed. So, if you stay with shorter channel length, the way to increase the gain is to go for a cascade first stage and the second stage so that with 2 stages you will get a very high gain. So, that is very much possible and that is also quite frequently done.

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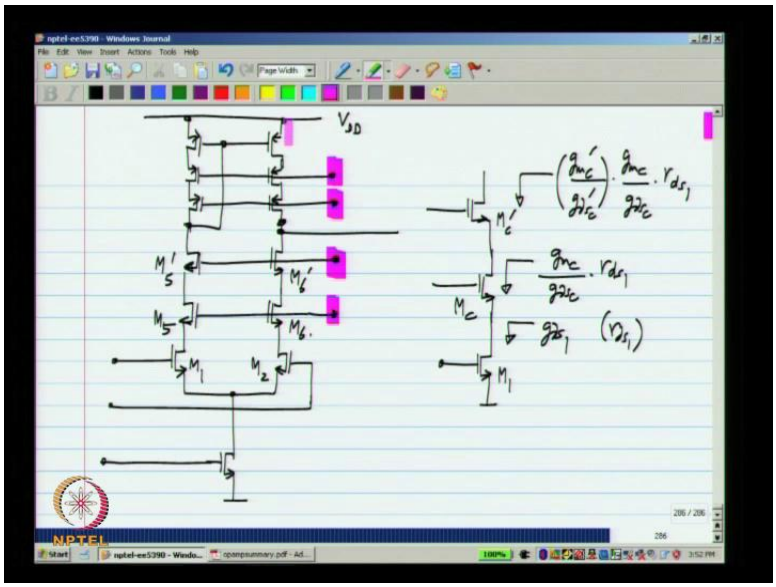

Now, another possibility is that we used not just 1 cascade, but 2 cascades. Usually such a thing is called as triple cascade. I will show it for the telescopic cascade topology. Now, just to illustrate the principle, I will show also a just common source amplifier

looking in here. That is why it is M 1. I will have Gd s 1 as the output conductance or Vd s 1 as the output resistance.

If I cascade with C, the output resistance will be Gm c by Gd s c times Rd s 1. I could cascaded with 1 more transistor that is why M c prime the output resistance will be Gm c prime by Gd s c prime Gm c by Gd s c times Rd s 1. So, it is even higher. Same thing can be done with the opamp as well. This is a differential pair of 2 cascades ok?

We have M 1, M 2, M 5, M 6 earlier and that is why I call it as M 5 prime and M 6 prime and similarly on top I need to have a current source with 2 cascades. There is no point in proving only one side on both sides is contributing to the output conductance. So, I should have a current mirror which is also triple cascaded. So, we need to establish a bias voltages at all these points. So, that all transistors remain in saturation and afterword similar thing can be done with folded cascade as well. Also an additional constraint is that we have now stacked more transistors.

So, that means, that things will be constrained more even before. So, we can have more and more cascades, but we will have lesser and lesser swings, but when you have a 2 stage opamp the swing at the output of the first stage does not have to be very high with this. It is possible to do this. So, some times when you want even higher DC, you can go for something known as triple cascade in the first stage and in the second stage ok?

There are lots of alternatives and lots of possibilities. One of the reasons why you should not try to remember the topologies without understanding what is going on behind them is because I have some basic topologies. I can combine them in many different ways to get seemingly very different alternatives, but once you understand the underlined principles they are all the same. So, we started with a single stage opamp. We went to telescopic and folded cascades. That is one way of increasing DC gain. We can go to 2 stage opamp as another way of increasing the gain.

So, in some ways the 2 stage opamp and the telescopic or folded cascade will have same DC gain. If you have a capacitive load, you have a resistive load. You cannot use cascade stage because that only increases output resistance, but does not increase the transconductance. Now, if you want further increasing gain, you can go for 3 stages or 4 stages or you can go for triple cascade telescopic stage or triple cascade folded cascade

stage. Alternatively you can combine the 2. You can have a telescopic stage followed by second stage or a folded cascade stage followed by second stage and so on.

The possibilities are endless and it is up to you as a designer to pick the right one for you. If you understand the trade of arrival you will be able to do that. Now, as usual in design you have a number of parameters and you will not be able to put down all the parameters on the paper and then turn them into equations and get the dimensions of all transistors ok?

It is very important to understand what to change if something is deficient. Let us say you have designed a 2 stage opamp and you have to find the dc gain to be too little. What can you do? You have to increase the gain of the first stage. That is an easy possibility or you increase the length of the transistors of the first stage or you go for the cascade for first stage. Those are all the possibilities ok?

Similarly, let us say you find that the input of the noise of 2 stage opamp is too much. Then what you will do? You know that is the first stage so, you have to manipulate the first stage in some way and you would not like to affect the transfer function at all. So, you do noise scaling for the first one. You do impedance scaling for noise scaling for first stage. Now, that way increases the transconductance of first stage. It means that you have to change the integrating capacitor so that your opamp behaves exactly as same as before. So, you may have to change different things by keeping some other things constant.

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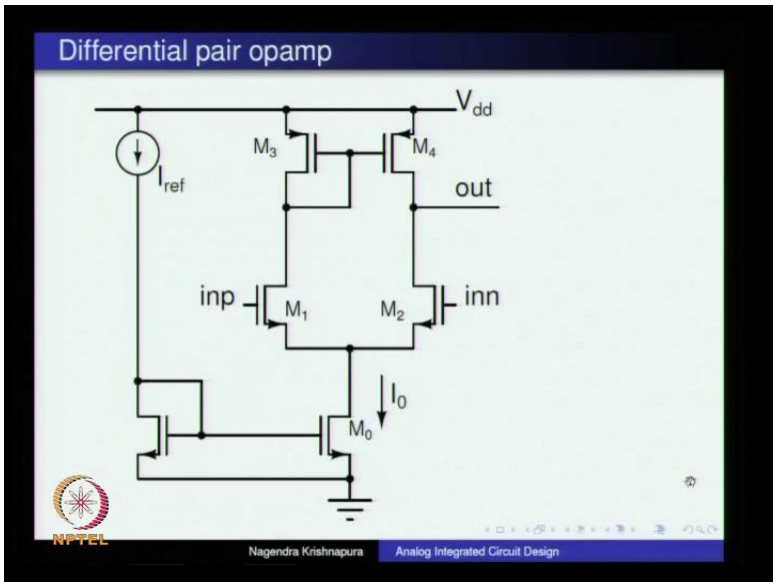

So, if you understand the basic principles very well, you will be able to do this quite easily. This is a quick summary of opamps that we studied so far. This is the differential pair opamp.

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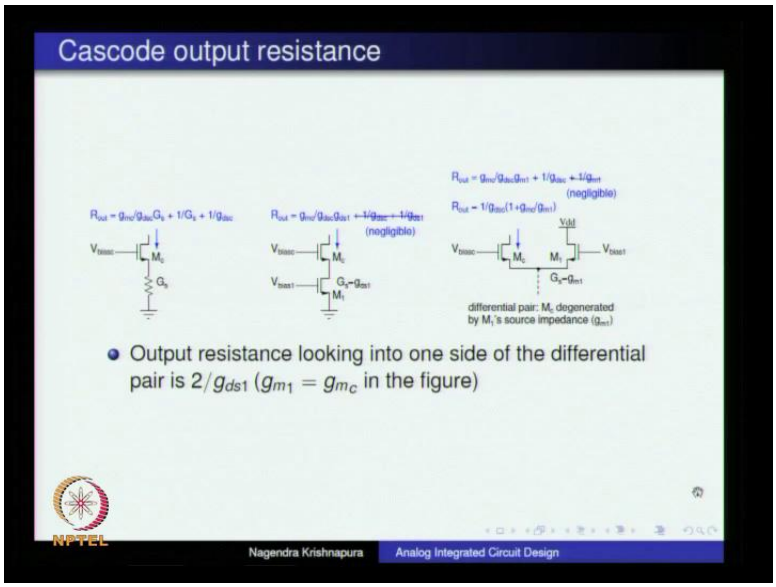

Now, the output resistance can be calculated using this. We know this is the output resistance of the cascade. It is given by this formula. When we have a resistor with conductance Gs and the source of the transistor Mc, we have another transistor. It will be Gd s 1 instead of Gs and finally, if we have a differential pair, it is as though this

transistor M 1. The impedance looking at source is at the source of this transistor Mc. So, Rout is 1 over Gd s c times 1 plus Gm s by Gm 1 and Gm s happens to be equal to M 1. This is simply Gd s c or the output resistance is 2 times Rd s c.

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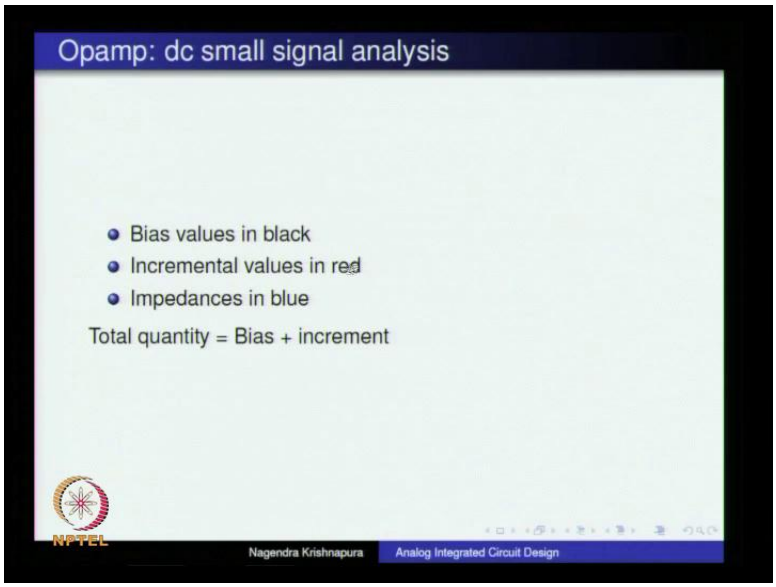

The following slide shows all Opamps with bias values in black, incremental values in red, impedance in blue. The total quality of course is bias plus increment.

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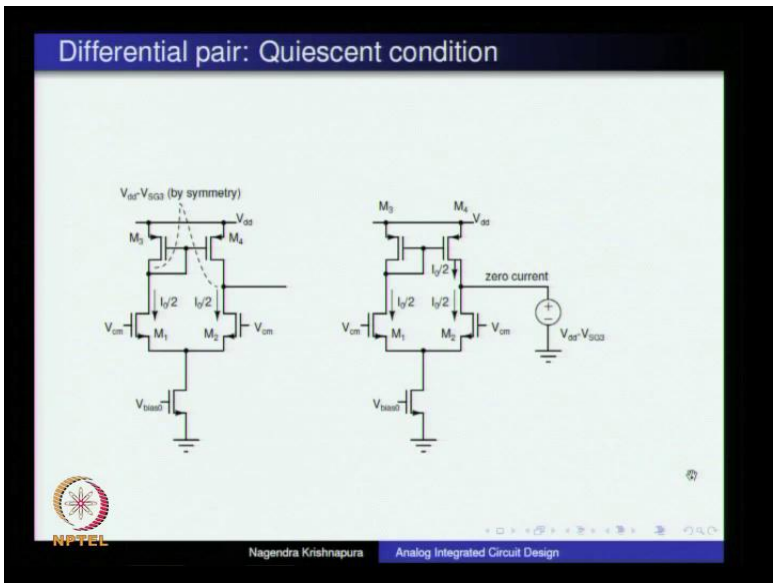

So, we said that this and that voltages are equal by symmetry. That is how we started the analysis. So, if we terminate Vd s plus Vg s 3, nothing will flow there and I naught by 2 flow through all these 4 transistors where I naught is the tail current.

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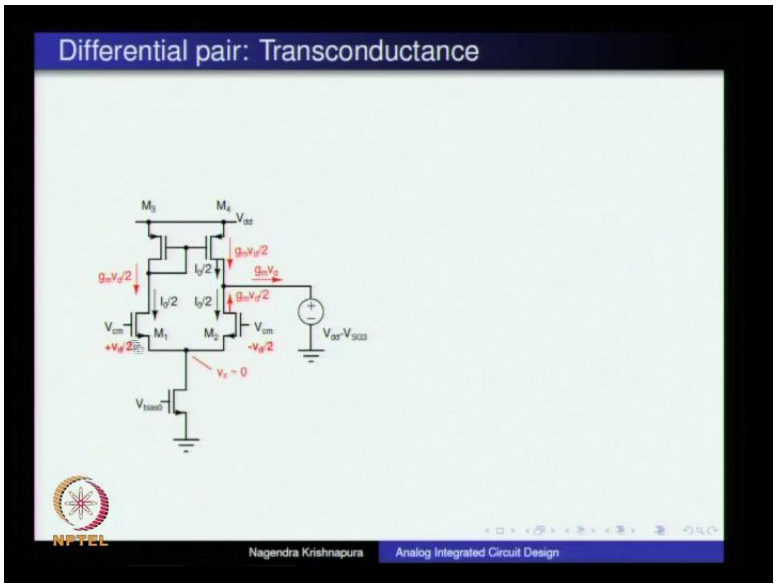

To calculate the trans conductance, we have this incremental voltages Vd by 2 that cause the current Gm v d by 2 here and G m v d by 2 in the opposite direction. So, net current of Gm v d is flowing through the output.

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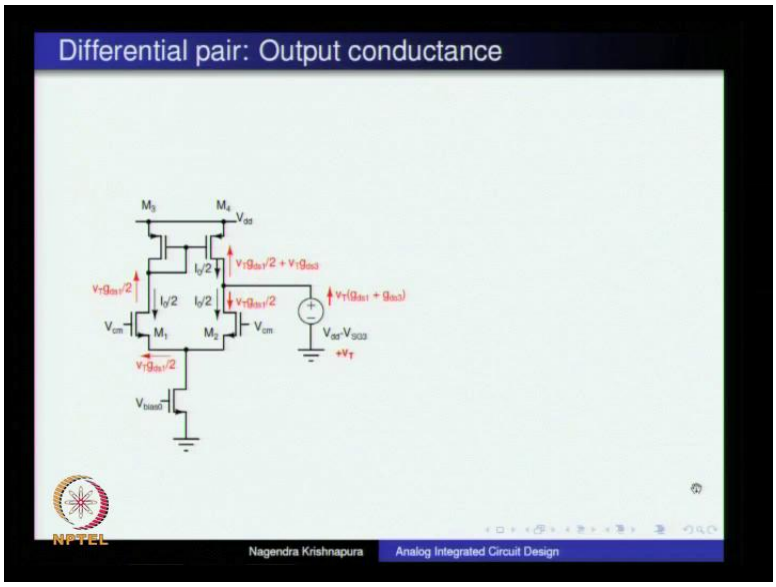

To calculate the output conductance, this is what happens if we apply a positive voltage Vt. We will have Vt of Gd s 1 by 2 flowing this way and that will also get an error. So, Vt of Gd s 1 by 2 will flow there plus Vt of Gd s 3.

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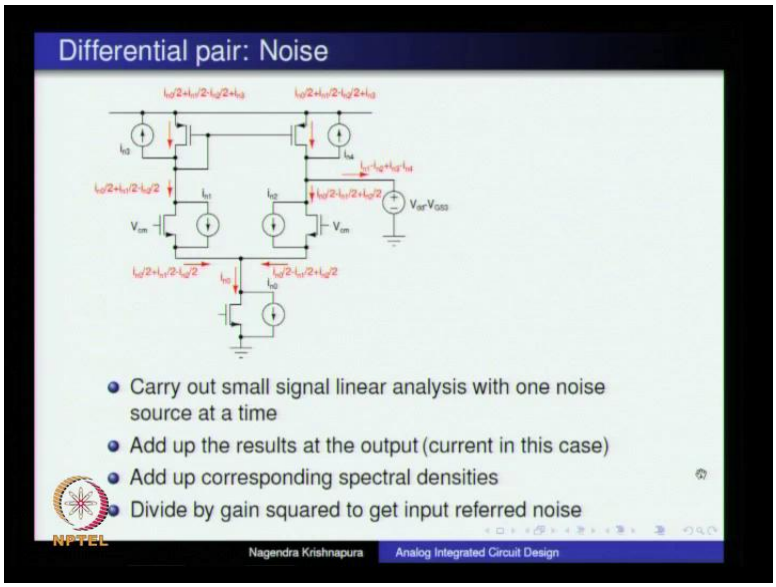

So, that is how we get output current at Gd s 1 plus Gt s 3. So, similarly we can calculate the noise and the other parameters. We will continue with that in a next lecture.