Analog Integrated Circuit Design
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Lecture No - 38
Common Mode Rejection Ratio; Example

Hello, and welcome to lecture thirty-eight of analog integrated circuit design. We have been looking at opamps at the transistor level and some detail, we saw how, we can make a single stage opamp and improve the d c gain by adding a second stage, and a third stage. So, on now we had already discussed all these things at the control source level, we also know how to make it at the transistor level, we also saw that the different stages of the opamps will be biased properly only when d c negative feedback is applied around the opamp. This is something that being known already that an opamp was always be used in d c negative feedback. Now you can see why if you do not do that? 1 or more of the stages inside the opamp will not be biased correctly.

Now in this lecture will mainly talk about the 1 particular aspect of the opamp, and also in many another circuits that is the common mode rejection. Now before, we go there I will briefly touch upon how to get even higher gains, let us say with the 2-stage opamp. It is a very simple technique. It is a combination of things that, we have seen already we look at that, and then look at common mode rejection of different circuits and why it is important?

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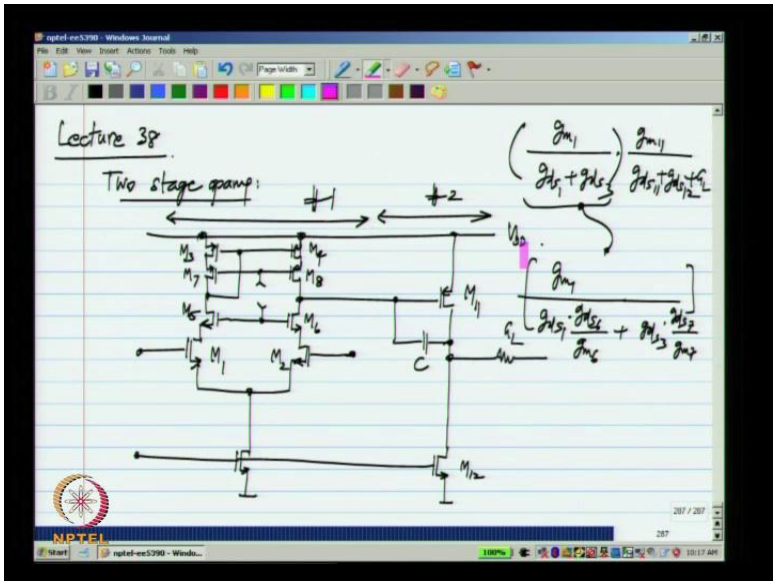

So, on now our 2 stage opamp look like this. Now this is the first stage and that is the second stage, and this is the output. Now if you want to have an opamp with a higher gain, then we can of course, go for a 3 stage opamp, but that needs a more complicated frequency compensation scheme.

We need to make sure that each of the smaller loops is stable, now a simple technique to increase the gain of this opamp is to simply replace the first stage. Instead of using the simple differential pair single stage opamp, we can use a cascaded single stage opamp for example, I can use a telescopic cascade opamp I will not show all the biasing details here. So, assume that these voltages are appropriately set the keep all transistor in saturation, now what happens is the gain of the first stage is higher originally, we had a total gain of plus g l, which is the conductance of any load that you connect now this part of it will replace it by. So, it will be replaced by the expression for the gain of the cascade amplifier this number is going to be much higher than that 1.

So, the overall gain also is going to be correspondingly higher. So, this is the simple way of increasing the gain d c gain of the 2-stage opamp, and integrating capacitor of the compensating capacitor exactly the same as before. So, similarly we can use a triple cascade or a folder cascade as the first stage, now whether you choose to do this or not depends on the available hydrom the input common mode range that you require. So, on actually becoming very common to do this, because as you go to deep sub micron processes the value of g m by g d s of a single transistor whether short channel length is rather small. So, you need to have higher gains and very convenient way of getting reasonably high gain is to use the cascaded first stage followed by a common source second stage.

Now we will move on to a very important topic with a opamps and many other sources circuits. In fact, which is the common mode rejection, now we have dealt with this earlier I showed the example of an inverting amplifier and a non-inverting amplifier. Now the amplifier was assume to react only to the difference between the input voltages, but the opamp also reacts the average value of the input voltage or the common mode input voltage. In this case we saw that there is a distinct difference in the behavior of the non inverting amplifier and the inverting amplifier, and that is because the non-inverting amplifier as a very large input common mode voltage for the opamp whereas, the inverting topology has a very small a common mode voltage wink, now let us look at the

common mode rejection of the opamp that we have design, and also we look at another circuit for, which will calculate the common mode rejection and see what the bad affect of having a poor common mode rejection as.

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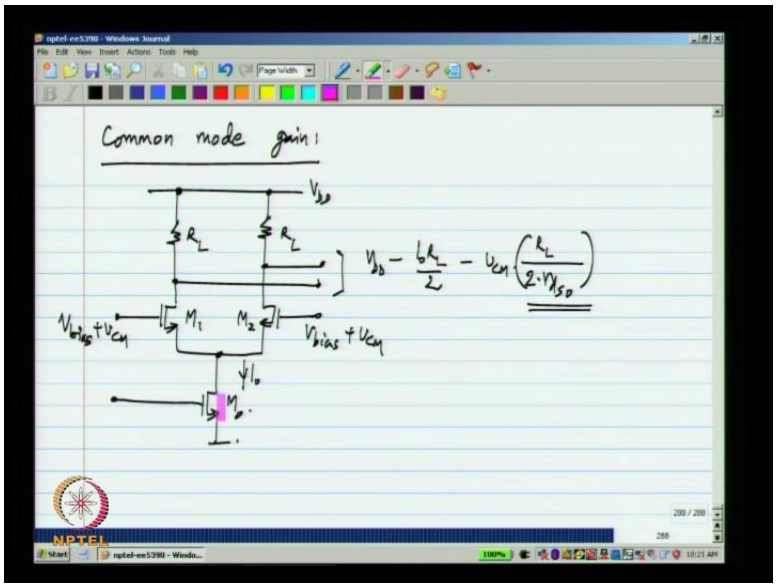

We have already looked at a common mode gain of a stage like this loaded by r l, we know that if we apply a small single common mode voltages to the 2 sides. The outputs will rise up together and the common modern gain will be this is approximately. The common mode gain have ignored the g m's of m 1 and m 2 are assume that the output resistance of l not is... So, large that the common mode gain can be approximated by r l by 2-time r d s 0. So, we can improve the common mode rejection by improving the r d s of the tile current source m not and that is basically mainly, what the decides the common mode gain? And consequently the common mode rejection ratio. Now the single stage opamp will have it is a slightly different topology, we do not have registers, but they have a current mirror load.

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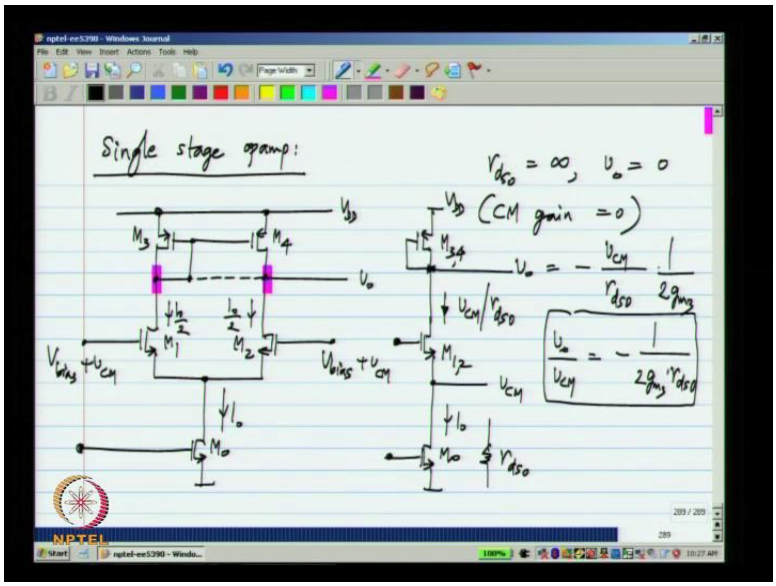

Let us say again we apply only a common mode small signal input that is identical input to the 2 sides of the differential pair. Now how do we figure out the what the output voltages? First of all we know that when the circuit is perfectly symmetrical that is m 1 and m 2 are identical m 3 and m 4 are a identical the voltages here, and there will be exactly identical, we have argued earlier by contradiction that if this voltage will difference from the others, you will find some inconsistency, because you consider the currents in m 1 and m 2 and the effect of v d s upon them and similarly the currents in m 3 and m 4 and the effect of their v d s upon them, and you will find that the only consistent solution is to have v naught equal to that voltage.

Now when you apply voltages to the 2 inputs v c m and v c m the same thing still applies. In fact, you can think of this is simply changing v bias; we have not changed anything at all. So, that is 1 thing now also the currents will divide equally between m 1 and m 2. If the current here is a certain value of i naught the current here will be i naught by 2 and the current there will be i naught by 2, let us say current source i naught is ideal that is this i naught does not depend on the voltage across m naught.

In that case even if you apply signal here this voltage will change the voltage of the tile not will change, but the currents do not change. So, that voltages at the drain show m 3 and m 4 will remain as they are... So, as before if already is 0 as infinity the output voltage will be 0 that is the common mode gain will be 0, but of course, in reality this

current source will be imperfect, and we will have some change in the voltage what happens is when you apply v c m this voltage will change and how do we evaluate the changes, and so on. The easiest way to work this out is to make use of the fact that the drain voltages of a m 1 and m 2 are identical, if these 2 voltages are identical what you can do? Is the simply tie them together and analyze the circuit this is the very common technique of analyzing circuits.

So, I am going to do that and the circuit will become a lot simpler. So, if I do that what happens is m 1 and m 2 are in parallel and m 3 and m 4 are in parallel, and I will rewrite the circuit with m 1 to, which means that it is a combination of m and m 2 and we have m 0 as it is and here we have m 3 and m 4 in parallel and there drain is connected to the gate, because you see that all these 3 are connected together, and v bias plus v c m is applied there, now as we saw before that transistor m 1 to behaves like a source follower. So, n is signal at the gate appears at the source with a gain of almost unity, now we know that this answer is different when you have body effect, and also when you have a finite resistance r d s 0 for m 0. I let you work that out workout the exact result here I will approximate the voltage of the source by v c m, now if this is v c m and the transistor m 0 as a as an incremental resistance r d s 0 the incremental current here. In this transistor will simply be v c m divided by r d s 0 and that incremental current flows into the g m of m 3 and m 4 in parallel.

So the output voltage will be nothing, but minus v c m by r d s 0 and the impedance looking into the diode connected transistor will be the combine g m of m 3 and m 4. This will be 1 over 2 g m 3. So, v naught by v c m is simply equal to minus 1 over 2 g m 3 r d s 0. So, couple of things to not just like before the quality of the current source decides the common mode rejection, but also the situation is better than before by using the active current binary load what we have got is an enhanced common mode rejection.

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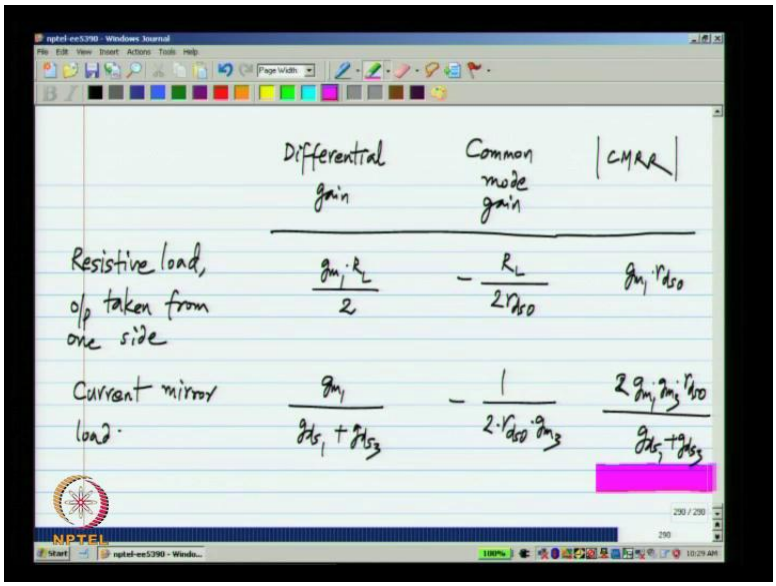

Now, let us say we have a differential pair with a resistive load and output taken from one side the differential gain will be g m 1 r l divided by 2 and the common mode gain will be r l by 2 r d s 0 will be negative, and if you have your current mirror load the differential gain will be g m 1 by gds 1 plus gds 3 and the common mode gain will be minus 1 over 2 r d s 0 g m 3, and the contrast is obvious if I calculate the c m r r, which is the ratio differential gain into the common mode gain and I will just show the absolute value of that, which is g m 1 times r d s 0. In this case you see that r l by 2 appears in the differential gain, and also in the common mode gain whereas, with the current mirror load in the differential gain the get 1 over gds 1 plus g d s 3 and in the common mode gain.

We get 1 over g m 3 the common mode load impedance is much smaller than the differential load impedance. So, that gives a further enhancement of c m r r. So, this will be 2 times g m 1 g m 3 r d s 0 by gds 1 plus gds 3. So, this common mode rejection of the differential pair with the current inner load is much higher than that of a differential pair with a resistive load now this is a good thing. So, this means that it does not respond as much to the common mode.

When you add a second stage that second stage does not differentiate between common mode and differential inputs, because the first stage is already converted the differential input to a single ended output. So, at the output of the first stage once you have a signal it

cannot be distinguished, whether it comes from a differential input signal or a common mode input signal. So, the second stage will react in the same way to the common mode input to the opamp and it differential input to the opamp so; that means, that the common mode rejection ratio will not change.

So, the common mode rejection is determined only by the first stage this is a common characteristic all opamps and with an active current mirror load the common mode rejection ratio is much better, now while synthesizing the opamp topology, we came up with the current mirror as a convenient way of providing a bias for the current i naught by 2. So, it is actually really a lot more than that is not merely providing a bias. It is also providing an enhance common mode rejection, now what is the effect of common mode rejection on the operation of the opamp? We have already seen what happens with inverting our non-inverting amplifiers, now we are look at another example about operating with different supplies and common mode voltages for the amplifiers, and see what happens I earlier said that any opamp can be operated with the single supply or a dual supply.

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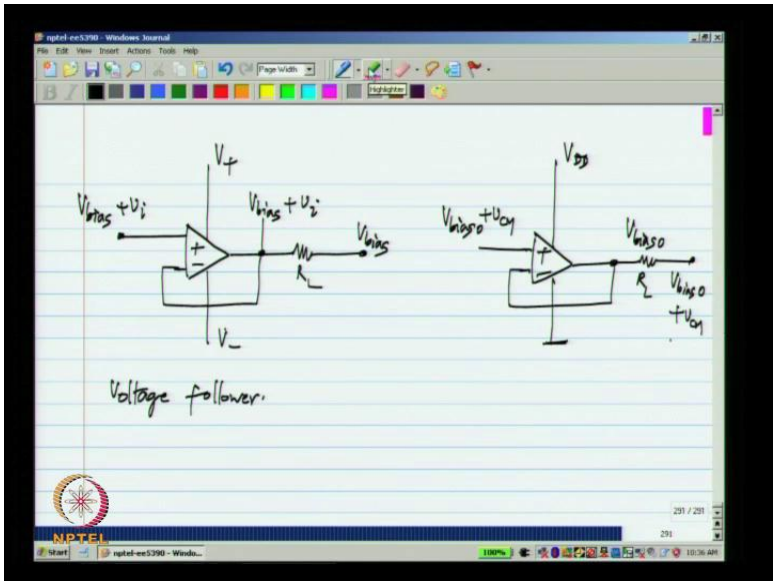

Now, let me take a very simple amplifier, which is a voltage follower now what does it mean to say that? I can have single supply or dual supplies first of all what it means is I can have any value of v bias here and v bias is there, and I can apply an input signal and output here will be at the same v bias plus v i.

Now this is true if the common mode rejection of the opamp is input finite. So, regardless of any value of v bias the output will be equal to v bias and any increment that you apply will come out exactly as you applied, now in case of c m o s opamp we talk about a single supply operation, which is some v d d and 0, and we apply bias v bias the load is connected to the same v bias now what is it mean to say that? The opamp as a finite common mode rejection what it means is that the output voltage will change depending on the common mode value. So, what it really means is just for simplicity, let me remove the mode resistance, because of a finite common mode rejection as I change the value of v bias. The output will change now how do the change ideally? If I apply any value of v bias there v bias should come out, because this is a unity gain follower. And let us assume that the opamp does not have any offsets and. So, on in reality what happens is different.

Now, let us assume that there is some value of v bias v bias 0 for, which the output is exactly equal to v bias 0. So, let us assume that there is some voltage for, which the output of this is exactly equal to that 1 this is the ideal operation of the voltage follower. Now, let me change the value of v bias, you can think of this is changing the value of v bias or changing the input have put the load back just to emphasis that the other side of the load is connected to v bias 0. In this case again no current flows through r l and the situation is exactly as before if for v bias 0 the output will be v bias 0, and the opamp does not supply any current, now let me change the value of v bias 0 that I will think of is applying some common mode voltage. So, I will apply a common mode voltage to this and a common mode voltage to that 1 now, what should happen? Is that the output should be at the exact the same incremental voltage as before.

The common mode rejection ratios I extremely important in many circuits, now in the case of that we have taken. So, for it depends on the topology of the opamp now what happens if you have a finite common mode rejection ratio is that if you change the input common mode voltage of the operation the opamp behaves differently. So, the output offset for instant depends on common mode input of the opamp now earlier, we said that the opamp can be operated with either with single supply or a dual supply and the behavior will be exactly the same.

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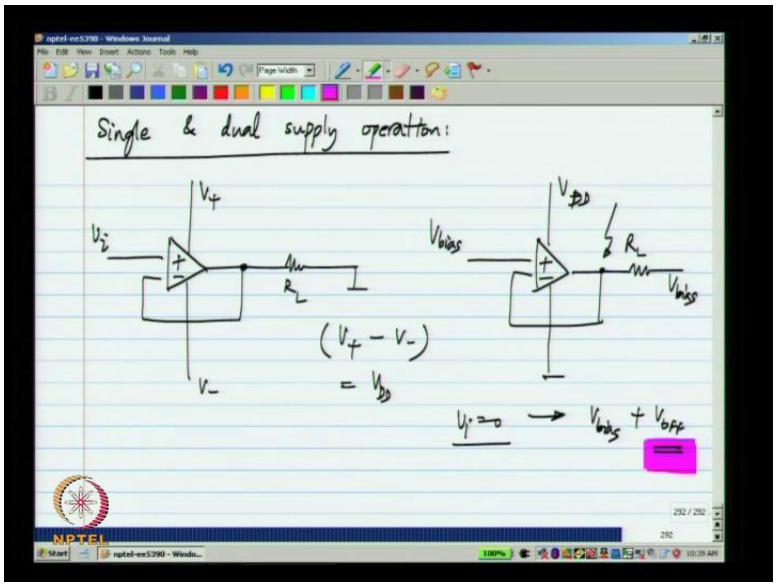

We have any circuit for simplicity I will take voltage follower. I said that we can operate with the 0 common mode voltage and only an input that is 0 bias voltage and only an input or let me call this v d d and 0, and have a bias voltage for both the input and output, and if I apply an increment here, I get the same exact same output in the 2 circuits provided that the supply voltages are the same that is v plus minus v minus the total supply voltage equals v d d minus 0.

Now, reality somewhat complicated so for we have not discuss the influence of v bias at all we only said that this value of v bias has to be within the common mode range of the opamp you know that there is some input common mode range for the opamp, and that is decided by the input stage, now and v bias can be anywhere within that range when reality what happens is if the value of v bias changes, because of the non-0 common mode gain of the opamp. The output will change in somewhere. So, let us I do not have the input. Now as I go on changing the v bias the output will change in somewhere, now when I do not have an input that is like saying I have v i, which is equal to 0 when I have v i equal to 0. What should the output be? It should be v bias, but there will be some offset voltage from v bias.

Now, what is it mean to say that? I have non-zero common mode gain when I change v bias the output will change so; that means, that I have changing output offset voltage. So, if you think of a d c voltage follower what happens, because of the non-zero common

mode gain of the opamp is that the output offset will change when you have a dynamic signal like a sine wave, now in every part of the sine wave will have a different offset and this is like having a distortion. Now this is a very important thing. So, it is not true that the input can be biased anywhere within the common mode range not depending on the common mode rejection ratio.

As you change the input bias voltage the output will change, now to minimize this effect the common mode rejection ratio has to be as I as possible, now in general this common mode rejection is something that bothers you whenever you intend to take the difference of 2 signals, but you also end up responding to the average of the signal, now a voltage is always measured between two points and you always want to take the voltage between two specific points. Now there are many cases the voltage across those 2 point is rather small, but the average of these 2 voltages with respect to ground the very large now, why is the average voltage relevant?

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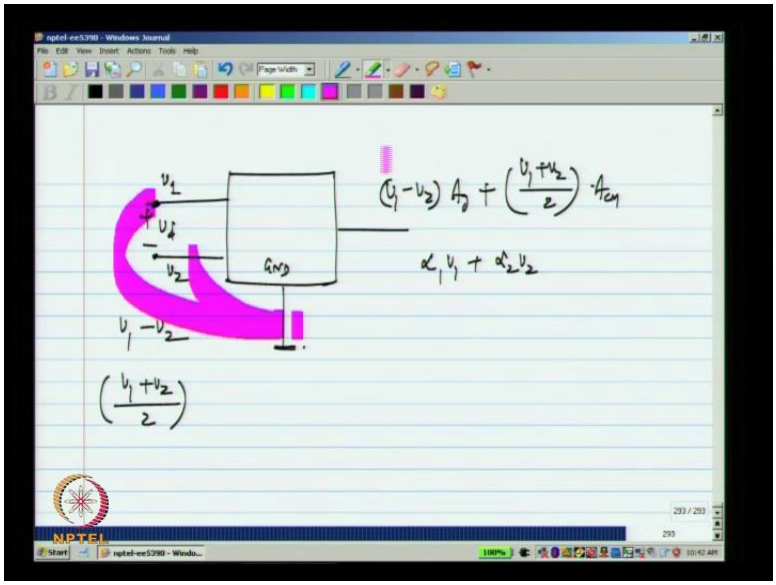

Because in general we will not have any circuit that responds only to this voltage, now all circuits will have some common reference point, which is the local ground of the circuit and what you really respond to is individual voltage is v 1 and v 2 with respect to ground. Now you design circuit. So, that it respond predominantly to v 1 minus v 2, and it does not respond to v 1 plus v 2 by 2 as we have discussed earlier, we can think of the voltage v 1 and v 2 individually or as the different and common mode voltages.

Now, because it always response to the 2 individual voltages v 1 and 2, we cannot always guarantee that the output response will be of the form v 1 minus v 2 times something. So, usually what will happen is you will be v 1 minus v 2 times the differential gain plus v 1 plus v 2 by 2 times some common mode gain notice that this is exactly the same as writing some alpha 1 v1 plus alpha 2 v 2, but since we usually I want the differential response to be large and the common mode response, which small it makes sense to write it in respond.

So, the real problem is when a c m is non-zero and v 1 plus v 2 by 2 happens to be large, now what I will do is I will discuss an example, circuit for which this common mode rejection is going to be important, and is also serves as a kind of an example, for calculations of mismatch, now this is not related to the common mode rejection of the opamp itself, but the common mode rejection of some circuit, which is supposed to respond to the difference voltage that is the difference between 2 input voltages.

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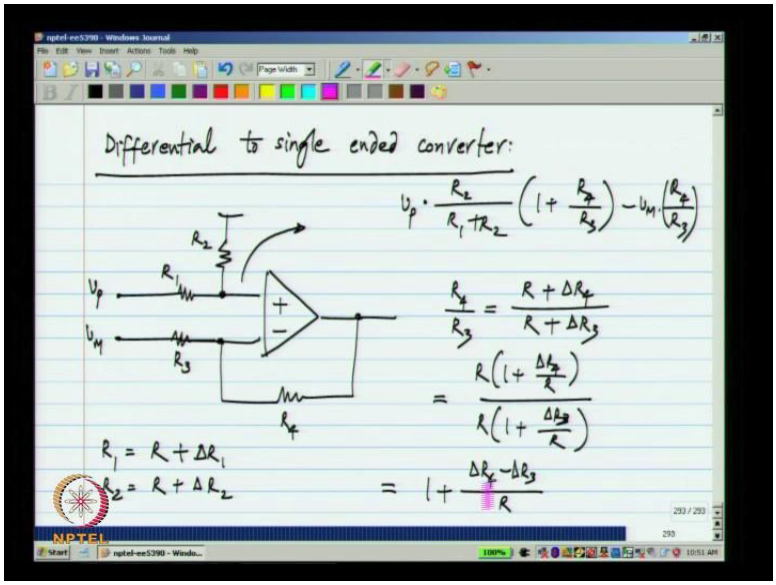

And it is known as a there are many cases in which, you have 2 inputs v p and v m and you want extract v p minus v m, now how do we do that, let us I add v m al1 and I wanted to get minus v m. What would I do? I could use an inverting amplifier of the gain minus 1. So, that is the I make this r and r. I know that the output will be minus v m and this is the opamp, and ideally it keep these 2 voltages the same, and the output will be exactly equal to minus v m, now what I want is not just this 1, but v p minus v m that is v

p must appear with some positive gain, now we also earlier discuss the relationship between inverting non inverting amplifiers and how they are really the same circuit, but with input supplied to different places.

So, let me take the same circuit and use the non inverting version instead the circuit is the same accept that have applied the input here. Now, what we get? I know that the gain is 1 plus this resistance divided by that resistance remember for gain k, we use to have r and k minus 1 r over here, and k minus 1 r equals r. So, k equals 2. So, here I get to times v p, but what I wanted was v p, now we want to smaller voltage that is quite easy. So, what to have to do? Is not apply v p here, but apply v p by 2.

So, how do I get v p by 2 from v p easiest thing in the world. I just use the resistive divider, and I combine the operation of these 2 circuits I combine these 2 circuits now from v m to the output is an inverting amplifier from v p to here. It is a resistive divider and from the thereto there is a non inverting amplifier of gain 2. So, here get v p by 2. So, at the output I will get v p minus v m, now this is the circuit that is used very often to convert difference voltage into a single added voltage we have 2 large the voltage is v p and v m and we want to take the difference between them, you can use this circuit and you can see that the output will be exactly equal to v p minus v m. So, what is the catch here?

Now, let us assume that the opamp is ideal. So, we are not now talking about the common mode of the opamp, we know that if the opamp as a finite common mode rejection ratio or a non-zero common mode gain. The output will respond to the input common mode the input common mode here is nothing, but v p by 2 and output will respond to that in addition to giving v p minus v m. So, that is one problem. So, I let you work out the details of that please take it as an exercise consider, an opamp with a common mode gain a c m and a differential gain ad and calculate the output.

So, you will find that the common mode gain will have some effect on the output of the opamp and by reducing a c m or reducing in particular reducing a c m by a d, you will improve the behavior. So, I will not look at that I will look at something else. That can also give you a finite common mode rejection ratio or a non-zero common mode of gain, now what is that have? You see the resistor divider as well as the non-inverting amplifier both depend on the registers ratios.

That attenuation of the resistive divider as well as the gain of non-inverting amplifier, now in reality we are 4 different registers for physically different registers. So, there values will be different. So, this will be r 1 r 2, and this will be r 3 and r 4 of course, nominally all of them equal r, but in reality there will be some difference r 2 is r plus delta r 2 and. so on…

So, now, what will be the output of this circuit again? Please take it is a exercise, and calculated for yourself I am going to write down the answer here. What we get here at this point will be v p times r 2 by r 1 plus r 2 and from there to the output, we have a gain of 1 plus r 4 by r 3. So, that is the gain from v p and the gain from v m of course, these minus r 4 divided by r 3, now if r 4 by r 3 happens to be 1 and r 1 by r 2 happens to be one this will be exactly equal to v p minus v m that I am reality, we know there will be different from each other.

So, let me consider, let us say one of these ratios r 4 by r 3 this will be r plus some value, and it will be r plus some other value, now delta r 4 and delta r 3 are differences from the nominal value r, now I can write this as, all r d1 is to take r out and expanded out the ratios and I will also use the fact that delta r 4 by r and delta r 3 by r are quantities much smaller than 1. So, what I will get will be 1 plus delta r 4 minus delta r 3 by r and these that r 4 minus delta r 3 is nothing, but the mismatch between these 2 resistors and divided by r you get the normalized mismatch between that 2 resistors and this is obvious this expression depends only on the relative mismatch between pairs of registers.

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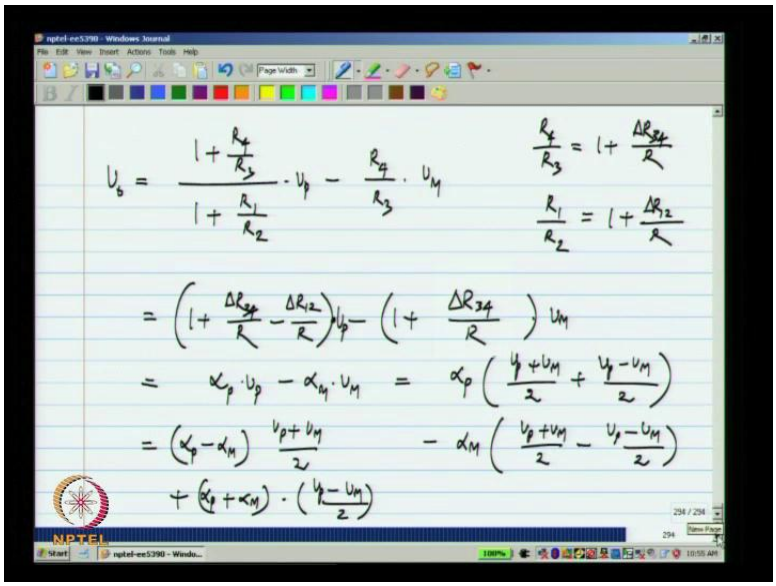

So, v out, which is 1 plus r 4 by r 3 divided by 1 plus r 1 by r 2 times v p minus r 4 by r 3 times v m. Now, r 4 by r 3 I said was 1 plus delta r 4 minus delta r 3 divided by r, similarly r 1 by r 2 will be 1 plus delta r 1 minus delta r 2 divided by r. So, here we will have 1 plus delta r 4 minus delta r 3 divided by r divided by 1 plus delta r 1 minus delta r 2 divided by r minus 1 plus delta r 4 minus delta r 3 divided by r this time v p minus this whole thing times v m. I do not want to keep on writing delta r 4 minus delta r 3. So, I will rewrite this as delta r 3 4 divided by r that the normalized mismatch between r 3 and r 4. Similarly this is delta r 1 2 divided by r. So, if I substitute that this is what I am going to get? I am going to once again use the fact that this delta are 3 4 by r and delta r 1 2 by r are quantities much smaller than 1. So, this entire thing reduces to…

So, that is what it is going to be? So, the output is of the form of some alpha p v p minus alpha m v m and alpha p is not exactly the same as alpha m, now this can be written as alpha p v p plus v m by 2 minus v p minus v m sorry plus v p minus v m divided by 2 minus alpha m v p plus v m by 2 minus v p minus v m divided by 2 have just resolved the signals into the differential and common mode components. So, which gives me alpha p minus alpha m times common mode voltage v p plus v m by 2 plus alpha p plus alpha m times v p minus v m by 2.

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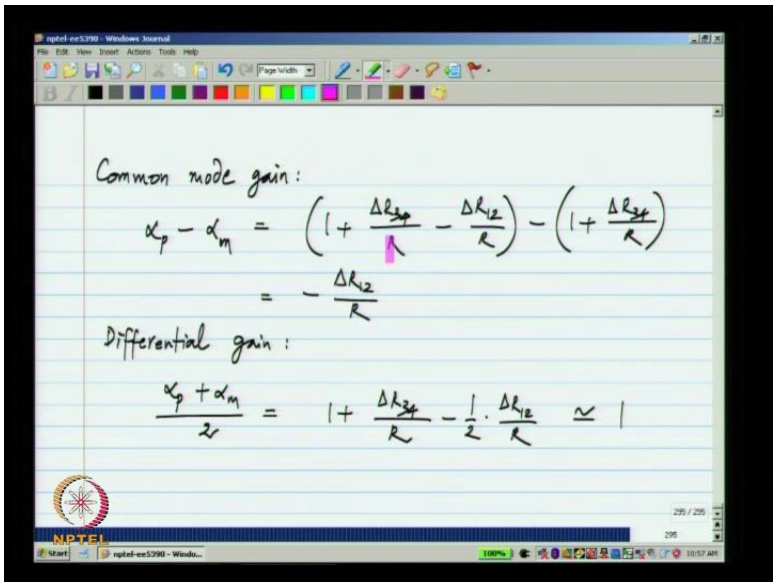

So, the common mode gain of this circuit is alpha p minus alpha m, which is equal to 1 plus delta r 3 4 by r minus delta r 1 2 by r minus alpha m, which is 1 plus delta r 3 4 divided by r. And it turns out to be simply minus delta r 1 2 divided by r, and the differential gain, which is alpha p plus alpha m divided by 2. This is the number that multiplies v p minus v m and that is equal to 1 plus delta r 3 4 by r minus 1 by 2 delta r 1 2 divided by r now. It is quite close to 1 it is different, because of the resistor mismatch, but right now we are interested in the effects of the common mode. So, we will ignore the inaccuracy in the differential gain and say that this is approximately equal to. So, the common mode rejection ratio is nothing, but 1 divided by that 1. So, we will simply work with the common mode gain. So, the circuit has a non-zero.

Common mode gain ideally it should have given an output v p minus v m in reality it gives some constant times the common mode voltage plus 1 times v p minus v m, now what is the effect of a this a common mode gain is quite small it is a relative between register 1 and 2 it is delta r 1 2 divided by r. So, what happens because of this? Now, what happens in reality is that that is we consider a case where you're trying to distinguish a small difference between 2 large voltages.

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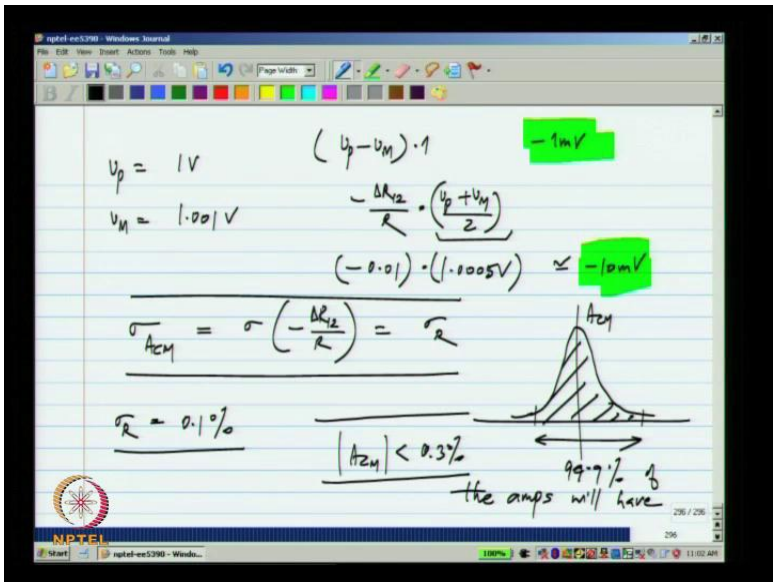

So, let us a the inputs are 1 volt and 1.001 volts. So, the output will be v p minus v m times 1. This part is minus 1 mille volt plus some resistor mismatch times v p plus v m by 2, now v p plus v m by 2 approximately 1 volts. It is 1 0. 0005volts. So, in fact, let me write that here, now how much is delta r 1 to by r. It depends on the physical size of the registers that you use.

Now, let us see that we have 1 percent mismatch, which sound small, but let see what happens. So, let say delta 1 2 by r is point 0 1 just I will take some particular number. Now, what happens here will have approximately minus ten mille volts. So, the contribution of the difference is 1 mille volt the contribution of the common mode is ten mille volts. It is much more than the difference and it is going to drown out any difference voltage that you have trying to measure, now it also turns out that this kind of circuit is used in many precision applications when let us a in thermocouple amplifier and…

So, on when you have a small voltage difference and you are trying to detect only that difference now, because of register mismatches the effect of common mode is lot more than the effect of the difference voltage and everything is completely washed out. So, the only solution the choose the registers that have a very small mismatched between them, now there are some other advance techniques the deal with this kind of circuit, which

need very good matching, but right now we will assume that we have to use this circuit as it is. So, the only way is to make the registers.

So, large that the mismatch become very small, now also 1 more thing now when we measure mismatches, we specify either the standard deviation or the variance here. I just calculated the output and it comes out to be some delta r 1 2 by r which is the amount of mismatch for a particular instance of this amplifier, what we should rather specify is the standard deviation of the common mode gain and that is nothing, but the standard deviation of delta r 1 2 by r and that is nothing, but sigma r itself which is the standard deviation of relative mismatch, now what does this mean? And let us say we make sigma r to be something better than what we had earlier.

So, let us a point one percent, now what this mean is that? The common mode gain will also had a standard deviation of point 1 percent, and if you plot the distribution of common mode gain over, let us a number of amplifiers that is a you make a million amplifiers and plot the distribution. The distribution will be Gaussian, because that is distribution of sigma this Gaussian and ninety-nine point nine percent of the amplifier will have a common mode voltage is magnitude is less than 3 sigma r or in other words point 3 percent, now whether this is good in a for not depends on the application. So, let us say we are interested in measuring a minimum difference voltage of 1 mille volt.

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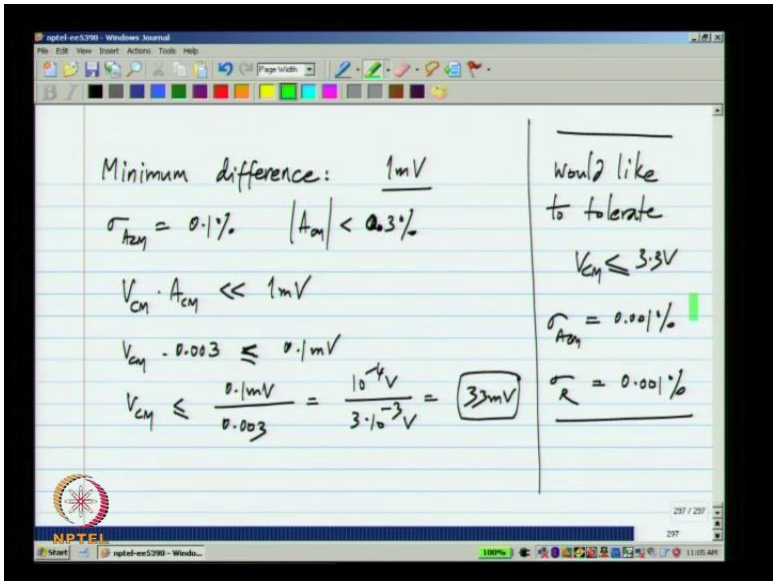

Now, let us also assume that our sigma a c m is point 1 percent so; that means, that ninety-nine percent of the amplifiers the common mode gain magnitude will be less than point 3 percent, now there is nothing secret about this ninety-nine point nine percent, we just assume that if there is only point 1 percent of the amplifiers that fall beyond this throw them away and use only the once that within this range, now are this amplifier to be usable the effect of the common mode that is v c m times a c m as to be much smaller than the smallest to different, which is 1 mille volt.

Now, a c m I will take it to be point 3 percent, which is the 3 sigma value know the gaussian distribution as any infinitely large amplitude, but will use 3 sigma as the amplitude. So, v c m times a c m, which is 0. 3 percent, which is 0.0 0 3 has to be much less than 1 mille volt. So, I will simply say it is 1 tenth of this value. So, that is 0.1 mille volt. So, is that is a less than or equal to 0.1 mille volt. So, v cm as to be less than equal to 0.1 mille volt by 0.0 0 3 and how much is that that will give you approximately 33 mille volts. So, while this amplifier ideally gives you only the difference and completely rejects the common mode with the mismatch that, we have it can only tolerate a common mode voltage of about 33 mille volts.

Now, let us say we have 2 tolerate common mode input voltage of 3.3 volts that is we would like to tolerate common mode voltages of 3.3 volts this means that the sigma a c m as to be correspondingly smaller. So, this 3.3 volts is hundred times larger than 33 mille volts. So, the sigma a c m as to be 0.0 0 1 percent or, because the sigma of the common mode gain is the same as the resistor mismatch that has to be 0.0 0 1 percent

So, if you are to be able to tolerate the very large common mode voltage the you have to use very precise the match registers. Now this is just an example circuit, where the common mode rejection as important. I so these just to put the reason for common mode rejection in context and this is a very common application that you have 2 voltages, and you take the difference, but the 2 voltages are with respect to some ground and the circuits always respond to the individual voltages or in other words that difference voltage as well as the average voltage, now in general also it turns out that the response to the common mode can be strongly influenced by the matching circuit, which ideally give you a zero common mode gain can give you in on non-zero common mode gain in presence of mismatches. So, these will see further in the following lecture. Thank you.