Analog Integrated Circuit Design
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Lecture No - 40
Fully Differential Single Stage Opamp

Hello everyone, and welcome to lecture 40 of analog integration circuit design. In the previous lecture, we look at the advantages of fully differential circuits, that is where every signal is carried and two wires. And the two wires carry equivalent opposite voltages with respect to ground. The main advantage is immediately to interference as well as that cause less interference. There are immune to both stay interference from other wires that may be passing, and also interference due to voltage drops on power supply and ground lines.

So, it like to make all the circuit that we already made fully differential, that is the opamp and the trans-conductor and so on, and that we look at in this class. Now, in the previous class we also saw how to analyze fully differential circuits, we can do that using common mode and differential mode half circuit. Now, as for as noise is concerned, if you take single noise source the circuit is not symmetric, but we can represent that as a combination of a common mode and differential noise voltages. The common mode noise is no effect and the differential noise will have some effect, and finally we found out that calculate the output noise of fully differential circuits. We can take the corresponding half circuit do its noise analyses as though that were the entire circuits and double the voltage noise spectral density.

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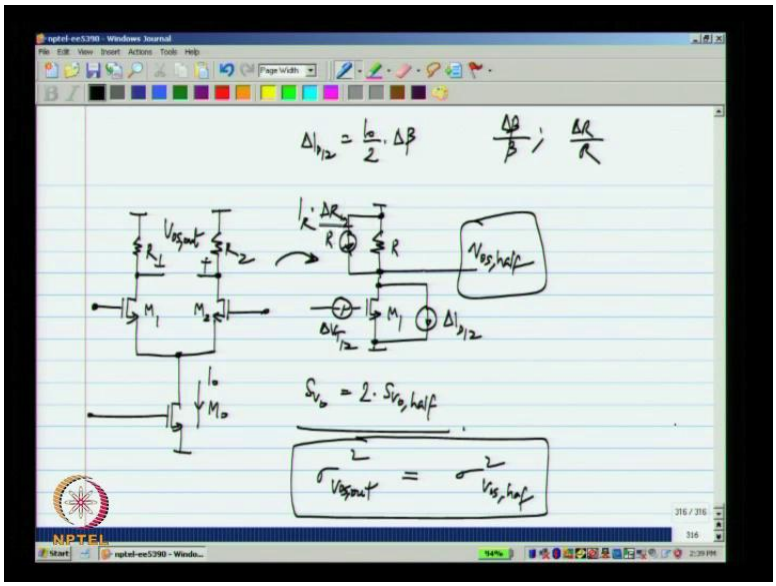

Now, will quickly look at how to calculate offset in a fully differential circuits then move on to design fully differential opamps. Now, we saw that with, we have a fully differential circuit such as the differential pair loaded by the resisters. The differential noise voltage between these 2 notes will have some spectral density S V o. Now, we take the half circuit and calculate its output noise voltage spectral density that may call it S V o half S V o will be 2 times S V o half. Now as I emphasize the noise current this register courses a certain output voltage here and there and similarly these register will cause some voltage here and there and so on.

But, the net result is that, you take the half circuit do to its on noise analysis and double the spectral density to get the output noise spectral density in a fully differential circuit's. Similarly, as for as the offset is concerned let us consider the offset here, the offset in presence of mismatches will be some dc voltage Vo s and here I am calculating it at the output it can be referred to the input by dividing by the gain. So, that is the output offset.

Now, can we calculate it that from the single ended equivalent circuit, it turns that we can first of all we simply insert the mismatch between transistor 1 and 2. That is the transistor corresponding to this single transistor in series with the gate of M1, if you have some current mismatch that can be inserted here delta I D12 mismatch in the absolute current and that is equal to I0 by 2 times delta beta. Delta beta is the mismatch in current factor between these 2, there is no threshold voltage mismatch, the current mismatch in

the between 2 transistor would be simply the quiz and current times the change in data value. Similarly, the effect of any mismatch in the register can be also represented by an equivalent current source are a voltage source.

So, the mismatch current will be equal to the quiz and current flowing in the register, which is in this case I0 by 2. Let me assume this current I0 times the mismatch in the resistance. Now, what we will be given will be delta beta by beta and delta R by R, and so on. For beta and R and so on, its specify the relative mismatch from that we can calculate delta beta and delta R and multiply that by I02. Here and there to get the equivalent current sources.

Now, how can it be it represented by an equivalent current, this comes from a simple application of substitution theorem are what is known as composition theorem. I will not go into the details, but the mismatch in every component can be their represented like this. So, finally, because all this voltages the small signal output voltage will be of some value. Let me call that V o s half it turns out that the variance of the output offset in the differential circuit exactly equals the variance of this output voltage we get in the half circuit. Now, in case of noise we get a factor of 2 in case of offset we do not get that, because this offset already represented the relative mismatch between to identical devices. It is assumed that this is delta VT 12 represent the mismatch between M1 and M2. Similarly, delta l D 1 2 represents the mismatch between current factors of M1and M2.

Similarly these delta R is not just the error in the value R compared to the nominal value, but the mismatch between if liable these R 1, R 2 and R12. So, because of this we do not get the factor of half and this is the way mismatch normally specified is the process people measure a large number of pairs of identical devices, and characterize the mismatch between them. So, what you have in the process data sheet is the mismatch between 2 nominally identical devices. So, again by simply doing the half circuit analyses, we can find out the offset voltages we consider the design of opamp in some detail. The opamp add differential input under single ended output, we needed the differential input to take the error between the desire and feedback signals, but the output goes single ended with respect to some ground. Now what we would like to this move on to fully differential opamps, because we already seen the advantages of fully differential signals.

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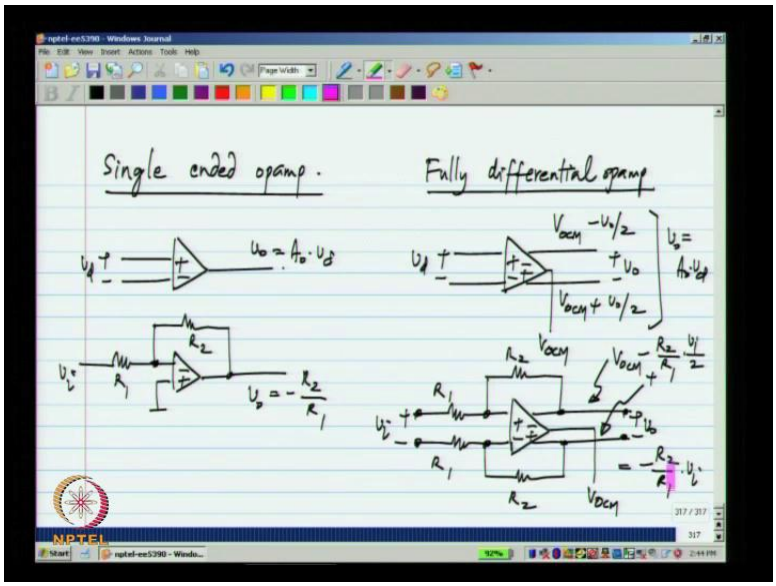

This is the single ended opamp. This is the input voltage and that is the output voltage and in the small signal region, it is some dc gain times V d. If Vd is the dc. What is the fully differential opamp. The input is the differential and the output is also differential in the differential voltage. Let me call it Vo and each of the individual voltages with respect to the ground would be some V c m plus let me call it Vo c m to denote its output common mode voltage minus Vo by 2, and this is Vo c m plus Vo by 2 and what is Vo c m is the common mode of the output. It is usually sum constant dc quantity and that will be an input to the opamp.

I will show it like this. So, you can specify the output common mode voltage of opamp the providing the corresponding voltage to the opamp, and this voltages will be internal to the opamp will say how this will used and we designed the circuit at the transistor level. Now, how do we use this opamp for example, we make an inverting amplifier like this one V o minus R2 by R1. Now, the fully differential version of this circuit would be the input is differential voltage here and the output differential output will be minus R2 by R1 times V i. I don't mention this earlier V0 in this will be A0 times V d. If V d is the d c and where it will a transfer function.

A transfer function of a opamp this is the fully differential version again you can easily analyze that by assuming that the input is the opamp are virtual shot, if the opamp behaves like an integrator are if it as very high gain than these 2 inputs will be at the

same voltage and the output will be minus R 2 by R 1 times Vi. And if you look at the individual voltage is let me assume that the output common mode voltage set to some voltages Vo c m, this will be Vo c m minus R 2 by R 1, Vi by 2 and these other side will be the same thing except to the plus sign.

So, the output will be fully differential. So, this is how make fully differential circuit also please note that once you have a fully differential circuits this minus sign loses its significance. If i measure the output voltage with upper terminal being positive and the lower being negative i get minus R 2 by R 1 times Vi if i flip the notation of V0, i will get plus R 2 by R 1 times Vi. So, simply by flipping the wires i can get either positive or negative gains. So, that is actually is simplification in the realization of differential circuit's. There are many occasion, where when you make is single ended circuit you need to realize gain of minus 1, simply to invert the polarity of the signal what as in differential case you can invert the polarity of the signal by simply crossing the wires. Now, how do we come up with fully differential circuit's for any circuit with opamps, which as 1 of the input terminals of the opamp be ground, it is very easy.

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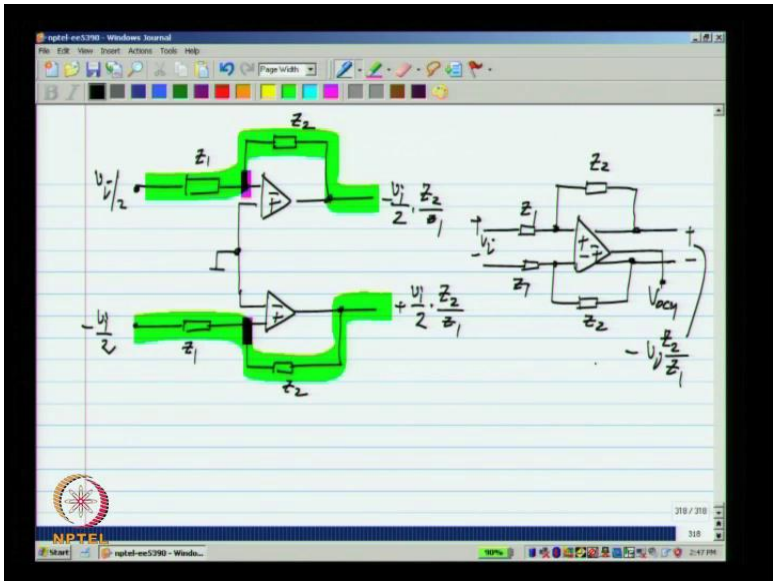

Let me just show the inverting amplifier example again, but I will show impedances just to make it look more general. So, we have this now, let me copy over and draw the same thing upside down.

Z 1 Z 2 now, these are 2 single ended circuits if i have Vi by 2. I get Vi by 2, Z 2 by Z 1 the negative of that and if i minus Vi by 2. I get this voltage at the output on this 2 voltages are connected to ground. Now, you see that there is virtual shot between this 2 terminals and these two. So, effectively the voltage and that point are the same, if the opamp are ideal. So, what we do the fully differential opamp is to essentially lift these of the ground that is ignore this part and have only this parts of the circuit. That total input voltage will be the total difference voltage, here Vi and the total output voltage will be Vi times Z 2 by Z 1.

And i will not always show this explicitly, but the output common mode voltage is set to Vo c m means that the 2 output voltages will be V o c m plus Vi times Z 2 by Z 1 by 2 and Vo c M minus Vi times Z 2 by Z 1 divided by 2 . So, this is quite easy to do for any circuit, in which the opamp as 1 terminal to ground. The opamp does not have either terminals at ground. you cannot do this, but usually we can make all the circuit that we want with circuits of this type. So, we would not worry too much about.

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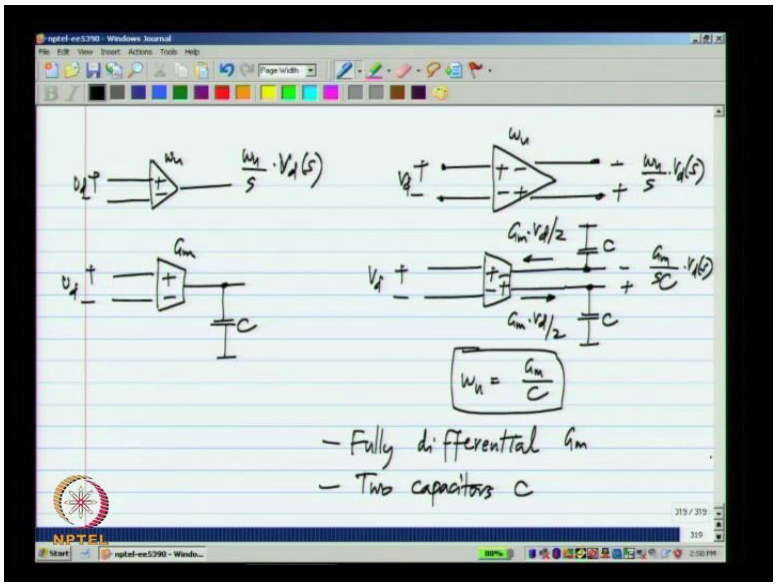

So, we would not worry too much about that now, how did we make our single ended opamp with a certain unity gain frequency omega u. we used a trans conductance are a voltage controlled current source G m and pasted its output current through a capacitor C. Now, when we want to make a fully differential opamp the principle is the same, let us say the unity gain frequency is omega u then the total output voltage will be omega u

by s, Vd of s that is what we would like ideally the opamp is an integrator what we need in this case is a fully differential trans conductor and what is the meaning of that.

if i apply voltage Vd there is a terminal at which it draws a current Gm times Vd and there is a terminal wire it pushes out the current Gm times Vd by 2. And you pass each of these currents through capacitors C then the output voltage will be Gm by C times V d of s and of course. The unity gain frequency of those opamp is Gm by C. So, first of all we need a fully differential trans conductance Gm and we need 2 capacitors and this is always the case. The physical structure, the schematic of a fully differential circuit will be symmetrical it has to be, we need two integrating capacitors C.

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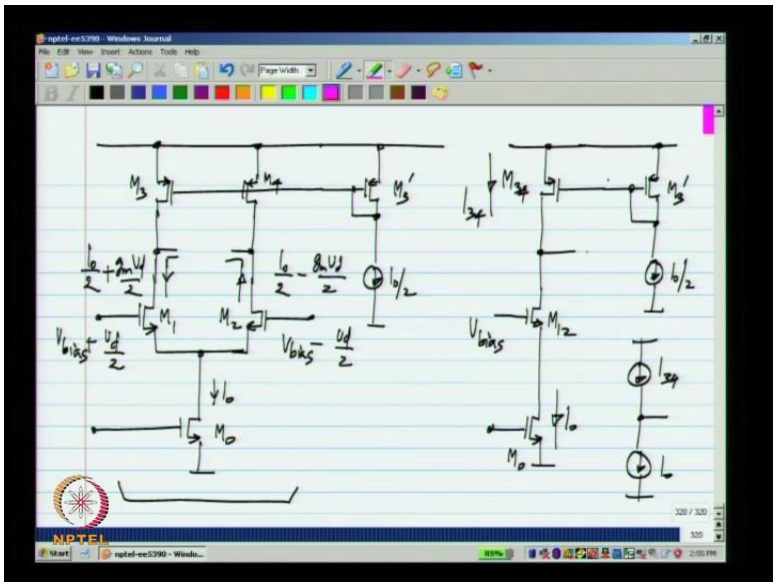

How do you realize the differential Gm. It turns out we can do it in a very similar way that we realized the single ended trans conductance, if you take a differential pair and apply a differential voltage to it, what we get are incremental current, which are equal and opposite. So, here we get total current of I0 by 2 plus G m Vd by 2 and here it is I0 by 2 minus Gm, Vd by 2. Now, this is exactly the form that we require here except that there is also the bias current I0 by 2. So, if we subtract is off the bias currents I0 by 2 from these 2 arms what we will be drawn from here, and what will be pushed in out of that note will be Gm, V d by 2. So, this is exactly circuit that we require, we need a differential pair and we need current sources I0 by 2. So, what is the difficulty now, we

can try to implement this directly, but. So, let us say, I take 2 P mos transistors and bias them with a current mirror.

Let me assume, this transistor are all identical M3 and M 4 and bias them with I02, what will happen. It is a very easy to see, when I make the common mode half circuit of this that, i take this half of the circuit and fold it over the other half. Let me assume that is there is no signal at this point. Now, clearly you see that this is like having 2 current sources that are connected together nominally this current source equals I0 that is the current in M3 and current in M4 put together, but in general it will be something else, I will call it I34 and if I34 is different from I0 either this voltage will keep on rising and till M34 goes in try out region or it will keep on falling and till M12 and M0 going to try out region.

So, these you recall it looks like having 2 kind source I34, I0 like this. We know that with ideal current source, we cannot even make this connection and less I34 happens to be exactly equal to I0 that is no way to guarantee that the total current from the upper transistors M3 and M4 equals the current from the lower transistor M0. So, if you do build this circuit, you will almost certainly find output very close to the Vdd rail, where the P mos transistors are in try out region are very close to ground rail, where then N mos transistor are in try out region. So, we cannot do this and we also know from biasing circuit that is where we bias the transistor that a given bias I0 that we will never be able to set the 2 currents sources independently and have their values to be equal to each other.

Now, the only way to do it is by setting 1 of them using negative feedback for instance we can adjust the gate voltages of M3 and M4 such that there total current output equals the current of M0 and we have to do this with negative feedback. So, let us see how to that, what happens is if the total current in M3 and M4 is larger than current from M0 these voltages will keep on rising. Now if the total current is smaller this voltage will keep on falling. what I want is for the sum of this 2 voltages to be sum constant such that the all the transistor M1, M2,M3and M4 are in such saturation region.

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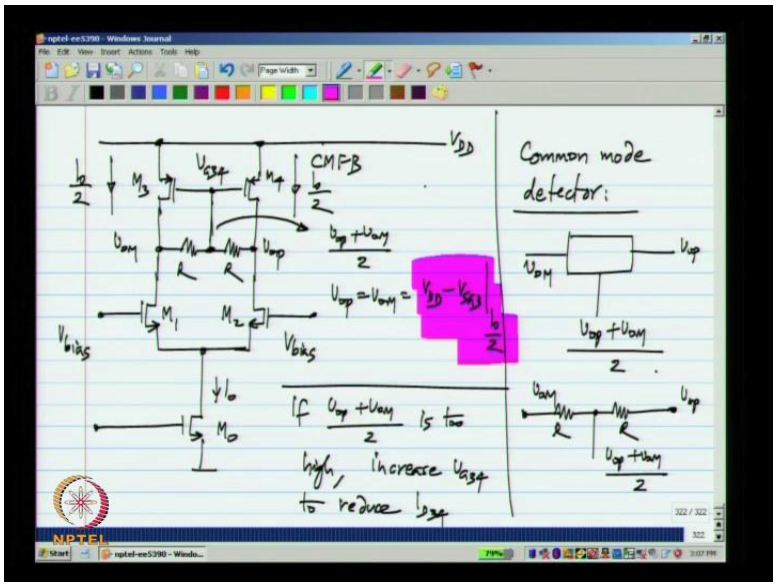

So, let me call this Vo p and Vo m we cannot using this kind of biasing this has to come from feedback which is usually call the common mode feedback or CMFB. Now what should this feedback be based on we should based on the average value of Vo p and Vom. We do not want to react to Vo p and Vo m individually like that said we need an opamp and opamp output must be able to vary, which not that the opamp output voltage must be fixed then the opamp is completely useless, what we want is that the average of the 2 output voltages V equal to constant Vo c m. These 2 voltages have an average or common mode value equals Vo c m. So, what should I do in negative feedback as usual I have to compares the actual value with desired value and adjust the actual value and till it becomes equal to the desired value.

Now, here what is the actual value that is the output common mode voltage of the opamp. I need detect the output common mode voltage, lets me call this the common mode detector. So, it output voltage will be nothing but Vo p plus Vo m divided by 2 than I have to compare it with the desire output common mode voltage Voc m and feed it back to the gate M3 and M4 in the right direction means that the output common mode is too high, what should happen is that what; that means, is that the current in M3 and M4 are lower than the current from M0. So, than the current in M3 and M4 must decrease, similarly, if the output common mode voltages are very high; that means, that the current in M3 and M4 is more than the current from M0. So, the current in M3 and M4 must decrease. So, when the current in M3 and M4 decreases V o m and V o p will be pulled

down. Similarly, when this output voltages is too low, the current in M3 and M4 must increase. So, that the output voltages increase.

So, you will see that to decrease the value of currents in M 3 and M 4, we need to increase the output voltages. So, if the voltages very high, the common mode feedback voltage must be increased, if the output common mode very low, the common mode feedback voltage must all so be decreased. So, the polarity of the opamp used in the common mode feedback is V1 by this, we can also determine science by breaking the loop, and making sure that what comes negative and so on. Whatever I described is just that what in different words. So, this is the general common mode feedback circuit we need to have a common mode detector. So, that you detect the actual output common mode voltage, you compare it with the desire common mode voltage Vo c m and you control one of the current sources with it in fully differential circuit. You will always have scenarios.

Where, we have some current source coming from the top and something coming from the bottom and the two have to be made exactly equal the way to do that is to control one of them using negative feedback. Now we will see how to implement this negative feedback, there is wide variety of common mode detectors as well as ways to close the feedback loop. First of all, let us consider common mode detector, we want to take in V o m and V o p and obtain an output V o p plus V o m divided by 2. How can we this the simplest way of getting the coverage of 2 voltages is to use a resistive divider V o p and V o m. So, will get V o p plus V o m by 2, if this two registers are equal. So, that is potential candidates for the common mode detector.

So, let us use that here we will see what the implication of this is later, let me label these voltages Vg34 and next thing is how to close the feedback loop. As I said the director common mode voltage Vo p plus Vo m by 2 is too high; that means, that the current M3 and M4 is too high and we have to go on increasing the value of Vg34.

So, that the current in M 3 and M4 goes on reducing and the output common voltage reaches the desired value. Similarly, if the detector common mode voltage is too low, they have to continuously reduce the value of Vg34. So, that the current M3 and M4 will increase and the output common mode voltages reaches the desired value and vice versa. Now, there are many ways of completing the loop, we can use an integrator or an opamp

between this point and that point. So, that we get the feedback action that I just described. But, the most simple realization of this is to observe that, if V o p plus V o m too high, Vg34 also must increase that is it must go in the same direction as Vo p plus Vo m by 2.Similarly, the incremental gain required from this point to that point is positive. So, as you can see here, if this voltages detector common mode is too high, the common mode feedback also must be high. Similarly, if this is too low, the common mode feedback also must be low.

In the simplest way to arrange that is to connect to together. Now, if you recall, how you derived the direct connector transistor, where the transistor biased constant current we detect that current differential, the drain and fad it back to the gate, where many ways of feeding it back, but the simplest realization was tie the gate to the drain. Now, this is similar, but in this case it is not a single transistor we detect the common mode voltage of two transistor and connected directly to gate to the two transistor. Now, we can analyze what happens, first of all let us assume that there is no differential input that this voltage have to be equal to each other vice symmetric. So, no current flows through R and this voltage equals the output voltage V o p plus V o m by 2.

Now, when the feedback circuit is settled the current as to be I0 by 2 and the current in this is also I0 by 2, and also the gate voltages of these equals the voltages of drains of M3 and M4. So, the output voltages will be equal to V d d minus Vs G of M3 or Vs G M4 at a current of I0 by 2. It has to be equal to this is, if this voltages higher than that; that means, that the current here is too low and the voltage is Vo p and Vo m and pull down. If this voltage is lower than what I mention here then current in M3 and M4 is higher than I0 by 2 and this voltage will be pulled up.

So, in this case the output common mode voltage will get stabilized to this particular value. Now, in this is nothing but the out common mode voltage V o c m. In this particular circuit we dint provide a V o c m from outside it is built into the constant of mos transistor. So, once you have the threshold voltage and the current factor and the current values you can calculate the output common mode voltage.

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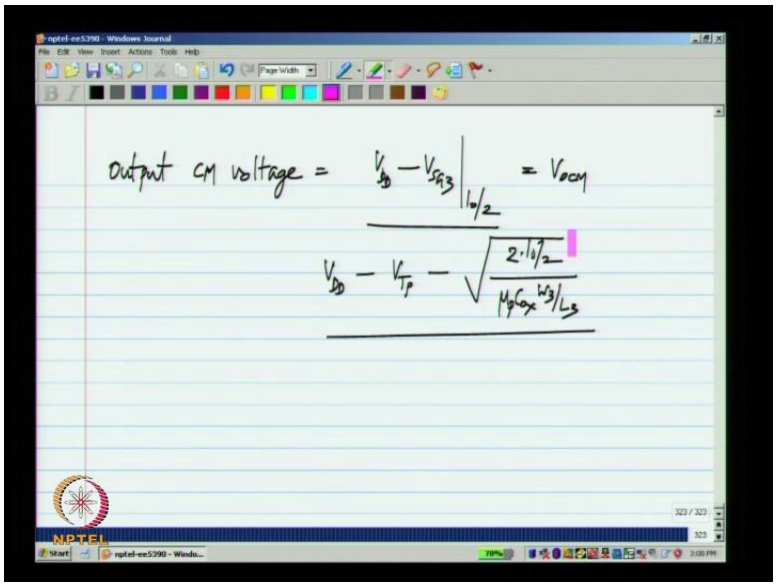

This is Vo c m. Now, we do not have freedom in setting the Vo c m arbitrarily it depends on the threshold voltage and the parameters of most, because Vs G 3 is nothing but the threshold voltage of the p mos transistors minus square root of 2 times I0 divided by Mu p Cox of w 3 by L3. Now, by choosing that dimensional of transistor, you can play around a little bit with the output common mode voltage, but you do not have too much freedom to do so, but in many cases this circuit words perfectly well.

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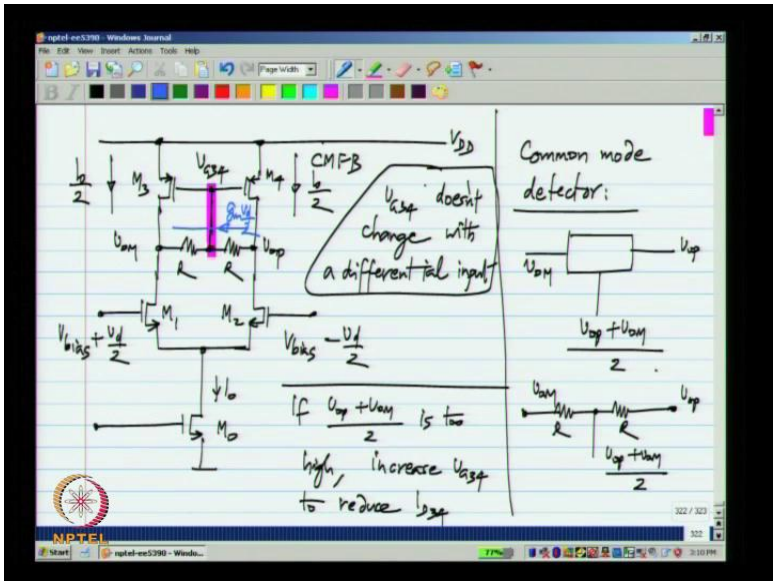

Now, what happens if you applied a differential input. Let us, I have plus Vd by 2 and minus Vd by 2 here, what happens in that case is that there will be an incremental voltage V o p and an equivalent opposite incremental voltage in V o m. Now, because the voltage at this node is the average the 2 voltages and the increments are equal and opposite the voltage Vg 3 4 does not change at all, if you have a fully differential input. So, what it means that M3 and M4 will continued is apply the same current as before and the differential current.

The extra current that is drawn from M1 and the extra negative current that is drawn from M2 will flow through R. So, there will be a current g mVd by2 in that direction. So, the upper transistor M3 and M4 behave like constant current sources and because of negative feedback there some is adjusted to be exactly equal to the value of the tile current source I0.And we need the negative feedback, because there will be no other way to adjust their values to be exactly equal to the tile current source.

So, a fully differential opamp needs common mode feedback and another way to think about it is that we really have two output voltage in a fully differential opamp the positive and negative output voltage and we need to feedback loop to fix the individual voltages. Now as usual it is better to think of differential and common mode voltages instead of individual voltages because what we desire is that differential voltage and what we want to suppress or we want to volt constant is the common mode voltage.

So, this kind of an opamp any, which why you think about it needs to independent feedback loops, now we do not think of it as a to independent feedback loops controlling each output voltage, we think of it is one feedback loop controlling the differential output voltage this is the feedback loop that controls the functionality. So if you look at this particular circuit in the single ended case the feedback loop found by the impedance is z 1 and z 2 control the output voltage. Similarly, here the feedback loop found by z 1 and z 2 control the differential output voltage.

Now, we need another feedback loop and that feedback loop operates only on the common mode output, and it helps at the common mode output voltage. Now, what is the effect of the common mode feedback on the differential circuit, we added some components here and we have to investigate what it is effect is, let me redraw this circuit.

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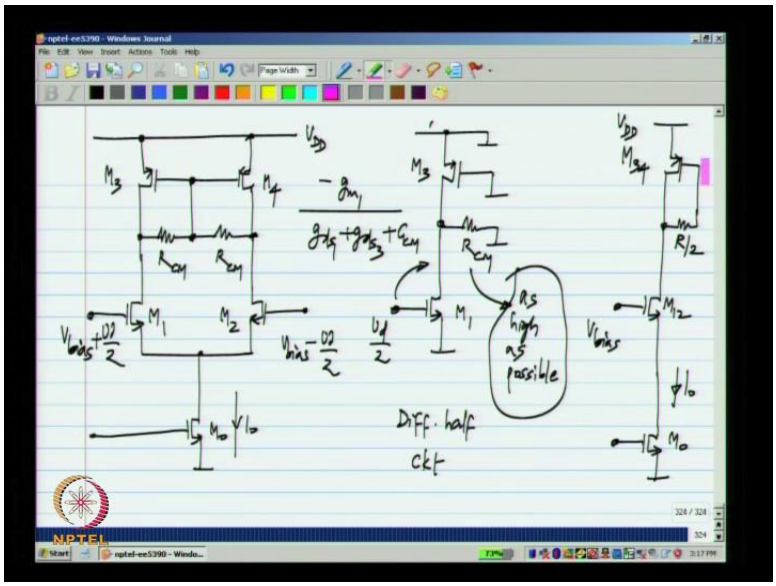

This is my fully differential of opamp or the simplest realization of the fully differential opamp and the differential half circuit is given by only one half of it by grounding all the nodes along the line of symmetry. This is the differential half circuit and the common mode half circuit is obtained by folding the two half together, which gives me M34 and R by 2 and M12 and M0 and here, we just have Vbias. This is the small signal ground that is Vdd. Now, first of all in the differential of circuit what we wanted was only this M 1, which is the trans conductance and M3, which is the load conductance or the load current source. Now, we see that we also have an extra element, which is R what is the effect of that it is very easy to see the R here, appears in parallel with the g d s of M3 and g d s of M1.

So, the voltage gain from this point to that point will be the gm of transistor M1 divided by g d s 1 plus g d s 3 plus this conductance g, just to make it explicit that we put it there for common mode feedback, let me rename that R cm and the reciprocal of that is G c m, and you can see that this G c m reducers the d c gain of the opamp.

Normally, viewed have got g m1 by g d s plus g d s 3 normally which by the way is exactly the same gain that we get for a single ended single stage opamp. Now, one thing, you also notice is that the analysis of dc gain in this case, the fully differential opamp is a lot easier than what we had to do for the single ended opamp. This is because the half

circuit concept a makes it very simple to analyze, we have only to transistors here with the resistor and by inspection we can write down the expression for the gain.

Now, this common mode deducting resistor R c m used the common mode detector, hence up reducing the gain. So, you have to use as high a value has possible you have to make this to be has high has possible and just for completeness let us also look at the common mode half circuit shown on the right side. Now, you see that this M3 direct connected with a resistance R by 2 in the feedback loop, because the gates do not carry any dc it makes no difference at all to the dc picture.

So, this makes the connection of this type of common mode feedback circuitry to diode connection very explicit. Now, in this case in the common mode picture you see that you have a current source I0, which is pumping the current into a diode connect transistor M34. So, the current in the M34 will be set to a value equal to I0, its quite obvious. If you did not have this feedback loop, the current in M34 could be different from I0 and this voltage would either rise or fall. But now, it will be set to a value equal to Vdd minus V sd of M34. Now, this brings us to another way of thinking about common mode feedback circuit. I just now, said that we need to stabilize the output common mode voltage as well

Now, this is like having to stabilize two output voltages quite instead of stabilizing the two output voltage separately. We stabilize the differential output using the differential feedback loop, which determines the function of the circuit, and we set the output common mode voltage to a constant value using the common mode feedback circuit.

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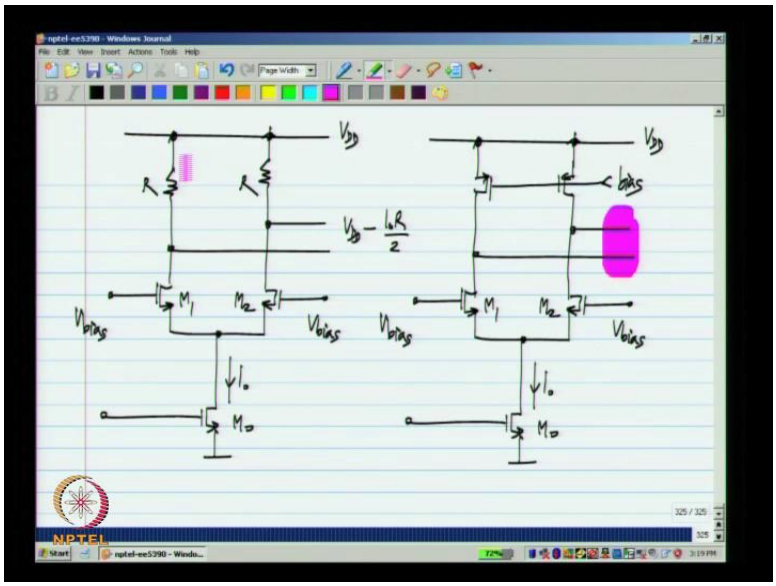

Now, another way to think of the common mode feedback circuit is as follows first of all, when we had only a differential pair with the resistive load. Now, what happens is that the output common mode voltage gets set to Vdd minus I0 R by 2. Where this is the current I0 now, there is no problem at all setting the output common mode voltage. It gets set to be Vdd minus I0 R by 2. Whereas, if you replace the resistance by current sources is some wires here, will not be able to tell what the output common mode voltage is, what is a voltage here will not be able to tell, because small differences in the current in the upper transistor and the current in the lower transistor I0 will cause this voltages to go up or down severely. This is because as long as the load resistance is rather small the output common mode voltage will be set very accurately whereas, if the impedance of the load becomes very high as in a current source there is a lot of uncertainty, because the small difference in current going into a large impedance can give you a large change in the output voltage.

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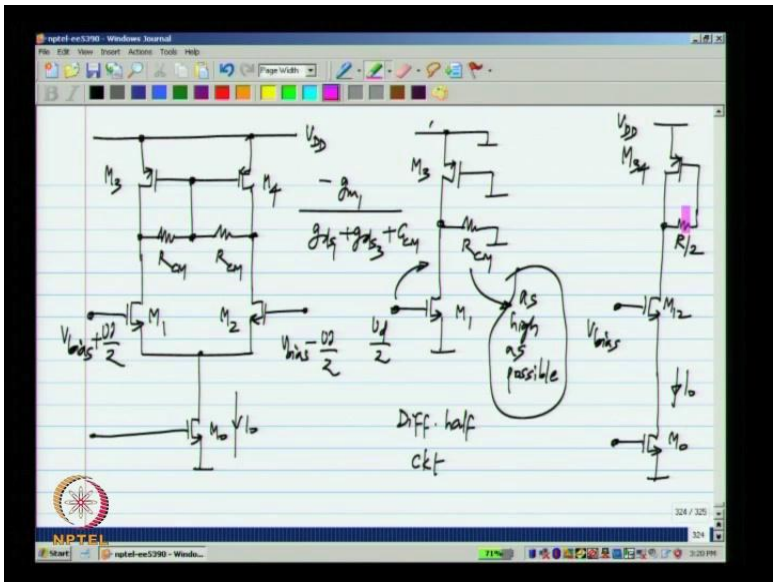

So, in a way what the common mode feedback circuit is doing is a shown in the figure on the right, it basically presents a small a impedance in the common mode. In the common mode, the transistor M34 is diode connected whereas, in the differential mode you see that the gate of M3 is grounded. So, there is no feedback at all in the differential mode around M3. So, the goal of the common mode feedback circuitry can also be thought of as providing a load resistance, which is very low for a common mode and very high for differential mode ideally the common mode feedback circuit should not affect the differential mode circuit at all, but in reality it does to some extent as we see here, it presents the load resistance R.

In the next lecture, what will do is look at different kinds of common mode feedback detectors and look at some choices, which will not affect the differential picture and consequently will not affect the differential gain. In summary, we need to have an extra feedback loop in fully differential circuits that is to stabilize the output common mode voltage.

Now, in order to do this we need to be able to deduct the output common mode voltage and feed it back to some current source in general in any high gain circuit. There is a current source on the bottom driven by the signal perhaps, and there is a current source on the top by perhaps providing a constant current, this is invariably the case you go back to any of the opamp.

Circuits we have studied. So, far you will find that this is the case now; a need for the current source is obvious they give you a very high incremental output resistance and consequently will give you very high gain. Now, very high gain also implies that output voltage is very sensitive to small changes in current that is the definition of the gain. In fact So, if you do not match the upper and lower current sources accurately the output common mode voltage will not be stabilized accurately. So, you have two stabilize one of the current sources using negative feedback.

We cannot have two current sources in open loop one on top of another to do this we detect the common mode voltage compare it to the desired common mode voltage, and feed it back to the common mode current source. The simplest realization we did not do the comparison explicitly, we simply feed it back directly. So, the output common mode voltage will not be something that we set, but it is related to the properties of the transistor, but none the less that is how common mode feedback in general words.

Now, the common mode feedback circuit provides a very low impedance in common mode and very high impedance in differential mode. In the differential mode there should be no feedback at all if the common mode feedback circuit is designed properly. In our case the common mode feedback circuitry is affecting the differential picture because the common mode detector is made using resistors. In the next lecture will see how to make common mode detector which will not affect differential picture.

Thank you.