

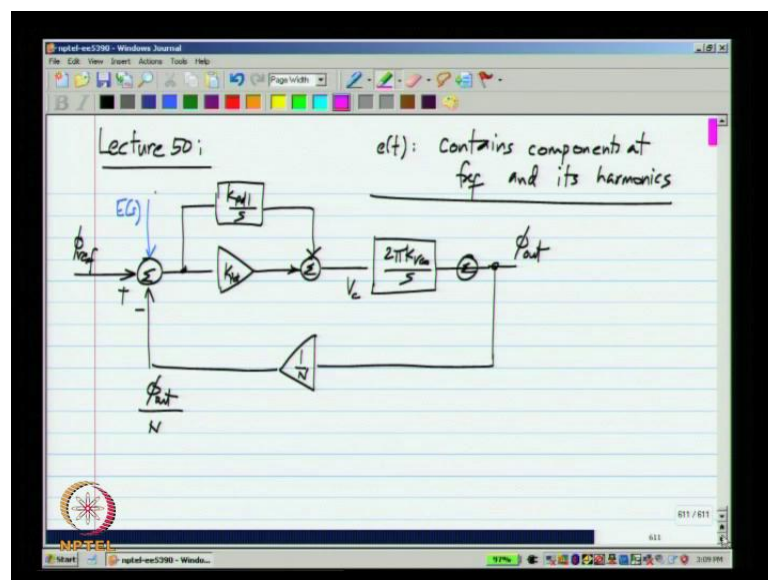
**Analog Integrated Circuit Design**  
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**Lecture - 50**  
**Type II PLL- Extra Poles; Random noise in the PLL**

Hello and welcome to lecture 50 of Analog Integrated Circuit Design, in the previous lecture we discuss the issue of reference be through in a time two PLL. We concluded that it will be much smaller than, in a type I PLL, because the width of the periodic error pulses is related to the reset delay and miss match between the a charge from current sources.

Now, both of these are rather small that is the reset delay will be much smaller than a period and the mismatch will be much smaller than, the nominal value of the charge from current. So, the rethrough component here in the type II PLL can be expected to be very small, but still they are present. And in many cases we will need to further attenuate them, so that put spectrum is sufficiently pure; in this lecture, we will discuss the way of modifying the PLL, so that we can further attenuate the reference be true.

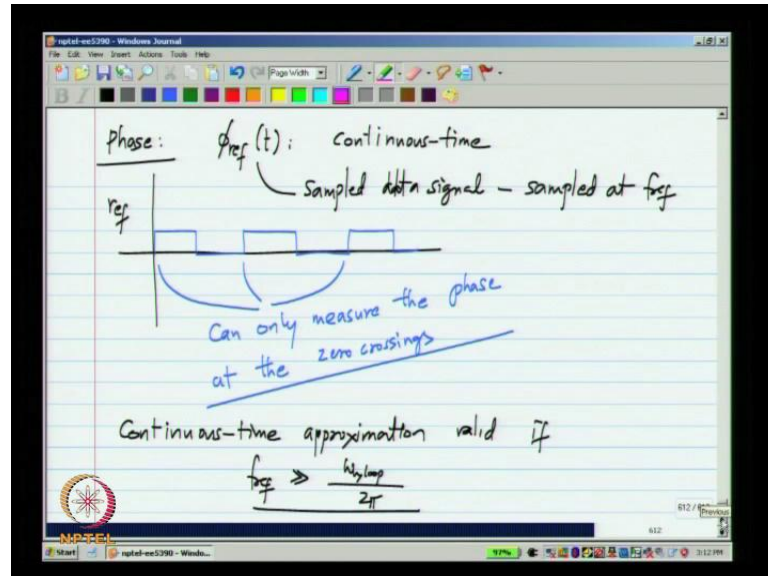
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This is the model of type II PLL and this E of s represents the periodic error of the phase deductor. Now, we know that this E of s or E of  $j 2 \pi f$  periodic error contains

components, at  $f_{ref}$  and its harmonics, now we have not yet discussed what the relationship of  $f_{ref}$  is to the bandwidth.

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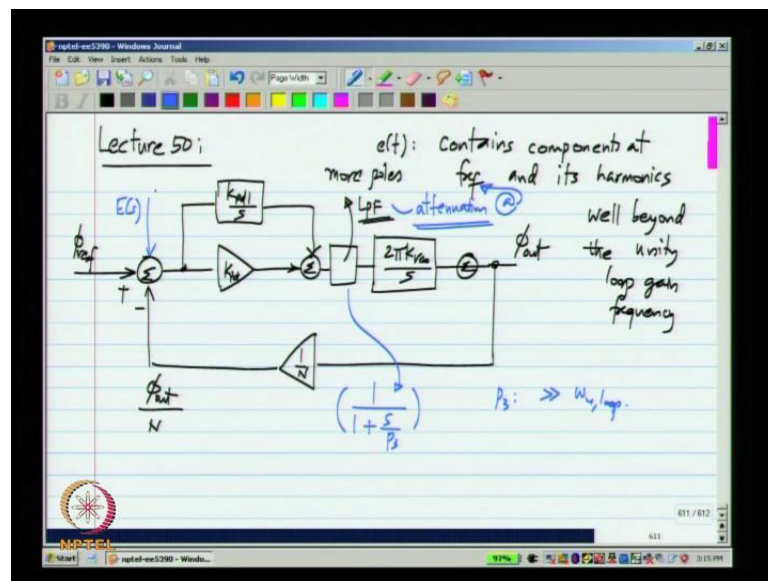
Now, it turns out that the phase let us say we take  $\pi$  ref, we have been talking as though this is the continuous quantity that is  $\pi$  ref of  $t$  is defined over continuous time. But, we also know that the reference phase signal is like this, we can only measure the phase at the zero crossings. So, this  $\pi$  ref of  $t$  is actually sample data signal and it is sampled at  $f_{ref}$  similarly, the phase of every periodic signal is sampled at its known frequency.

So, the actual phase lock loop is rather complicated and that it has, the input phase sampled that  $f_{ref}$ , the output phase sampled at  $n$  times  $f_{ref}$  and there is a rate conversion in the frequency divider. And also there are truly continuous time quantities, like the control voltage of the VCO, because the voltage across the capacitors and resistor which form the loop filter is continuous; now it is possible to analyze the phase lock loop by including all these satellites, but it is rather complicated.

And also it turns out that if, the loop bandwidth that is the unity loop gain frequency is much smaller than, the reference frequency. We can use the continuous times approximation for all these signals without making significant errors. And it turns that that is also a reasonable case in practice; in practice we can make a lot phase clock loop with this condition and they work very well.

So, we will operate under the assumption that the reference frequency is much more than, the unity gain frequency of the loop, unity loop gain frequency and we will continue to use, the continuous time approximation. So, the main point here is that the reference frequency, will always be much greater than the unity loop gain frequency, in a phase lock loop. In practice this reference frequency will be at least 10 times, the unity loop gain frequency and frequently a lot more than that, so we are well within the valid range of this approximation.

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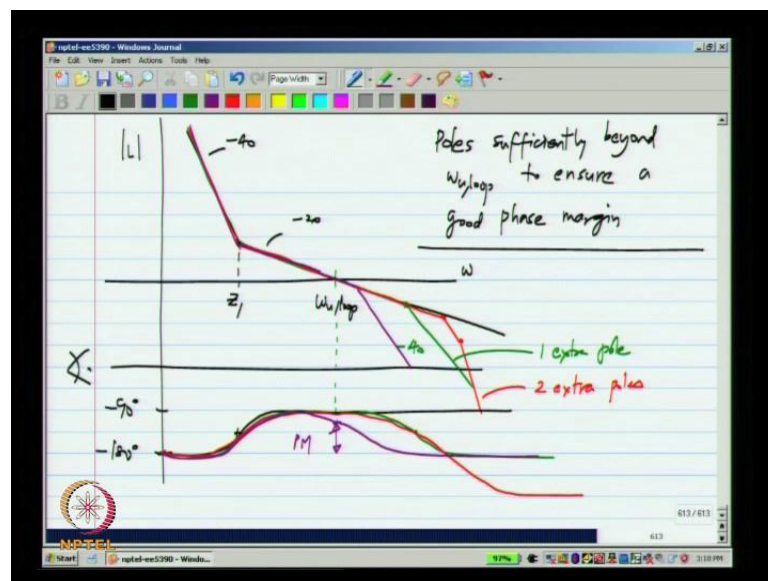
Now, what it means for the reference feed through is that, the reference feed through components are definite find its harmonics and they are at frequencies well beyond the unity loop gain frequency. Now, we have seen repeatedly that at frequencies well beyond the unity loop gain frequency, if you evaluate a transfer function let say between  $E$  of  $s$  and  $\phi$  out. What matters is only the powered path, the feedback is negligible beyond the unity loop gain frequency and it does not matter at all.

So, all we have is a for the transfer function from  $E$  of  $s$   $\phi$  out is this power path, now if we want to reduce the strength of the reference be true. What we have to do is manipulate, the transfer function of this forward path and at the frequencies of the reference through which is the  $f_{ref}$  in his harmonics. So, the solution turns out to be very simple all we have to do is to add an extra filtering step here.

For instance it could consist of 1 pole, but in general also it could be even more than one pole, so we can introduce more poles that means, this is a low pass filter and this introduce significant attenuation at  $f_{ref}$  and it is harmonics that is the idea. So, now, this attenuation will further reduce the component of  $f_{ref}$ , before it changes the value of  $\pi$  out, so we will have a smaller reference  $p$  through and smaller values of references spur.

So, for instant what can it done is let us say we have a single extra pole, this charge pump function could be form,  $1 + s \text{ by } P_3$ , where  $P_3$  is at a frequency much greater than  $\omega_{u \text{ loop}}$ . Now, keep in mind that if you introduce poles within the unity loop gain frequency you will have a serious problem with instability, but if introduce poles well beyond the unity loop gain frequency it is possible to keep the system stable, but introduce attenuation at higher frequencies.

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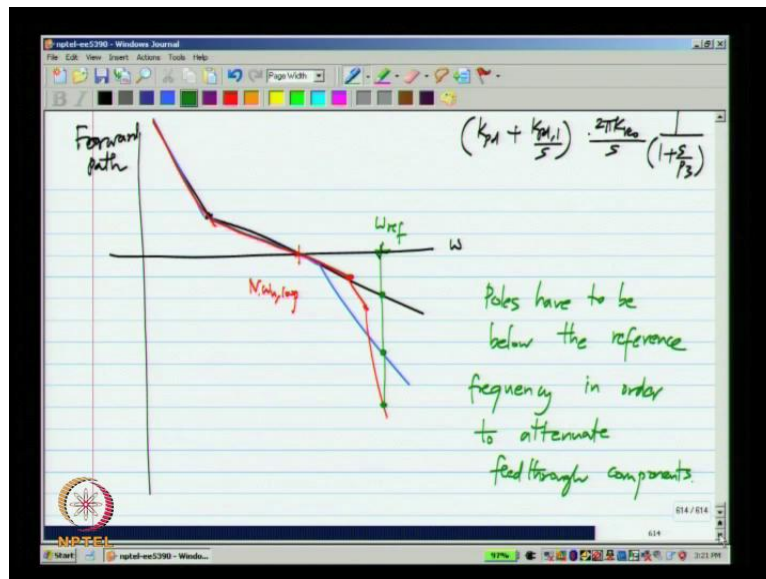
So, what happens now, the loop gain magnitude would have done this in the type II PLL that we know, it starts with the slope of minus 40 db per decade and at the frequency of the 0, it changes to minus 20. And the phase it starts from minus 180 reaches minus 135 and stays at minus 90, this is the angle of the loop gain. Now, if we introduce another pole beyond the unity loop gain frequency, this is the unity loop gain frequency.

Let say, we introduce an extra pole than this is what will happen, the slope of gain changes to minus 40; and also the phase will do that and go up the minus 180. And similarly, if we introduce 2 extra poles it could do that as well we will have something

like this and something that is what 2 extra pole and so on. Now, the closer this poles come to the unity loop gain frequency, the greater they will affect the phase margin; but we can certainly find the locations of this poles, such that we still have a healthy phase margin.

For instance if the single pole, the single extra pole happen to be over there what happens is the phase will do that and do that. So, you can see that the phase margin is now reduced, so this is the phase margin, so we have to make sure that the poles are sufficiently beyond, the unity loop gain frequency to ensure a good phase margin. Or rather hands, what happens to the attenuation of the reference p through.

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We know that the forward path gain, the gain of the forward path is  $k_p d + k_p d I$  by  $s$ ,  $2 \pi k_v c o$  by  $s$  times, we have extra poles it will also come in to picture. So, normally it would just be like that is without the extra pole and with the extra pole something like that and so on. And with 2 extra poles you could have, so this is just the gain of the power path and this frequency will be at  $n$  times  $\omega_u$  loop. These poles have to be beyond  $\omega_u$  loop not necessarily  $n$  times  $\omega_u$  loop although this diagrams shows it like that.

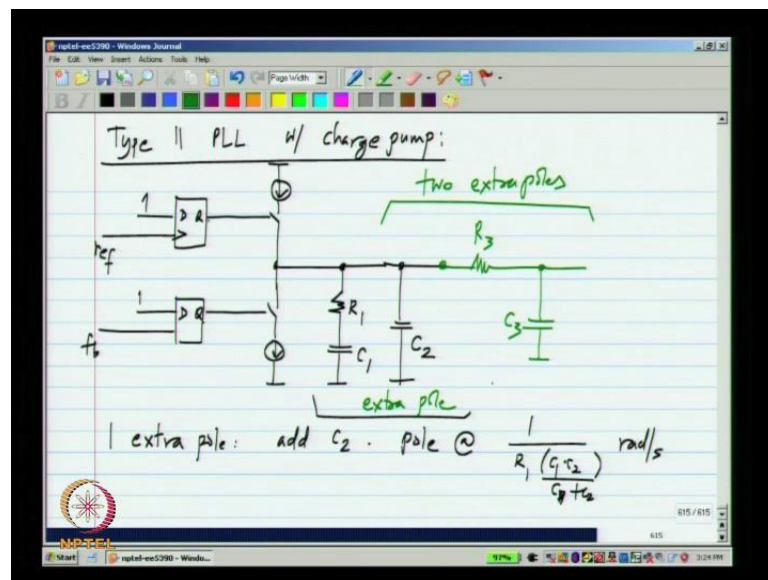
Now, let say you are reference frequency is here this is  $\omega_{ref}$  with the original PLL you have this much attenuation, with the single extra pole you have that much and two extra poles we have that much and so on. So, with greater number of poles you can

potentially have higher attenuation. But, also with the higher numbers of poles what happens is you have to place the poles further away from the unity loop gain frequency.

So, you may or may not get additional attenuation when you introduce extra poles. So, that is something that you have to evaluate and it depends on the proportion between different quantities like, the reference frequency and the bandwidth or the unity loop gain frequency and so on. And also the attenuation that you would like to have, so but general in you could introduce more poles in the have to be sufficiently beyond the unity loop gain frequency.

So, that the phase margin is maintained, so that you do not have too much ringing in the settlings of the PLL. And you also you should place the poles at a sufficiently low frequency, that you have significant attenuation at  $f_{ref}$  and its harmonics; of course, the largest components will be at  $f_{ref}$  and it is a lowest frequency. So, the poles that you place have to be below the reference frequency also otherwise, you will not get any attenuation from that. Now, in general it is a usually possible to finds the switch port for 1 or 2 extra pole, so that the reference p through is attenuated.

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Now, how do we implement this in practice we have the type II PLL with the charge pump from lets again take this one and, now this is the loop filter and to have 1 extra pole all we have to do, is to introduce the capacitor here this output here is the current. So,

putting an extra capacitor will introduce a pole and that pole frequency happens to be this, will introduce the pole at  $\frac{1}{r_1 C_1 + C_2} \text{ by } C_1 + C_2$  radians per second.

If you want a get another extra pole you could do this, so this is possible and here we get two extra poles and with this we get extra pole and so on. So, it possible to add all of these things and the loop gain will become, more complicated it will be a higher order, but this poles will be necessarily at frequencies beyond the unity loop gain frequency. So, hopefully they want change the behavior too much, but of course, you have to put these things in a simulator and a analyze it and see.

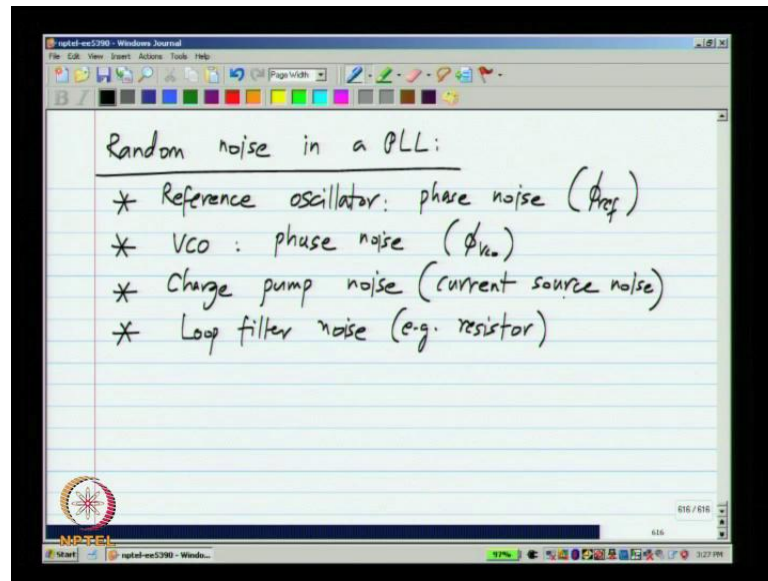
So, that is reference p through can be further attenuated if necessary there is not much point putting like, too many more poles. Because, than each of them has to be such a frequency that they do not introduce significant attenuation at the reference frequency also this is not the only way to realize the loop filter, this is I said very popular way of realizing the phase lock loop, this charge pump is easy to realize.

It also has some advantage with respect to noise that I will outline later and the loop filter also is a passive filter and again easy to realize. But, people have made phase lock loops with active loop filters and so on, one of the main concern there is the extra noise added by the active components, but it is possible. So, you can go through the literature and look for other topologies of loops filter, I said this is the most popular.

Now, the next issue that we will discuss is random noise that is the effect of random noise from, different sources on the output phase of the PLL. As, we now any output phase deviation that is not 0 means that the output signal is not exactly periodic and most of the time, we can think of it as a periodic signal with some extra component either in the time domain or the frequency domain, in the time domain has deter and in the frequency domain as phase noise. So, effectively what will be evaluating will be either the jitter or the phase noise due to different sources of noise in the PLL. Now, we have consider one kind of noise or a periodic disturbances, which is the reference p through no we will look at sources of random noise.



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Now, the random noise can be due to many different sources first of all the reference which will also be an oscillator. The reference oscillator on any reference source will have some phase noise that means, that  $\phi_{ref}$  will have some random component and the VCO will have some phase noise, that is will have some  $\phi_{vco}$  which is not 0, added by the VCO and we will have the noise from the charge pump, we know that the charge pump consist of current sources  $I_{cp}$ .

So, basically each current source will have some noise and they will get converted to, phase noise of the output and also loop the filter will have noise, for instance our loop filter has a resistor. If you have active loop filter you can have more noise and this will create voltage noise or a current noise and as you wish to model it and it will get converted to phase noise.

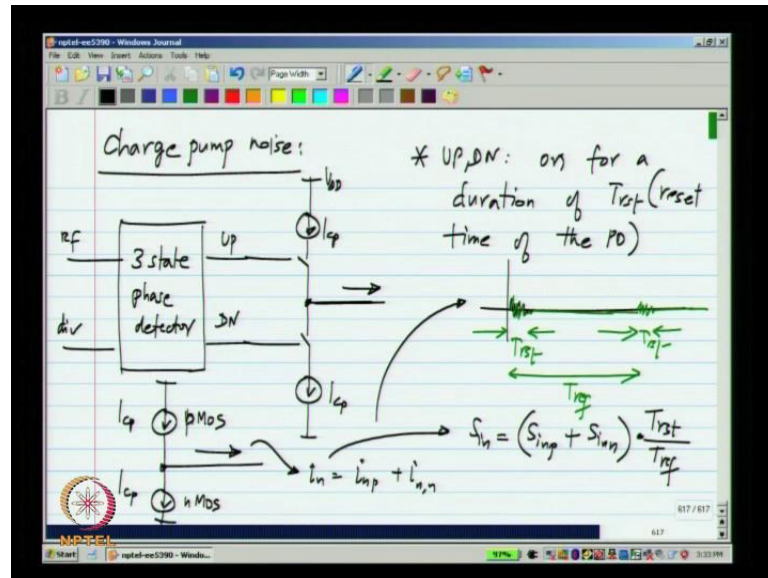
Now, what we will look at first is the charge pump noise and the loop filter noise, they were easy to deal with then we will look at the phase noise, from either the reference or the VCO for that first. We have to find out what a reasonable model for a phase noise of oscillator is, that is a complicated topic in itself and we will certainly deal with that in detail here we will not look at exactly how much, the phase noise is for a given oscillator.

We will only try to figure out the general nature of phase noise which is true for any oscillator, there can be some deviations from that, but this is generally true and then use



that as the model and then you can go through, the literature for different ways of calculating the V C O of the phase noise and also more importantly modeling it and simulating it in a simulator.

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Now, what does the charge consist of it consist of two current sources given by these up and down pulses, sometimes you also called some q and q b and effectively. The output is the current let me draw the complete p of d, I want show the topology at the briefly top level, but we know how to make the pre steady phase deductor and for the purposes of modeling, whatever current noise comes out.

I would like to refer it to the input of the phase detector this is because, I already calculated the transfer function from the input of the phase detector to the output, I know what pi out by pi ref is. So, if I refer these noise to the input over here which by the way common with the error the noise is represented, then I can use the transfer function I already evaluated.

Now, we will make some simplifying assumptions here we know that the there will be some reset duration and this is up and down switches, will be on for that reset duration there will be on for a little bit extra period. Because, the phase offset, but I will ignore for that now and I will say that up and shown or on for a duration of  $t_{rst}$  which is the reset time, of the phase detector.

Now, what does it mean during this time basically have a very simple equivalent circuits I have both the current sources, which by the way are physically different current sources this is p mos current source, which is pushing current out and I will have a n mos current source at the bottom which is pulling current in, the output current normally may be 0, if the two currents are identical.

But, the noise will not be 0, the noise will be simply the sum of these two noises you can say, it is  $I_{n,p}$  minus  $I_{n,n}$ . But, because they are uncorrelated we can think of it as the sum, so this means that what we have is some noise. If I look at it in the time domain it looks like this, there will be some random noise, but it is not continuously on because, when up and down are both 0 these switches will be off and there will be no noise at the output.

So, I will have something other this sort for a duration of  $t_{rs}$  and there will be nothing for the remaining period. The period of the wave form is also  $t_f$  and there will be something for  $t_{rs}$  and so on. Now, if the current sources were continuously on the spittle density would be simply, the sum of the two spectral density that is  $S_{I_n}$  would be simply, the sum of a the p mos current spectral density and the n mos noise current spectral density.

Now, because, they are around only for a duration of  $t_{rs}$  out of  $t_{ref}$  it turns out that the noise spectral density, will be multiplied by duty cycle. So, this turns out to be the case you can figure out, how this happens if you have a white noise source, I am here assuming only thermal noise in our white noise from the current sources. If you have a white noise source that is modulated by certain duty cycle, the output spectral density will be duty cycles times. The input spectral density, you can imagine that there are a number of current sources which are all during the different periods, you can look at standard base of calculating spectral density is to confirm this result.

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The image shows a handwritten derivation on a digital whiteboard. The equations are as follows:

$$\frac{\phi_{out}}{\phi_{ref}} = N \cdot \frac{1 + s/z_1}{1 + \frac{s}{z_1} + \frac{s^2}{\omega_{loop} z_1}} = \frac{\phi_{out}}{\phi_{n,cp}}$$

$$s_{in} = (s_{inp} + s_{inn}) \cdot \frac{T_{rst}}{T_{ref}}$$

input ref. noise of the charge pump

$$S_{s_{in,cp}} = \frac{s_{in}^2}{(I_{cp}/2\pi)^2} = \left(\frac{2\pi}{I_{cp}}\right)^2 \left[ s_{inp} + s_{inn} \right] \left( \frac{T_{rst}}{T_{ref}} \right)^2$$

$$S_{s_{out,cp}} = \left(\frac{2\pi}{I_{cp}}\right)^2 \left[ s_{inp} + s_{inn} \right] \left( \frac{T_{rst}}{T_{ref}} \right)^2 \cdot \left| \frac{\phi_{out}}{\phi_{n,cp}} \right|^2$$

Now, what will be the output phase noise as a result of this random noise, we know that  $\phi_{out}$  by  $\phi_{ref}$  is  $n$  times  $1 + g$  divided by  $1 + s$  plus  $g$   $1 + s$  square by  $\omega_u$  loop times  $g$ . So, this is also by the way equal to  $\phi_{out}$  by  $\phi_{n,cp}$ , where  $\phi_{n,cp}$  is the input refer noise of the charge pump, when I say input refer noise it is refer to the input of the phase detector and has the dimension of phase.

Now, we saw that  $s_{in}$  is nothing but, the sum of the transistor current source noise spectral densities, times reset period divided by the reference period and if I refer it to the input, of the p f d. It will be this divided by the gain of the phase detector gain from the input phase to the output current, which is  $I_{cp}$  divided by  $2\pi$  and of course, square because, we are talking about spectral densities which is  $2\pi$  by  $I_{cp}$  squared  $s_{in}$  plus  $s_{in}$  n t r s t by t ref.

And finally, the output noise spectral density due to this the output phase noise density due to the charge pump a current noise is  $2\pi$  by  $I_{cp}$  square  $s_{in}$  plus  $s_{in}$  n times t r s t by t ref times. The magnitude squared of the transfer function, I say  $\phi_{out}$  by  $\phi_{in}$  it is also the same as  $\phi_{out}$  by  $\phi_{n,cp}$  may be, I will show the explicitly here and we know that this is a low pass transfer function.

So, this is the association that gives you the contribution of the charge pump currents noise, to the output phase noise spectral density. Now, these expression looks very complicated and in general we will use a simulator to both a calculate, the spectral

density of the current sources as well as for the phase noise. But, we still need to know how to manipulated certain things in order to reduce the noise, that usually the goal up design all of the hand calculations that we do is usually for a figuring out, how to change things. So, that you minimize some imperfection of maximize some a good polities of the circuits, in this case you may want to reduce the amount of charge form noise contribution to the output, then we can use this expression to see what is it that we need to do.

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$$S_{out,cp} = \left(\frac{2\pi}{I_c}\right)^2 \left[ S_{mp} + S_{mn} \right] \left(\frac{T_{rst}}{T_{ref}}\right) \cdot \left|\frac{\beta_{out}}{\beta_{cp}}\right|^2$$

\* Reduce  $T_{rst}/T_{ref}$   $\frac{4\pi^2}{I_c^2} \frac{8}{3} kT (g_{mp} + g_{mn}) \left(\frac{T_{rst}}{T_{ref}}\right) \left|\frac{\beta_{out}}{\beta_{cp}}\right|^2$

\* Increase  $I_c$   $k_{pt} = \frac{I_c R}{2\pi}$   $= \frac{4\pi^2}{I_c^2} \frac{8}{3} kT \left[ \frac{g_{mp}}{I_c} + \frac{g_{mn}}{I_c} \right] \left(\frac{T_{rst}}{T_{ref}}\right) \left|\frac{\beta_{out}}{\beta_{cp}}\right|^2$

— reduce R  $k_{pt} = \frac{I_c R}{2\pi}$

Increase C  $k_{pt} = \frac{I_c}{2\pi C}$

\* Increase  $\left\{ \begin{array}{l} V_{ovp} - V_{TP} \\ V_{ovn} - V_{TN} \end{array} \right.$   $\left[ \frac{2}{V_{ovp} - V_{TP}} + \frac{2}{V_{ovn} - V_{TN}} \right]$

Let me copy over this expression, now first of all you see that if you reduce  $t_{rst}$  if you make a phase deductor which has very quick reset. This automatically reduces the noise contribution and if you reduce the noise of the current sources that of course, will automatically reduce the noise contribution as well. In fact, I will expand this out we know that the transistors noise currents spectral density is given by  $\frac{8}{3} kT$  and it is  $g_{mp}$  for the p mos and  $g_{mn}$  for the n mos and its multiplied by  $4$  by square by  $I_c$  square.

This is the expression we have times  $t_{rst}$  by  $t_{ref}$  times  $\pi$  out by  $I_c$  square, now this I can rewrite as  $4\pi^2$  by  $I_c^2$   $\frac{8}{3} kT$   $g_{mp}$  by  $I_c$  plus  $g_{mn}$  by  $I_c$   $t_{rst}$  by  $t_{ref}$   $\pi$  out by  $\pi$  square. Now, this quantity in brackets we know this is  $2$  by  $v_{ovp}$  minus  $v_{tp}$  plus  $2$  by  $v_{ovn}$  minus  $v_{tn}$ , so these are inversely related to the get over drives of the current source devisees. We know we have analyze this earlier and seen that

way of reducing the noise of a current source is to use a large gate, over drive for the current source devices and the same things works here.

If you want to reduce the charge form noise you use as larger a get over drive as possible for the current sources. So, that parts works and finally, you also see inverse proportionality to  $I_{cp}$ , now by the way I say I reduce the noise its assume that everything else about the PLL that like the transfer function are kept constant. Because, if I change the transfer function also too many things are changing and you may not meet some other specification here I am talking about realizing a PLL with a lesser contribution of noise from the charge pump.

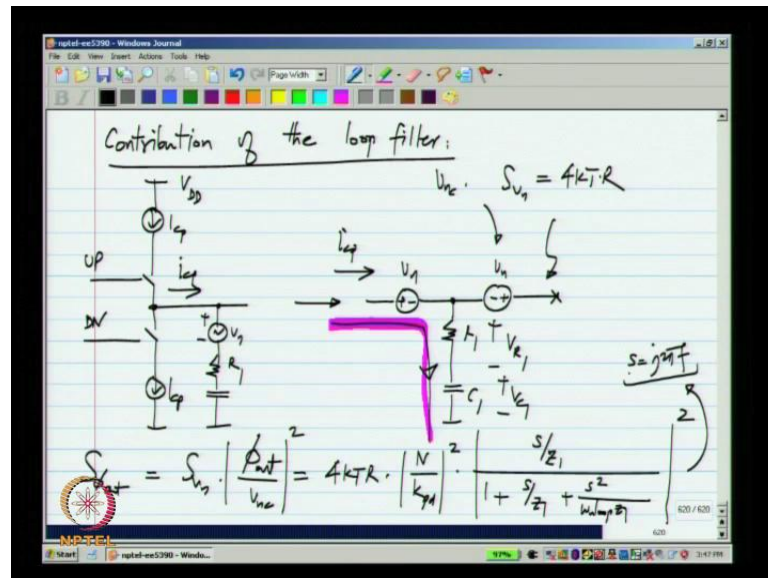
But, everything else kept the same, now this expression is inversion proportional to  $I_{cp}$  so if you increase the value of  $I_{cp}$  naturally. The charge from noise contribution will come down, but we also know that like I said you increase  $I_{cp}$ , so this also automatically means you have to reduce  $r$  and increase  $c$  this will be because,  $k_{pd}$  is  $I_{cp} r$  by  $2\pi$  and  $k_{pd} I$  is  $I_{cp}$  divided by  $2\pi c$ .

So, these things have to be maintain the same, so that means, that if you double the value of  $I_{cp}$  you have to reduce the value of  $r$  by half and double. The value of the capacitor, now you also recognizes that this is nothing, but impedance scaling of the charge form loop filter circuits. So, if you impedance scale it that is if you, lower the impedance and increase the current level the noise contribution will come down.

So, that is the way and finally, of course, as I said earlier increase  $v_{sdp}$  minus  $v_{t p}$  and  $v_{gsn}$  minus  $v_{t n}$ . So, this also works, so when you design a PLL if you find that charge form is contribute, too much noise you can try all of these things to reduce the noise. The simplest way of course, is the impedance scaling, but that also implies more power decapitation as usual it will always work to increase  $I_{cp}$  reduce  $r$  and increase the value of  $c$  you will reduce the noise contribution.

But, you have increase the power dissipation and you also increase the area if this  $c$  is realize own ship, it will occupy a large area and you have made  $d$  even large any way that is the story of the charge forms noise contribution to the output phase noise.

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Similarly, we can calculate the contribution of the loop filter, we will take the simple case where we have only the single resistor and a capacitor. It is also easier to calculate in this case we have only a single noisy component, which is  $r_1$  and this can be equivalently represented as I will only show this part. The noise of  $r_1$  can be modeled as some noise  $d_n$ , in series with  $r_1$  and we know spectral density of  $v_n$ .

Now, what I will do is I pull this  $v_n$  and put it into the two things that are connected to it, you see that let say this source is that polarity. So, what I can do is I will show  $v_n$  here and  $v_n$  there, In fact more obvious if I put a  $v_n$  on top and this diagram, all have done is the voltage here is this voltage plus  $v_n$  and instead of showing. It as a single source I split the voltage source into two parts like this. So, voltage here and there will be exactly the same and we have  $r_1$  and  $c_1$ , we have  $I_{cp}$  and this  $I_{cp}$  will flow into resistor and the capacitor just as before.

Now, this  $v_n$  has no effect it is in series with a current source, this  $v_n$  what it will do is ideally we would have got some  $v_{r_1}$  and  $v_{c_1}$  and now the control voltage of the  $v_{c_0}$  will consist of  $v_{r_1}$  plus  $v_{c_1}$  plus  $v_1$ . Now, earlier I said that I will add an error to the control voltage of the  $v_{c_0}$  and calculate its effects, on the output phase noise and now you see the context for it. The noise from the loop filter is modeled exactly by such a transfer function.

We know that this noise here will be  $v_n c$  and this spectral density is given by  $4 k t$  times  $r$  at the output phase noise, spectral density is given by  $s v_n$  times  $\pi$  out by  $v_n c$  square. Which is given by  $4 k t r$  and  $\phi$  by  $v_n v_n c$  squared is nothing, but  $n$  by  $k p d$  square times  $s$  by  $g 1$ ,  $1$  plus  $s$  by  $g 1$  plus  $s$  square by  $\omega_u$  loop  $g 1$ . The magnitude squared of this with  $s$  substituted by  $j 2 \pi f$ , the spectral density is usually represented versus, the frequency in hertz  $f$  and all we have to do is to substitute  $s$  equals  $j$  to  $\pi f$  in the transform function in order to obtain the appropriate multiplying factor.

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The image shows a digital notepad with the following content:

$$S_{\phi_{out}} = 4kTR \cdot \left| \frac{V}{k_{pd}} \right|^2 \cdot \left| \frac{s/z_1}{1 + \frac{s}{z_1} + \frac{s^2}{\omega_{loop} z_1}} \right|^2$$

Below the equation, there are handwritten notes:

- \* Reduce  $R$
- Increase  $I_c p$   $k_{pd} = I_c p / 2\pi$
- Increase  $C$   $k_{pd,1} = I_c p / 2\pi C$

These two lines are grouped under the label "Impedance scaling".

- \* Increase  $k_{pd}$
- Reduce  $k_{re}$

So, we can let me copy this over here, now again the purpose of this calculation is to figure out if we have to reduce this noise, how to go about it first of all you see that this is the band pass transfer function. It peaks at  $s$  equals  $j$  times  $s$  square of  $\omega_u$  loop times  $z_1$ , somewhere in the middle that is where the contribution of the resistant will be highest.

So, to reduce this noise what all can you do reduce the value of  $r$ , which as I said earlier you should change any other part of the transfer function, then you also have to increase  $I_c p$  and increase  $c$  this is because  $k p d$  is  $I c p$  are by  $2 \pi$  and  $k p d$  is  $I c p$  by  $2 \pi c$  you keep these things constant, you have to increase  $I c p$  and you increase  $c$  and this is nothing, but impedance scaling as usual.

So, impedance scaling will reduce the contribution of charge pump noise, as well as the loop filter noise and another thing you can do you see, that  $k p d$  is here in the



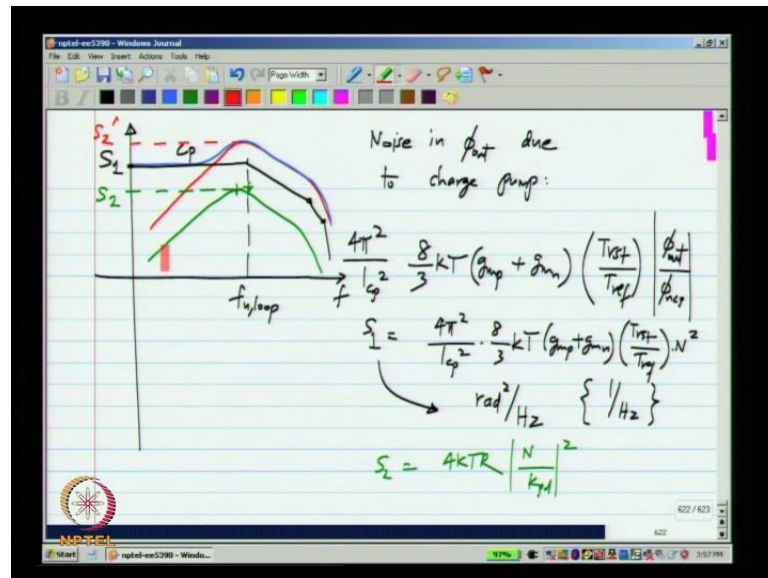
denominator you increase  $k_p d$  and this means, that you keep the loop parameters the same you have to reduce  $k_v c_o$  of by the same factor. Now, this may or may not be possible to do, but if you have to do it you will have to reduce the value  $k_v c_o$  as well. So, that we want change anything else.

Now, why does this reduce the contribution of the resistors noise that is because, if we go back to the model of the PLL here this  $v_n c$  is added over there. If you increase  $k_p d$  and reduce the value of  $k_v c_o$  you increase the gain, before you add the noise and reduce the gain, after you add the noise and that naturally leads to a reduction in the output noise. So, that is what it does and finally, this is just a feature you see that from this expression.

If  $n$  is very large then the contribution of the resistors noise can be very large because, it simply gets multiplied by  $n$  this by the way it also true, of the charge pump in the expression for the output phase noise spectral density, you have the factor  $n$  square. Which means that if you realize the PLL with a very large  $n$ , you multiply the frequency by a very large number, then these contributions can become quite significant.

Now, if the reference frequency and the output frequency are fixed there is not much you can do about this, other than let say impedance scaling to reduce the contributions. But, these things are particularly severe when you try to implement a very high gain and this is somewhat, similar to if you want to implement a very high gain amplifier, then any noise source at the input will get a amplified by the same factor as the gain. Now, we have discuss the effect of random noise of charge pump and the loop filter, what we then have to do is to figure out how to deal with the noise in the reference.

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Now, the question is now that we have calculate the effect of random noise from the charge pump, the loop filter what do we do with it or in general, whenever we calculate the output noise in a PLL. What do we do with it first of all, let us take noise in phi out due to the charge pump, we have the expression for it and that is this whole thing. So, the point is it will have the same shape as phi out by pi n c p there as to the terms here are frequency independent.

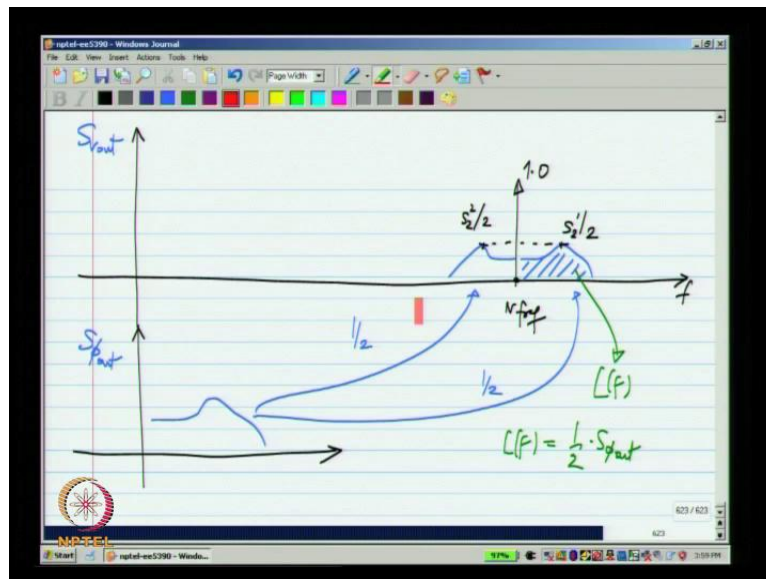
It will look like that and that and if your additional poles, it will look that where this is omega u loop. So, within the loop band width it contributes a lots of noise and this spectral density. Let me call it s 1 and s 1 will be the d c value of this and this will have dimensions of this is the phase noise spectral density, so it will have radians square for hertz or really dimensions of just 1 by frequency. F let me in being consistent with the convention for noise spectral density all this unity loop gain frequency in hertz.

So, this is the contribution of the charge pump and due to the loop filter again we calculated, that it will have a peak value of let me call it as 2 and this is due to the resistor and this is due to the charge pump. The peaks are not necessarily at this frequency, In fact, they are not at this frequency, but there will be something like that and the peak value due to that will be 4 k d r times n by k p d squared and by summing these 2 will get some noise.

Now, the way have written it  $s_1$  will dominate, but it could be that  $s_2$  dominates as well that is entirely possible. It could be that the noise to the resistor dominates and if it is like this, let say this is  $s_2$  prime then the overall noise spectral density will be something of that all. Now, what does it mean for the output to have this phase noise, what it means is that if you take the spectrum of the output signal that is  $v_{out}$  verses  $f$  ideally. It should be an impulse at a frequency  $n$  items  $f_{ref}$  in reality.

It will be smeared out and for small phase variations, we can think of it as this impulse plus some error spectrum that how, we model the reference  $p$  through and that is. Now we are going to model the phase noise, we will assume that there is impulse which carries most of the energy and there will be this basically whatever spectral density. We have we will take the blue curve. Because, it looks more interesting if we consider the green curve for the resistor noise, then the output noise will simply follow the black curve.

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Now, if we assume that it is the blue curve, then what happens is that in addition to this you will see on the spectrum analyzer. If you measure the spectrum of the output signals it is replicated on both sides, so this is what you are going to get. Where if this 1 normalize to unity what happens is this peak here, which corresponded to  $s_2$  prime will, now correspond to  $s_2$  prime by 2 and  $s_2$  prime by 2 the 2 sides.

So, in other words I have the spectrum of  $\phi$  out which look like this and it will go to that side and that side with the factor of half. So, I should really right  $s_{\phi}$  out here and  $s_v$  out here and  $s_v$  out is what you would see if you plug, the output of the phase lock loop to spectrum analyzer you will see as strong  $p$  corresponding to the periodic component at  $n$  times  $f_{ref}$  in addition to that, if it for ideally periodic you would see only that pick in addition to that you will see these side bands.

Because, of the noise and what are those side bands basically, you get half on the negative side and half on the positive side, that is half bellow  $n$  times  $f_{ref}$  and half above  $n$  times  $f_{ref}$  and they will be corresponding to the spectral density of the noise of the output phase, that is  $s_{\phi}$  out and this noise basically, which is half of  $s_{\phi}$  out is known as the phase noise, that is the official conventional definition of phase noise and that is call  $L(f)$  of  $f$  is basically half of  $s_{\phi}$  out.

What it means is if you are given an oscillator or some periodic source and told that it has a certain phase noise spectral density  $L(f)$ . So, that means, that you will see periodic component with  $L(f)$  on the positive side and  $L(f)$  reflected on the negative side. So, that is just to give a feel for where this specifications come from these are simple and conceptually similar to circuits noise, but we are dealing with phases naught voltages.

So, we will calculate the spectral density of the phase, but it that is not directly what you see what you see directly when you apply a voltage signal or a current signal in to a spectrum analyzer is, the spectrum of either the voltage or the current. Now, this is how to interrupt the spectral density of phase noise, it will cause some change in the spectral density of the output voltage or current.

It will be replicated around the periodic component and all of these things are true when the phase deviations are much smaller, than 1 that is 1 radium in next lecture, we will look at the noise of the oscillator. Such, as the  $v_{c/o}$  as well as the reference source the reference itself comes from some high quality oscillator like the crystal oscillator. We will see what a typical phase noise of that that is like then we will kind of take that as the macro model and see what the output phase noise look like.

Thank you, I will see you in the next lecture.